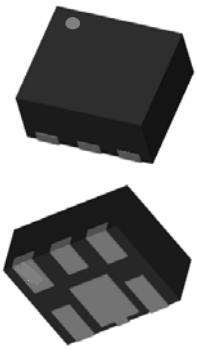
LOW CAPACITANCE TVS/ZENER ARRAYS FOR ESD PROTECTION

These 4 and 5 TVS/Zener Arrays have been designed to protect sensitive equipment against ESD in CMOS circuitry operating at 5V. These TVS arrays offers an integrated solution to protect 4 or 5 data lines in applications, where the board space is a premium, in a Quad Flat no-Lead package that only occupies an area of 1.8 sq mm.



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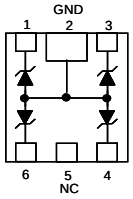

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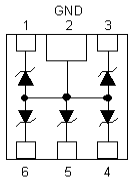


SPECIFICATION FEATURES

- **IEC61000-4-2 ESD 20kV Air, 15kV Contact Compliance**
- **Low Leakage Current, Maximum of 1µA at rated voltage**
- **Maximum Capacitance of 15pF per device at 0Vdc 1MHz**
- **Peak Power Dissipation of 20W under 8/20µs Waveform**
- **Quad Flat No Lead package QFN (1.2x1.5 sq mm, Height: 0.75mm)**
- **Lead Free Package 100% Tin Plating, Matte finish**

APPLICATIONS

- **Personal Digital Assistant (PDA)**
- **Digital Cameras**
- **Portable Instrumentation**
- **Mobile Phones and Accessories**
- **MP3 Players**

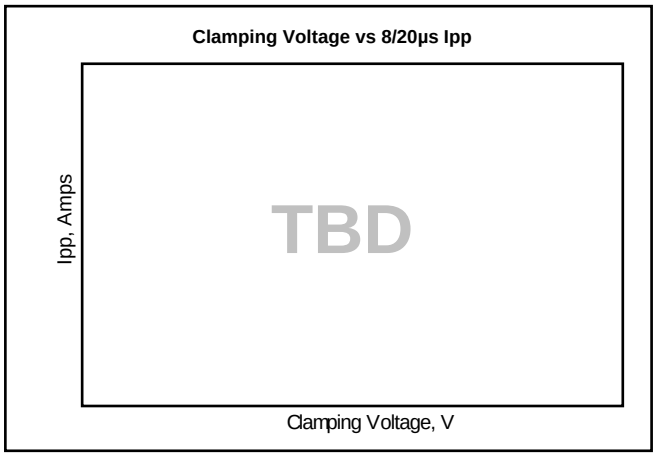
MAXIMUM RATINGS (Per Device)

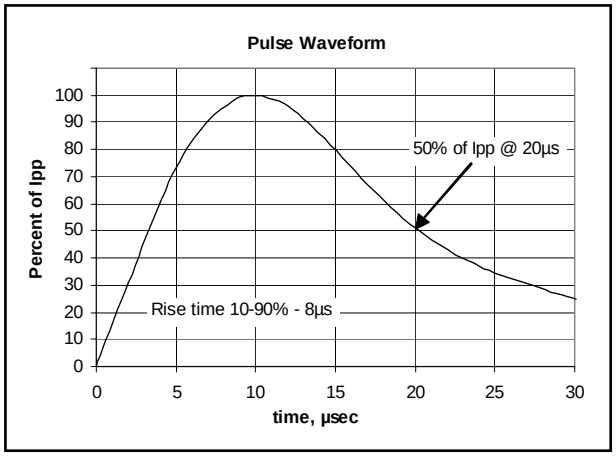
Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{PP}	20	W
Peak Pulse Current (8/20µs Waveform)	I_{PPM}	TBD	A
ESD Voltage (HBM Per MIL STD883C - Method 3015-6)	V_{ESD}	20	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

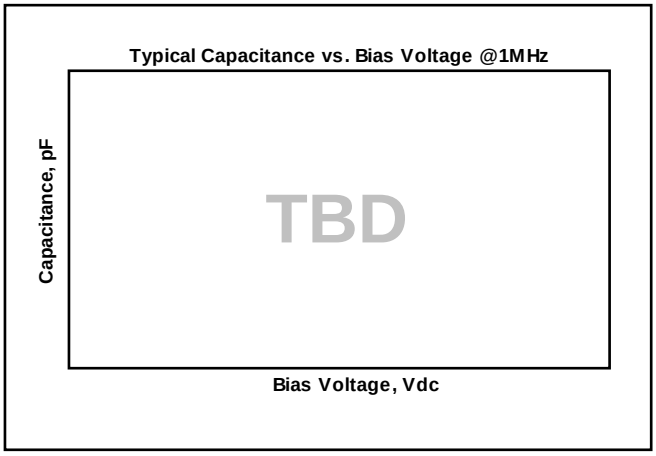
ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	6			V
Reverse Leakage Current	I_R	V_R = 5V			1	µA
Clamping Voltage (8/20µs)	V_c	Ipp = TBD		TBD	TBD	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz betweeen I/O lines and		TBD	15	pF

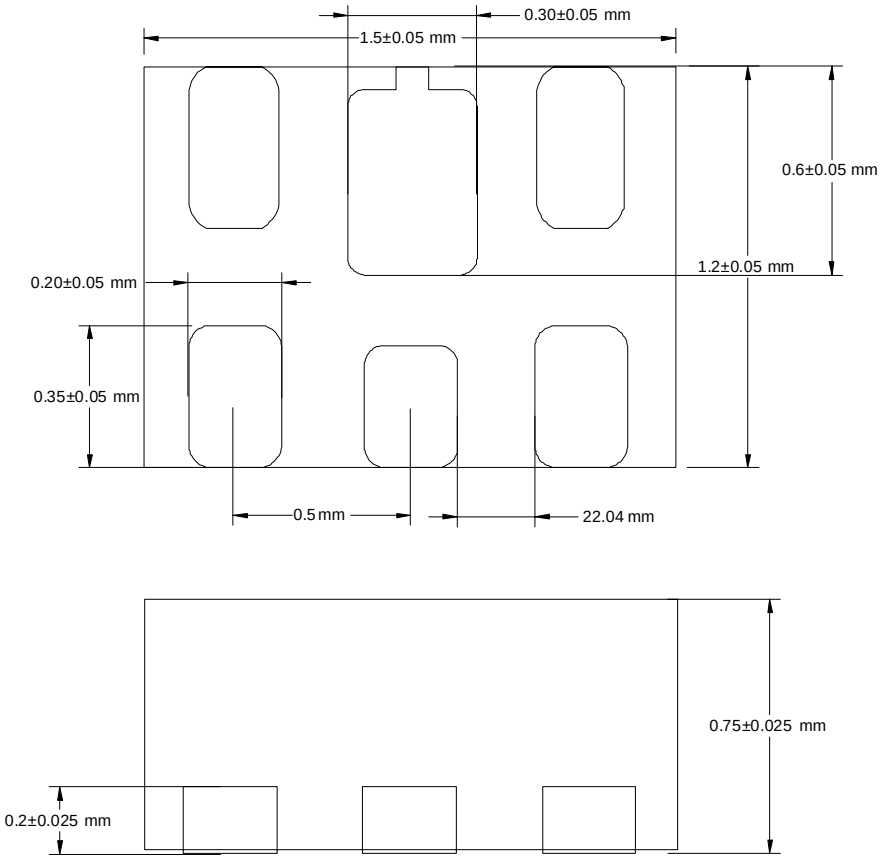
TYPICAL CHARACTERISTIC CURVES (Per Device) Tj = 25°C

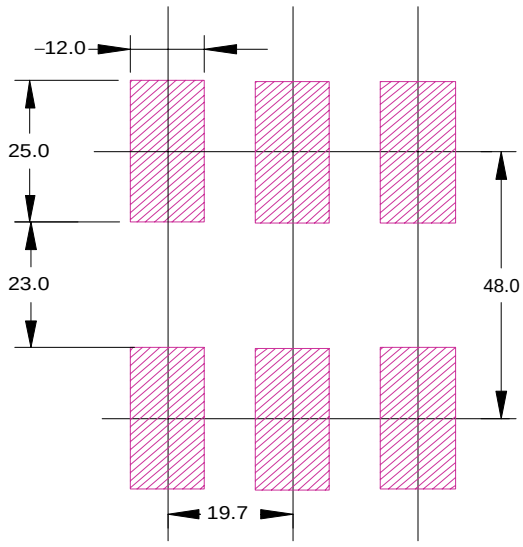




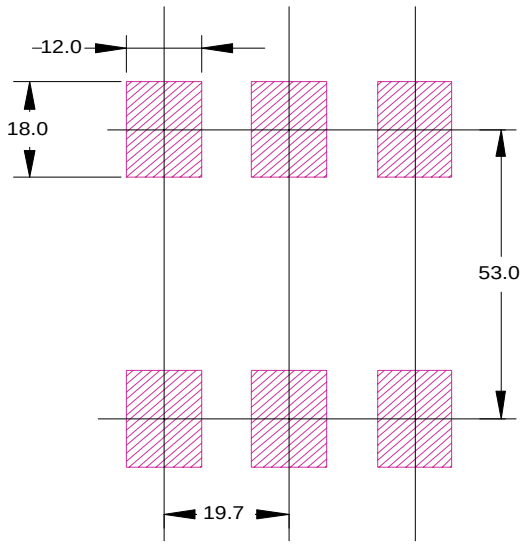


PACKAGE DIMENSIONS AND SUGGESTED PAD LAYOUT





Suggested Pad Layout (in mils)



Alternate Pad Layout SOT666 (in mils)