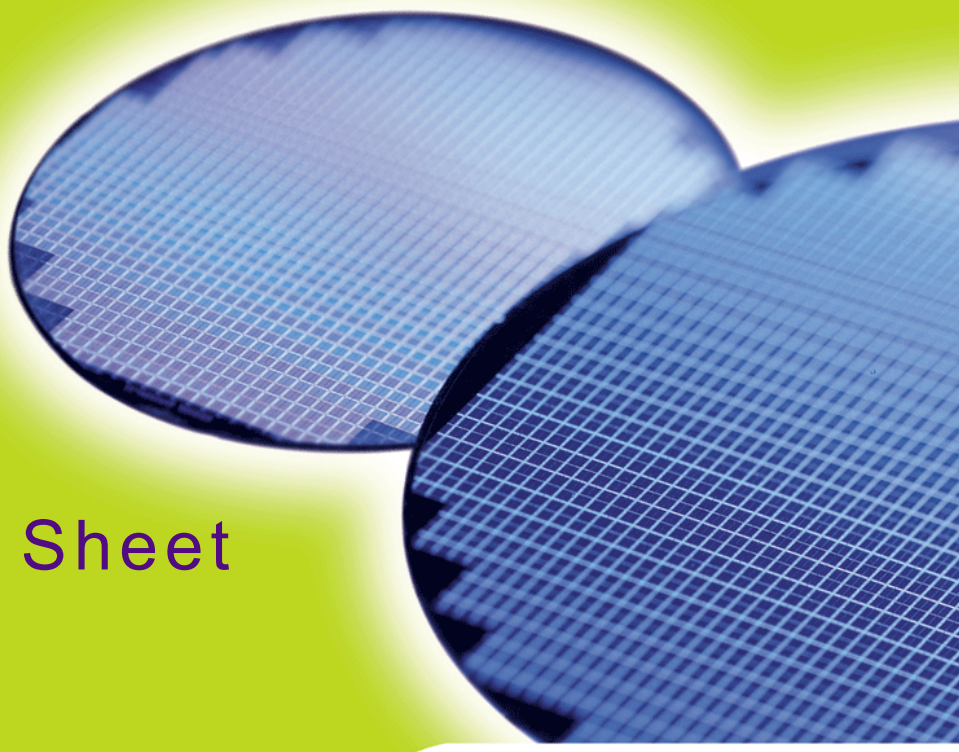
January 2007

HYS64D32301[G/H]U–5–B
HYS[64/72]D64xxx[G/H]U–[5/6]–B
HYS[64/72]D128xxx[G/H]U–[5/6]–B

184-Pin Unbuffered Double-Data-Rate Memory Modules
UDIMM
DDR SDRAM



Internet Data Sheet

Rev. 1.22

www.qimonda.com

HYS64D32301[G/H]U–5–B, HYS[64/72]D64xxx[G/H]U–[5/6]–B, HYS[64/72]D128xxx[G/H]U–[5/6]–B Revision History: 2007-01, Rev. 1.22	
Page	**Subjects (major changes since last revision)**
All	Adapted internet edition
23	t_{DQSS} min from 0.75ns to 0.72ns t_{RFC} min from 70ns to 65ns
Previous Revision: 2006-09, Rev. 1.21	
All	Qimonda update
Previous Revision: 1.2	
4	Added new product type
16	Added raw card C Diagram
18	Updated I_{DD} values
20	Added SPD Code for new product type
Previous Revision: Rev. 1.1	

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:
techdoc@qimonda.com

1 Overview

This chapter contains features and the description.

1.1 Features

- 184-Pin Unbuffered Double-Data-Rate Memory Modules (ECC and non-parity) for PC and Workstation main memory applications
- One rank 32M × 64, 64M x 64, 64M ×72 and two ranks 128M × 64, 128M ×72 organization
- standard Double Data Rate Synchronous DRAMs Single +2.5V (± 0.2V) power supply
- Built with 512-Mbit in P-TSOPII-66 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- JEDEC standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Standard reference layout
- Gold plated contacts
- DDR400 speed grade supported
- Lead-free

TABLE 1
Performance for –5 and –6

Part Number Speed Code			–5	–6	Unit
Speed Grade	Component		DDR400B	DDR333B	—
	Module		PC3200 - 3033	PC2700 - 2533	—
Max. Clock Frequency	@CL3	f_{CK3}	200	166	MHz
	@CL2.5	$f_{CK2.5}$	166	166	MHz
	@CL2	f_{CK2}	133	133	MHz

1.2 Description

The Qimonda HYS64D32301[G/H]U–5–B, HYS[64/72]D64xxx[G/H]U–[5/6]–B and HYS[64/72]D128xxx[G/H]U–[5/6]–B are industry standard 184-Pin Unbuffered Double-Data-Rate Memory Modules (UDIMM) organized as 32M × 64M (256 MB), 64M ×64 (512 MB), 128M ×64 (1 GB) for non-parity and 64M ×72 (512 MB), 128M ×72 (1 GB) for ECC main memory applications. The memory array is designed with 512Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

TABLE 2
Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC3200 (CL=3.0)			
HYS64D64300GU–5–B	PC3200U–30330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300GU–5–B	PC3200U–30330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320GU–5–B	PC3200U–30330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320GU–5–B	PC3200U–30330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC2700 (CL=2.5)			
HYS64D64300GU–6–B	PC2700U–25330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300GU–6–B	PC2700U–25330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320GU–6–B	PC2700U–25330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320GU–6–B	PC2700U–25330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC3200 (CL=3.0)			
HYS64D32301HU–5–B	PC3200U–30330–C0	one rank 256 MB DIMM	512 Mbit (×16)
HYS64D64300HU–5–B	PC3200U–30330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU–5–B	PC3200U–30330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU–5–B	PC3200U–30330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU–5–B	PC3200U–30330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)
PC2700 (CL=2.5)			
HYS64D64300HU–6–B	PC2700U–25330–A0	one rank 512 MB DIMM	512 Mbit (×8)
HYS72D64300HU–6–B	PC2700U–25330–A0	one rank 512 MB ECC-DIMM	512 Mbit (×8)
HYS64D128320HU–6–B	PC2700U–25330–B0	two ranks 1 GB DIMM	512 Mbit (×8)
HYS72D128320HU–6–B	PC2700U–25330–B0	two ranks 1 GB ECC-DIMM	512 Mbit (×8)

*Note: All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D64300HU-6-B, indicating rev. B dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example "PC2700"), the latencies and SPD code definition (for example "20330" means CAS latency of 2.0 clocks, RCD (*Row-Column-Delay*) latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 0), and the Raw Card used for this module.*

2 Pin Configuration

The pin configuration of the Unbuffered DDR SDRAM DIMM is listed by function in **Table 3** (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 4** and **Table 5** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 3
Pin Configuration of UDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
137	CK0	I	SSTL	**Clock Signals 2:0**
	NC	NC	–	
16	CK1	I	SSTL	
76	CK2	I	SSTL	
138	$\overline{CK0}$	I	SSTL	**Complement Clock Signals 2:0**
	NC	NC	–	
17	$\overline{CK1}$	I	SSTL	
75	$\overline{CK2}$	I	SSTL	
21	CKE0	I	SSTL	**Clock Enable Rank 0**
111	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2-rank module*
	NC	NC	–	*Note: 1-rank module*
Control Signals				
157	$\overline{S0}$	I	SSTL	**Chip Select Rank 0**
158	$\overline{S1}$	I	SSTL	**Chip Select Rank 1** *Note: 2-rank module*
	NC	NC	–	*Note: 1-rank module*
154	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
65	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
63	$\overline{WE}$	I	SSTL	**Write Enable**

Pin#	Name	Pin Type	Buffer Type	Function
Address Signals				
59	BA0	I	SSTL	**Bank Address Bus 2:0**
52	BA1	I	SSTL	
48	A0	I	SSTL	**Address Bus 11:0**
43	A1	I	SSTL	
41	A2	I	SSTL	
130	A3	I	SSTL	
37	A4	I	SSTL	
32	A5	I	SSTL	
125	A6	I	SSTL	
29	A7	I	SSTL	
122	A8	I	SSTL	**Address Bus 11:0**
27	A9	I	SSTL	
141	A10	I	SSTL	
	AP	I	SSTL	
118	A11	I	SSTL	
115	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
	NC	NC	–	*Note: 128 Mbit based module*
167	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	–	*Note: Module based on 512 Mbit or smaller dies*

Pin#	Name	Pin Type	Buffer Type	Function
Data Signals				
2	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
6	DQ2	I/O	SSTL	
8	DQ3	I/O	SSTL	
94	DQ4	I/O	SSTL	
95	DQ5	I/O	SSTL	
98	DQ6	I/O	SSTL	
99	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
19	DQ10	I/O	SSTL	
20	DQ11	I/O	SSTL	
105	DQ12	I/O	SSTL	
106	DQ13	I/O	SSTL	
109	DQ14	I/O	SSTL	
110	DQ15	I/O	SSTL	
23	DQ16	I/O	SSTL	
24	DQ17	I/O	SSTL	
28	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
114	DQ20	I/O	SSTL	
117	DQ21	I/O	SSTL	
121	DQ22	I/O	SSTL	
123	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
35	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
126	DQ28	I/O	SSTL	
127	DQ29	I/O	SSTL	
131	DQ30	I/O	SSTL	
133	DQ31	I/O	SSTL	
53	DQ32	I/O	SSTL	
55	DQ33	I/O	SSTL	
57	DQ34	I/O	SSTL	
60	DQ35	I/O	SSTL	
146	DQ36	I/O	SSTL	
147	DQ37	I/O	SSTL	
150	DQ38	I/O	SSTL	

Pin#	Name	Pin Type	Buffer Type	Function
151	DQ39	I/O	SSTL	**Data Bus 63:0**
61	DQ40	I/O	SSTL	
64	DQ41	I/O	SSTL	
68	DQ42	I/O	SSTL	
69	DQ43	I/O	SSTL	
153	DQ44	I/O	SSTL	
155	DQ45	I/O	SSTL	
161	DQ46	I/O	SSTL	
162	DQ47	I/O	SSTL	
72	DQ48	I/O	SSTL	
73	DQ49	I/O	SSTL	
79	DQ50	I/O	SSTL	
80	DQ51	I/O	SSTL	
165	DQ52	I/O	SSTL	
166	DQ53	I/O	SSTL	
170	DQ54	I/O	SSTL	
171	DQ55	I/O	SSTL	
83	DQ56	I/O	SSTL	
84	DQ57	I/O	SSTL	
87	DQ58	I/O	SSTL	
88	DQ59	I/O	SSTL	
174	DQ60	I/O	SSTL	
175	DQ61	I/O	SSTL	
178	DQ62	I/O	SSTL	
179	DQ63	I/O	SSTL	
44	CB0	I/O	SSTL	**Check Bit 0** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
45	CB1	I/O	SSTL	**Check Bit 1** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
49	CB2	I/O	SSTL	**Check Bit 2** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
51	CB3	I/O	SSTL	**Check Bit 3** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
134	CB4	I/O	SSTL	**Check Bit 4** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*

Pin#	Name	Pin Type	Buffer Type	Function
135	CB5	I/O	SSTL	**Check Bit 5** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
142	CB6	I/O	SSTL	**Check Bit 6** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
144	CB7	I/O	SSTL	**Check Bit 7** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
5	DQS0	I/O	SSTL	**Data Strobe Bus 7:0**
14	DQS1	I/O	SSTL	
25	DQS2	I/O	SSTL	
36	DQS3	I/O	SSTL	
56	DQS4	I/O	SSTL	
67	DQS5	I/O	SSTL	
78	DQS6	I/O	SSTL	
86	DQS7	I/O	SSTL	
47	DQS8	I/O	SSTL	**Data Strobe 8** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
97	DM0	I	SSTL	**Data Mask Bus 7:0**
107	DM1	I	SSTL	
119	DM2	I	SSTL	
129	DM3	I	SSTL	
149	DM4	I	SSTL	
159	DM5	I	SSTL	
169	DM6	I	SSTL	
177	DM7	I	SSTL	
140	DM8	I	SSTL	**Data Mask 8** *Note: ECC type module*
	NC	NC	–	*Note: Non-ECC module*
EEPROM				
92	SCL	I	CMOS	**Serial Bus Clock**
91	SDA	I/O	OD	**Serial Bus Data**
181	SA0	I	CMOS	**Slave Address Select Bus 2:0**
182	SA1	I	CMOS	
183	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
184	V_{DDSPD}	PWR	–	**EEPROM Power Supply**

Pin#	Name	Pin Type	Buffer Type	Function
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	PWRzp	–	**Power Supply**
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	GND	–	**Ground Plane**

Pin#	Name	Pin Type	Buffer Type	Function
Other Pins				
82	V_{DDID}	O	OD	**V_{DD} Identification**
9, 10, 71, 90, 101, 102, 103, 113, 163, 173	NC	NC	–	**Not connected**

TABLE 4
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

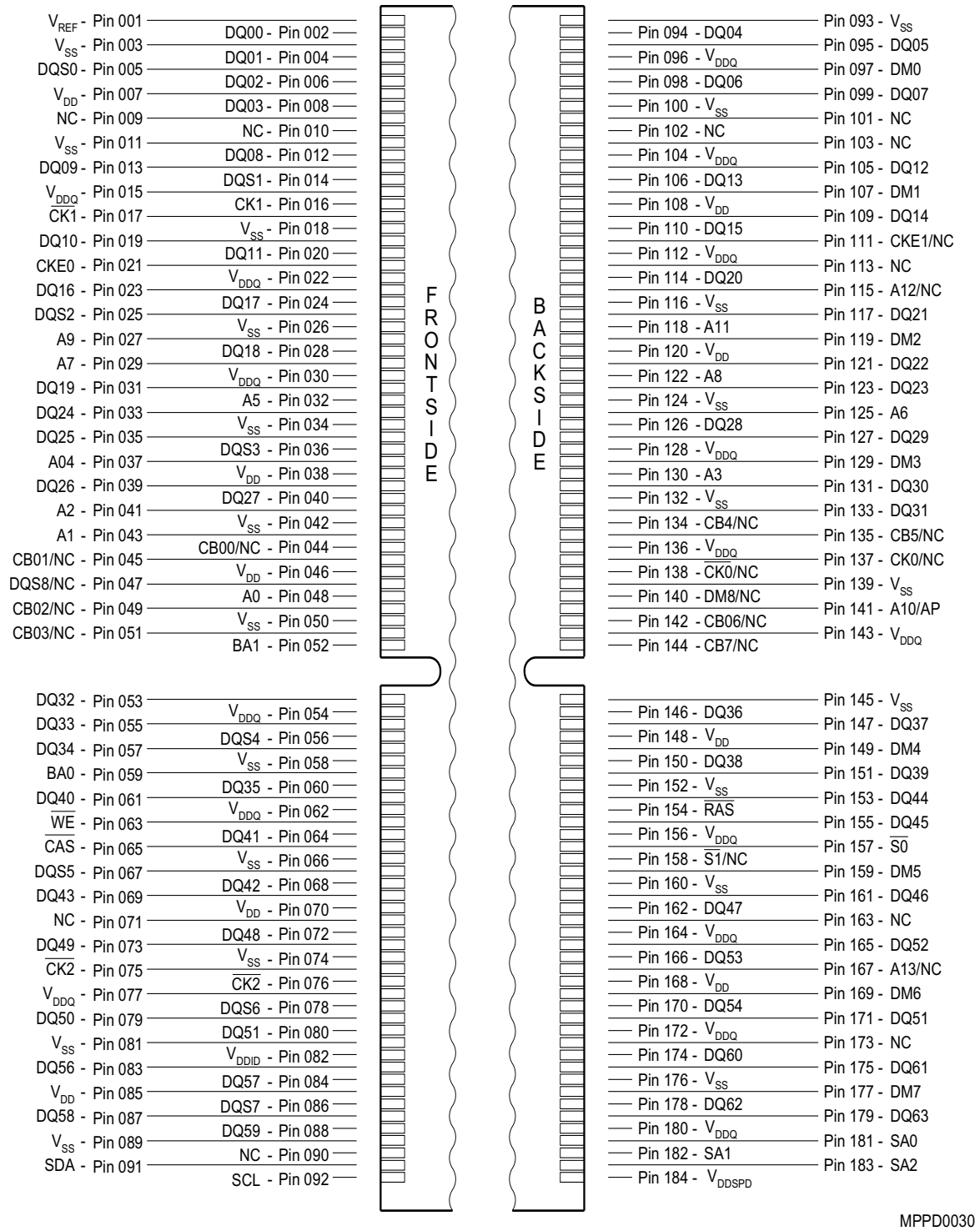
TABLE 5
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

TABLE 6
Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M ×64	1	32M ×16	4	13/2/9	8K	64 ms	7.8 ms
512 MB	64M ×64	1	64M ×8	8	13/2/11	8K	64 ms	7.8 ms
512 MB	64M ×72	1	64M ×8	8	13/2/11	8K	64 ms	7.8 ms
1 GB	128M ×64	2	64M ×8	16	13/2/12	8K	64 ms	7.8 ms
1 GB	128M ×72	2	64M ×8	18	13/2/12	8K	64 ms	7.8 ms

FIGURE 1
Pin Configuration 184-Pin, UDIMM



3 Electrical Characteristics

This chapter lists the electrical characteristics.

3.1 Operating Conditions

This chapter describes the operating conditions.

TABLE 7
Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	—	V_{DDQ} + 0.5	V	—
Voltage on inputs relative to V_{SS}	V_{IN}	–1	—	+3.6	V	—
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	—	+3.6	V	—
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	—	+3.6	V	—
Operating temperature (ambient)	T_A	0	—	+70	°C	—
Storage temperature (plastic)	T_{STG}	–55	—	+150	°C	—
Power dissipation (per SDRAM component)	PD	—	1	—	W	—
Short circuit output current	I_{OUT}	—	50	—	mA	—

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

TABLE 8
Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note[1] / Test Condition
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2)3)]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0	—	0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04	—	V_{REF} + 0.04	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15	—	V_{DDQ} + 0.3	V	[8]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3	—	V_{REF} – 0.15	V	[8]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3	—	V_{DDQ} + 0.3	V	[8]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36	—	V_{DDQ} + 0.6	V	[8)6)]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71	—	1.4	—	[7]
Input Leakage Current	I_I	–2	—	2	µA	Any input 0 V ≤ $V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [8)9)]
Output Leakage Current	I_{OZ}	–5	—	5	µA	DQs are disabled; 0 V ≤ $V_{OUT} \leq V_{DDQ}$ [8]
Output High Current, Normal Strength Driver	I_{OH}	—	—	–16.2	mA	V_{OUT} = 1.95 V [8]
Output Low Current, Normal Strength Driver	I_{OL}	16.2	—	—	mA	V_{OUT} = 0.35 V [8]

1) 0 °C ≤ T_A ≤ 70 °C
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% VREF (DC). VREF is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
8) Inputs are not recognized as valid until V_{REF} stabilizes.
9) Values are shown per component

TABLE 9
AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note[1] / Test Condition
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	Min. (t_{CL}, t_{CH})		Min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK}	5	8	—	—	ns	CL = 3.0 2)3)4)5)
		6	12	7.5	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
DQ/DQS output hold time	t_{QH}	t_{HP} –t_{QHS}		t_{HP} –t_{QHS}		ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	Fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	Slow slew rate 3)4)5)6)10)

Parameter	Symbol	–5		–6		Unit	Note[1] / Test Condition
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	Fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	Slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	70	—	72	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	$t_{RCD} - t_{RASmin}$				ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	—	—	—	—	t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)
2) Input slew rate ≥ 1 V/ns for DDR400, DDR333
3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.
4) Inputs are not recognized as valid until V_{REF} stabilizes.
5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.
6) These parameters guarantee device timing, but they are not necessarily tested on each device.
7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
10) Fast slew rate ≥ 1.0 V/ns, slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.
11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

3.2 Current Conditions and Specification

This chapter describes the Conditions and Specification.

TABLE 10
I_{DD} Specification for HYS[64/72]D[32/64/128]3xxHU–5–B

Product Type	HYS64D32301HU–5–B		HYS64D64300HU–5–B HYS64D64300GU–5–B		HYS72D64300HU–5–B HYS72D64300GU–5–B		HYS64D128320HU–5–B HYS64D128320GU–5–B		HYS72D128320HU–5–B		Unit	Note [1)2)]
Organization	256 MB		512 MB		512 MB		1 GB		1 GB			
	×64		×64		×64		×64		×72			
	1 Rank		1 Rank		1 Rank		2 Ranks		2 Ranks			
	–5		–5		–5		–5		–5			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	400	480	640	800	720	900	950	1180	1070	1330	mA	3)
I_{DD1}	460	560	720	880	810	990	1030	1260	1160	1420	mA	3)4)
I_{DD2P}	10	20	10	30	20	40	30	64	31	70	mA	5)
I_{DD2F}	120	140	240	290	270	320	480	580	540	650	mA	5)
I_{DD2Q}	80	100	150	210	170	230	300	420	340	470	mA	5)
I_{DD3P}	50	60	100	130	110	140	190	260	220	290	mA	5)
I_{DD3N}	170	200	310	380	350	420	620	750	700	850	mA	5)
I_{DD4R}	480	580	680	800	770	900	990	1180	1120	1320	mA	3)4)
I_{DD4W}	500	600	720	840	810	950	1030	1220	1160	1370	mA	3)
I_{DD5}	820	980	1640	1960	1850	2210	1950	2340	2200	2630	mA	3)
I_{DD6}	11	20.8	22	42	30	50	45	80	50	90	mA	3)
I_{DD7}	1140	1360	2080	2480	2340	2790	2390	2860	2690	3210	mA	3)4)

1) DRAM component currents only
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx} [component] + **n** × I_{DD3N} [component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx} [component]

TABLE 11

I_{DD} Specification for HYS[64/72]D[64/128]3xxHU–6–B

Product Type	HYS64D64300HU–6–B HYS64D64300GU–6–B		HYS72D64300HU–6–B HYS72D64300GU–6–B		HYS64D128320HU–6–B HYS64D128320GU–6–B		HYS72D128320HU–6–B		Unit	Note [1)2)]
Organization	512 MB		512 MB		1 GB		1 GB			
	×64		×72		×64		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–6		–6		–6		–6			
Symbol	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD0}	600	720	680	810	880	1050	990	1180	mA	3)
I_{DD1}	680	800	770	900	960	1130	1080	1270	mA	3)4)
I_{DD2P}	10	30	10	40	30	64	290	70	mA	5)
I_{DD2F}	200	240	230	270	400	480	450	540	mA	5)
I_{DD2Q}	140	190	150	220	270	380	310	430	mA	5)
I_{DD3P}	90	120	100	140	180	240	200	270	mA	5)
I_{DD3N}	280	330	320	370	560	660	630	740	mA	5)
I_{DD4R}	620	720	690	810	900	1050	1010	1180	mA	3)4)
I_{DD4W}	650	760	730	860	930	1090	1040	1220	mA	3)
I_{DD5}	1480	1760	1670	1980	1760	2090	1980	2350	mA	3)
I_{DD6}	22	42	24	47	43	80	49	94	mA	3)
I_{DD7}	1870	2230	2110	2510	2150	2560	2420	2880	mA	3)4)

1) DRAM component currents only
2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C
3) The module I_{DDx} values are calculated from the component I_{DDx} data sheet values as: **m** × I_{DDx} [component] + **n** × I_{DD3N} [component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules
4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions
5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (**m** + **n**) × I_{DDx} [component]

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 12
HYS[64/72]D[64/128]3x0GU-5-B

Product Type		HYS64D64300GU–5–B	HYS72D64300GU–5–B	HYS64D128320GU–5–B	HYS72D128320GU–5–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U–30330	PC3200U–30330	PC3200U–30330	PC3200U–30330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E^2PROM	80	80	80	80
1	Total number of Bytes in E^2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support	00	02	00	02

Product Type		**HYS64D64300GU–5–B**	**HYS72D64300GU–5–B**	**HYS64D128320GU–5–B**	**HYS72D128320GU–5–B**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U–30330**	**PC3200U–30330**	**PC3200U–30330**	**PC3200U–30330**
JEDEC SPD Revision		**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	1C	1C	1C	1C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	60	60	60
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	50	50	50	50
25	t_{CK}@ CL_{max} -1 (Byte 18) [ns]	75	75	75	75
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50	50
27	t_{RPmin} [ns]	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C
30	t_{RASmin} [ns]	28	28	28	28
31	Module Density per Rank	80	80	80	80
32	$t_{AS,}$ t_{CS} [ns]	60	60	60	60
33	$t_{AH,}$ t_{CH} [ns]	60	60	60	60
34	t_{DS} [ns]	40	40	40	40
35	t_{DH} [ns]	40	40	40	40
36 - 40	Not used	00	00	00	00
41	t_{RCmin} [ns]	37	37	37	37

Product Type		HYS64D64300GU–5–B	HYS72D64300GU–5–B	HYS64D128320GU–5–B	HYS72D128320GU–5–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U–30330	PC3200U–30330	PC3200U–30330	PC3200U–30330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
42	t_{RFCmin} [ns]	41	41	41	41
43	t_{CKmax} [ns]	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50
46	Not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	Not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	3E	50	3F	51
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32

Product Type		HYS64D64300GU–5–B	HYS72D64300GU–5–B	HYS64D128320GU–5–B	HYS72D128320GU–5–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U–30330	PC3200U–30330	PC3200U–30330	PC3200U–30330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
81	Part Number, Char 9	47	47	30	30
82	Part Number, Char 10	55	55	47	47
83	Part Number, Char 11	35	35	55	55
84	Part Number, Char 12	42	42	35	35
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

TABLE 13
HYS[64/72]D[64/128]3x0GU-6-B

Product Type		HYS64D64300GU–6–B	HYS72D64300GU–6–B	HYS64D128320GU–6–B	HYS72D128320GU–6–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U–25330	PC2700U–25330	PC2700U–25330	PC2700U–25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E^2PROM	80	80	80	80
1	Total number of Bytes in E^2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1

Product Type		**HYS64D64300GU–6–B**	**HYS72D64300GU–6–B**	**HYS64D128320GU–6–B**	**HYS72D128320GU–6–B**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**	**PC2700U–25330**	**PC2700U–25330**	**PC2700U–25330**
JEDEC SPD Revision		**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75	75	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max}-1 (Byte 18) [ns]	00	00	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00	00	00
27	t_{RPmin} [ns]	48	48	48	48
28	t_{RRDmin} [ns]	30	30	30	30
29	t_{RCDmin} [ns]	48	48	48	48
30	t_{RASmin} [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	80	80
32	t_{AS}, t_{CS} [ns]	75	75	75	75
33	t_{AH}, t_{CH} [ns]	75	75	75	75
34	t_{DS} [ns]	45	45	45	45
35	t_{DH} [ns]	45	45	45	45
36 - 40	Not used	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C
42	t_{RFCmin} [ns]	48	48	48	48
43	t_{CKmax} [ns]	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D
45	t_{QHSmax} [ns]	55	55	55	55
46	Not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	Not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	42	54	43	55
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F

Product Type		HYS64D64300GU–6–B	HYS72D64300GU–6–B	HYS64D128320GU–6–B	HYS72D128320GU–6–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U–25330	PC2700U–25330	PC2700U–25330	PC2700U–25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	47	47	30	30
82	Part Number, Char 10	55	55	47	47
83	Part Number, Char 11	36	36	55	55
84	Part Number, Char 12	42	42	36	36
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x

Product Type		**HYS64D64300GU–6–B**	**HYS72D64300GU–6–B**	**HYS64D128320GU–6–B**	**HYS72D128320GU–6–B**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**	**PC2700U–25330**	**PC2700U–25330**	**PC2700U–25330**
JEDEC SPD Revision		**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

TABLE 14
HYS[64/72]D[32/64/128]3xxHU-5-B

Product Type		HYS64D32301HU–5–B	HYS64D64300HU–5–B	HYS72D64300HU–5–B	HYS64D128320HU–5–B	HYS72D128320HU–5–B
Organization		256MB	512MB	512MB	1 GByte	1 GByte
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U –30331	PC3200U –30330	PC3200U –30330	PC3200U –30330	PC3200U –30330
JEDEC SPD Revision		Rev. 1.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E^2PROM	80	80	80	80	80
1	Total number of Bytes in E^2PROM	08	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D	0D
4	Number of Column Addresses	0A	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	01	02	02
6	Data Width (LSB)	40	40	48	40	48
7	Data Width (MSB)	00	00	00	00	00
8	Interface Voltage Levels	04	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50	50	50
11	Error Correction Support	00	00	02	00	02
12	Refresh Rate	82	82	82	82	82
13	Primary SDRAM Width	10	08	08	08	08
14	Error Checking SDRAM Width	00	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	CAS Latency	1C	1C	1C	1C	1C
19	CS Latency	01	01	01	01	01
20	Write Latency	02	02	02	02	02
21	DIMM Attributes	20	20	20	20	20
22	Component Attributes	C1	C1	C1	C1	C1

Product Type		**HYS64D32301HU–5–B**	**HYS64D64300HU–5–B**	**HYS72D64300HU–5–B**	**HYS64D128320HU–5–B**	**HYS72D128320HU–5–B**
Organization		**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U –30331**	**PC3200U –30330**	**PC3200U –30330**	**PC3200U –30330**	**PC3200U –30330**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	60	60	60	60	60
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	50	50	50	50	50
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	75	75	75	75	75
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50	50	50
27	t_{RPmin} [ns]	3C	3C	3C	3C	3C
28	t_{RRDmin} [ns]	28	28	28	28	28
29	t_{RCDmin} [ns]	3C	3C	3C	3C	3C
30	t_{RASmin} [ns]	28	28	28	28	28
31	Module Density per Rank	40	80	80	80	80
32	t_{AS}, t_{CS} [ns]	60	60	60	60	60
33	t_{AH}, t_{CH} [ns]	60	60	60	60	60
34	t_{DS} [ns]	40	40	40	40	40
35	t_{DH} [ns]	40	40	40	40	40
36 - 40	Not used	00	00	00	00	00
41	t_{RCmin} [ns]	37	37	37	37	37
42	t_{RFCmin} [ns]	41	41	41	41	41
43	t_{CKmax} [ns]	28	28	28	28	28
44	$t_{DQSQmax}$ [ns]	28	28	28	28	28
45	t_{QHSmax} [ns]	50	50	50	50	50
46	Not used	00	00	00	00	00
47	DIMM PCB Height	01	00	00	00	00
48 - 61	Not used	00	00	00	00	00
62	SPD Revision	10	00	00	00	00
63	Checksum of Byte 0-62	16	3E	50	3F	51
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F	7F

Product Type		HYS64D32301HU–5–B	HYS64D64300HU–5–B	HYS72D64300HU–5–B	HYS64D128320HU–5–B	HYS72D128320HU–5–B
Organization		256MB	512MB	512MB	1 GByte	1 GByte
		×64	×64	×72	×64	×72
		1 Rank (×16)	1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC3200U –30331	PC3200U –30330	PC3200U –30330	PC3200U –30330	PC3200U –30330
JEDEC SPD Revision		Rev. 1.0	Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX	HEX
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Part Number, Char 1	36	36	37	36	37
74	Part Number, Char 2	34	34	32	34	32
75	Part Number, Char 3	44	44	44	44	44
76	Part Number, Char 4	33	36	36	31	31
77	Part Number, Char 5	32	34	34	32	32
78	Part Number, Char 6	33	33	33	38	38
79	Part Number, Char 7	30	30	30	33	33
80	Part Number, Char 8	31	30	30	32	32
81	Part Number, Char 9	48	48	48	30	30
82	Part Number, Char 10	55	55	55	48	48
83	Part Number, Char 11	35	35	35	55	55
84	Part Number, Char 12	42	42	42	35	35
85	Part Number, Char 13	20	20	20	42	42
86	Part Number, Char 14	20	20	20	20	20
87	Part Number, Char 15	20	20	20	20	20
88	Part Number, Char 16	20	20	20	20	20
89	Part Number, Char 17	20	20	20	20	20

Product Type		**HYS64D32301HU–5–B**	**HYS64D64300HU–5–B**	**HYS72D64300HU–5–B**	**HYS64D128320HU–5–B**	**HYS72D128320HU–5–B**
Organization		**256MB**	**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×64**	**×72**	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC3200U –30331**	**PC3200U –30330**	**PC3200U –30330**	**PC3200U –30330**	**PC3200U –30330**
JEDEC SPD Revision		**Rev. 1.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**	**HEX**
90	Part Number, Char 18	20	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00

TABLE 15
HYS[64/72]D[64/128]3x0HU-6-B

Product Type		HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U–25330	PC2700U–25330	PC2700U–25330	PC2700U–25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E^2PROM	80	80	80	80
1	Total number of Bytes in E^2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0B	0B
5	Number of DIMM Ranks	01	01	02	02
6	Data Width (LSB)	40	48	40	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	t_{CK} @ CL_{max} (Byte 18) [ns]	60	60	60	60
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	00	02	00	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	t_{CCD} [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	20	20	20	20
22	Component Attributes	C1	C1	C1	C1

Product Type		HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U–25330	PC2700U–25330	PC2700U–25330	PC2700U–25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
23	t_{CK} @ CL_{max} -0.5 (Byte 18) [ns]	75	75	75	75
24	t_{AC} SDRAM @ CL_{max} -0.5 [ns]	70	70	70	70
25	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	00	00	00	00
26	t_{AC} SDRAM @ CL_{max} -1 [ns]	00	00	00	00
27	t_{RPmin} [ns]	48	48	48	48
28	t_{RRDmin} [ns]	30	30	30	30
29	t_{RCDmin} [ns]	48	48	48	48
30	t_{RASmin} [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	80	80
32	t_{AS}, t_{CS} [ns]	75	75	75	75
33	t_{AH}, t_{CH} [ns]	75	75	75	75
34	t_{DS} [ns]	45	45	45	45
35	t_{DH} [ns]	45	45	45	45
36 - 40	Not used	00	00	00	00
41	t_{RCmin} [ns]	3C	3C	3C	3C
42	t_{RFCmin} [ns]	48	48	48	48
43	t_{CKmax} [ns]	30	30	30	30
44	$t_{DQSQmax}$ [ns]	2D	2D	2D	2D
45	t_{QHSmax} [ns]	55	55	55	55
46	Not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	Not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	42	54	43	55
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F

Product Type		HYS64D64300HU–6–B	HYS72D64300HU–6–B	HYS64D128320HU–6–B	HYS72D128320HU–6–B
Organization		512MB	512MB	1 GByte	1 GByte
		×64	×72	×64	×72
		1 Rank (×8)	1 Rank (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2700U–25330	PC2700U–25330	PC2700U–25330	PC2700U–25330
JEDEC SPD Revision		Rev. 0.0	Rev. 0.0	Rev. 0.0	Rev. 0.0
Byte#	Description	HEX	HEX	HEX	HEX
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	36	37	36	37
74	Part Number, Char 2	34	32	34	32
75	Part Number, Char 3	44	44	44	44
76	Part Number, Char 4	36	36	31	31
77	Part Number, Char 5	34	34	32	32
78	Part Number, Char 6	33	33	38	38
79	Part Number, Char 7	30	30	33	33
80	Part Number, Char 8	30	30	32	32
81	Part Number, Char 9	48	48	30	30
82	Part Number, Char 10	55	55	48	48
83	Part Number, Char 11	36	36	55	55
84	Part Number, Char 12	42	42	36	36
85	Part Number, Char 13	20	20	42	42
86	Part Number, Char 14	20	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x

Product Type		**HYS64D64300HU–6–B**	**HYS72D64300HU–6–B**	**HYS64D128320HU–6–B**	**HYS72D128320HU–6–B**
Organization		**512MB**	**512MB**	**1 GByte**	**1 GByte**
		×64	**×72**	**×64**	**×72**
		1 Rank (×8)	**1 Rank (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2700U–25330**	**PC2700U–25330**	**PC2700U–25330**	**PC2700U–25330**
JEDEC SPD Revision		**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**	**Rev. 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00

5 Package Outlines

This chapter contains the package outlines of the products.

FIGURE 2
Raw Card C DDR UDIMM HYS64D32301HU–5–B (1 Rank Module)

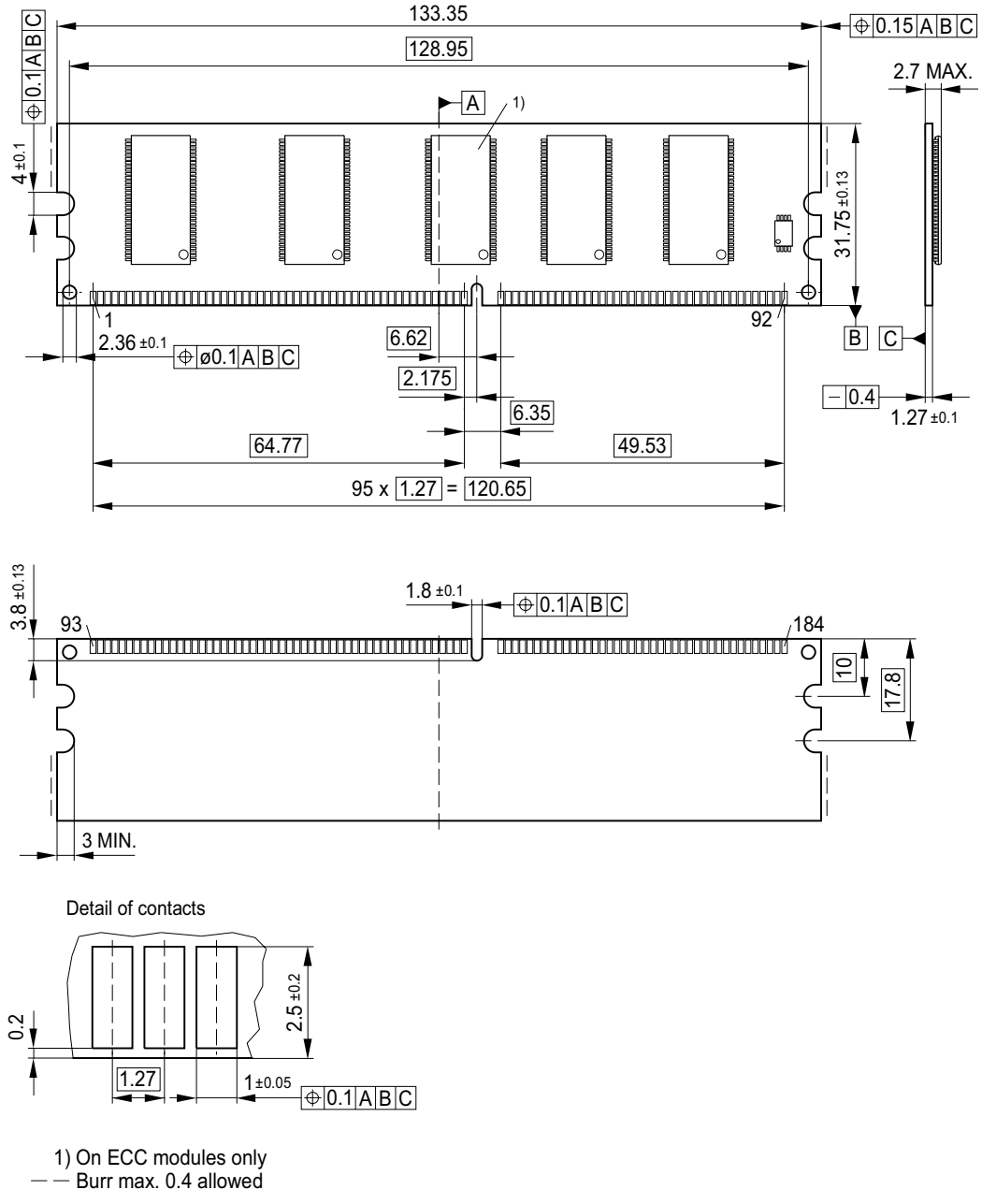


FIGURE 3
Raw Card A DDR UDIMM HYS64D64300HU–[5/6/7]–B (1 Rank Module)

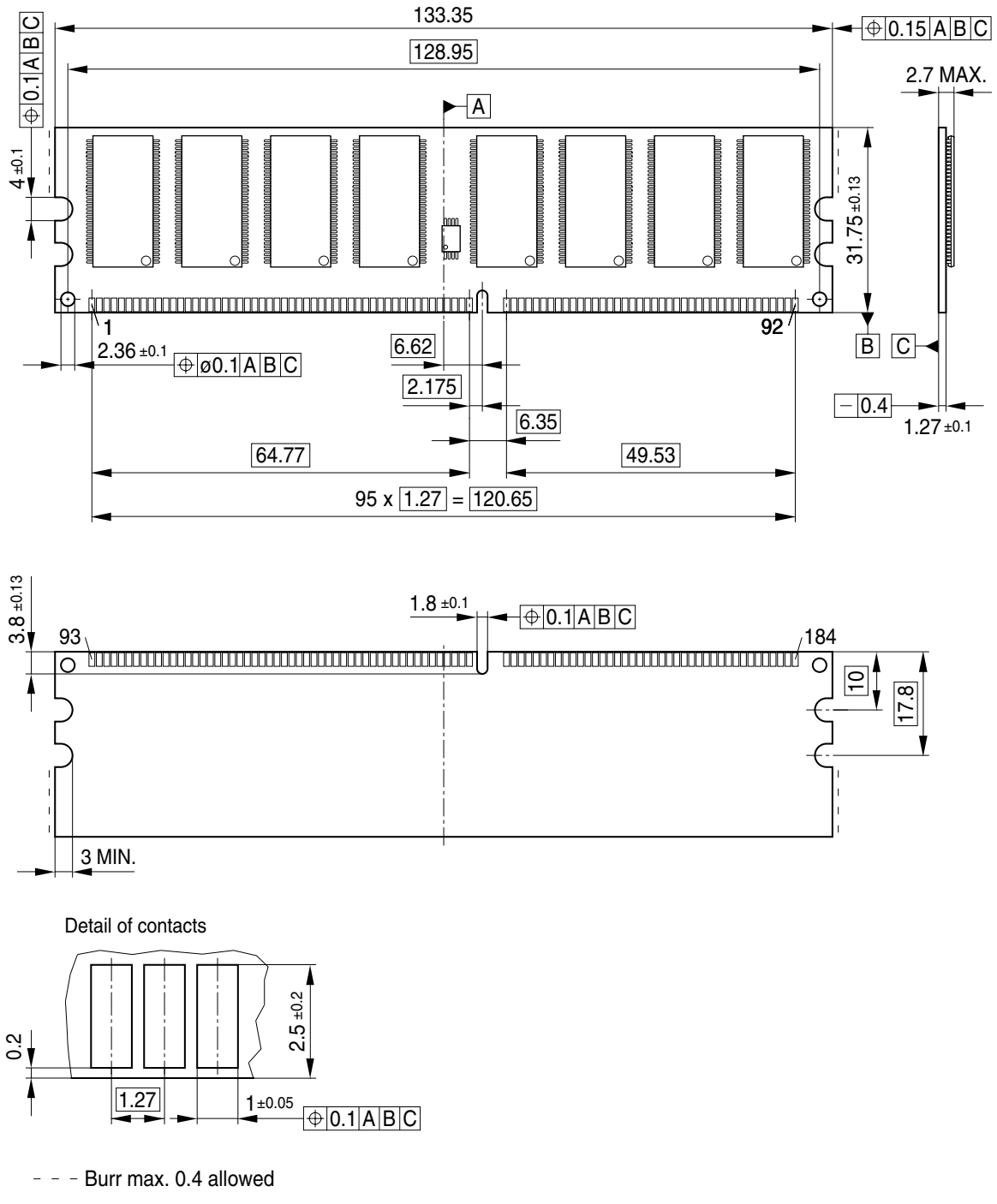
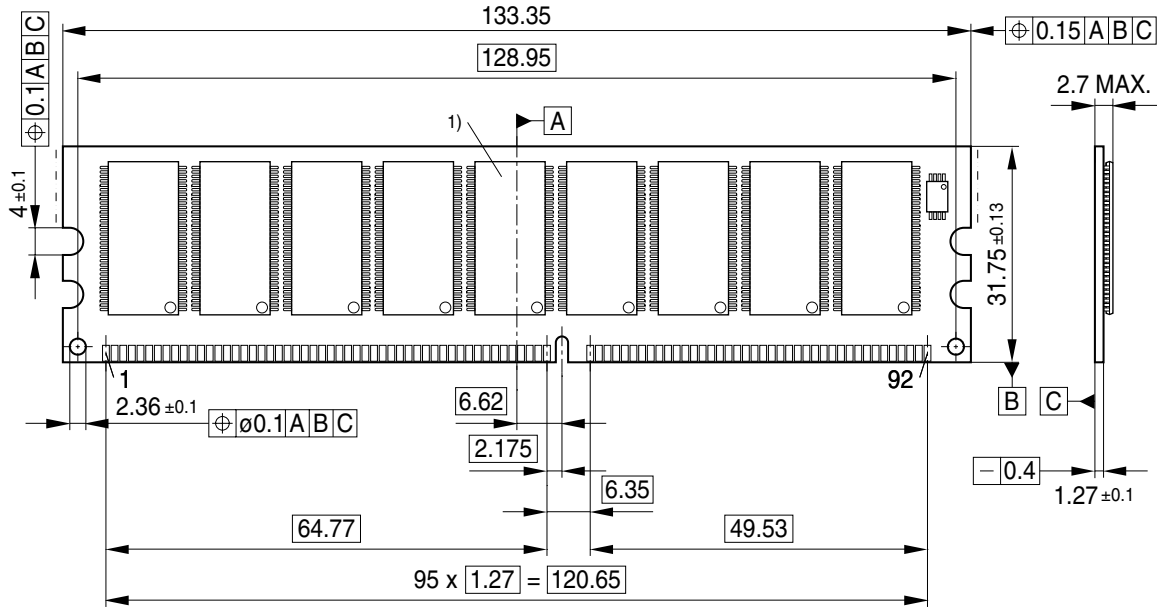
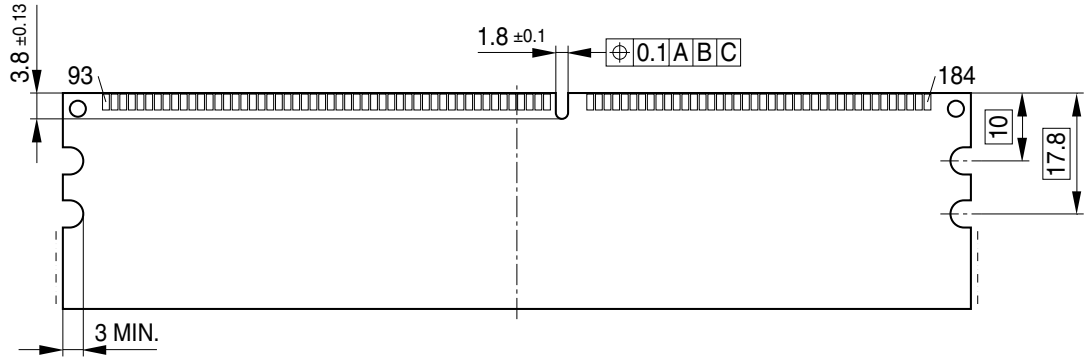
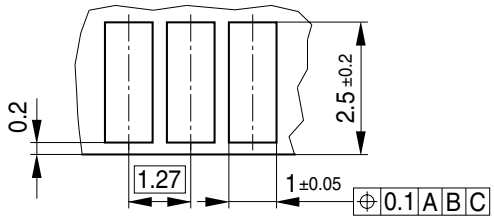


FIGURE 4
Raw Card A DDR UDIMM HYS72D64300HU–[5/6/7F]–B (1 Rank Module)





Detail of contacts



1) On ECC modules only
- - - Burr max. 0.4 allowed

FIGURE 5

Raw Card B DDR UDIMM HYS64D128320HU–[5/6/7]–B (2 Ranks Module)

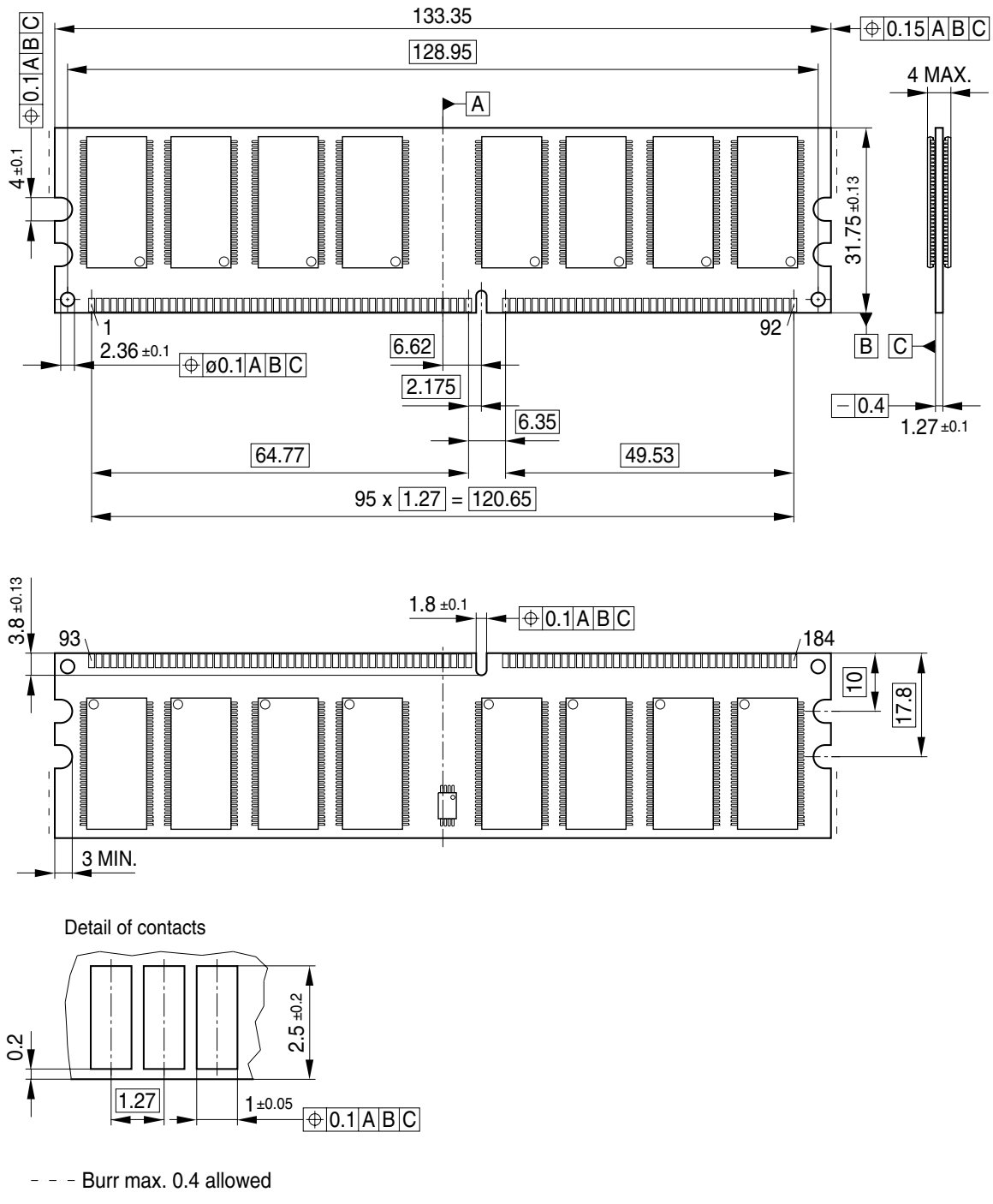
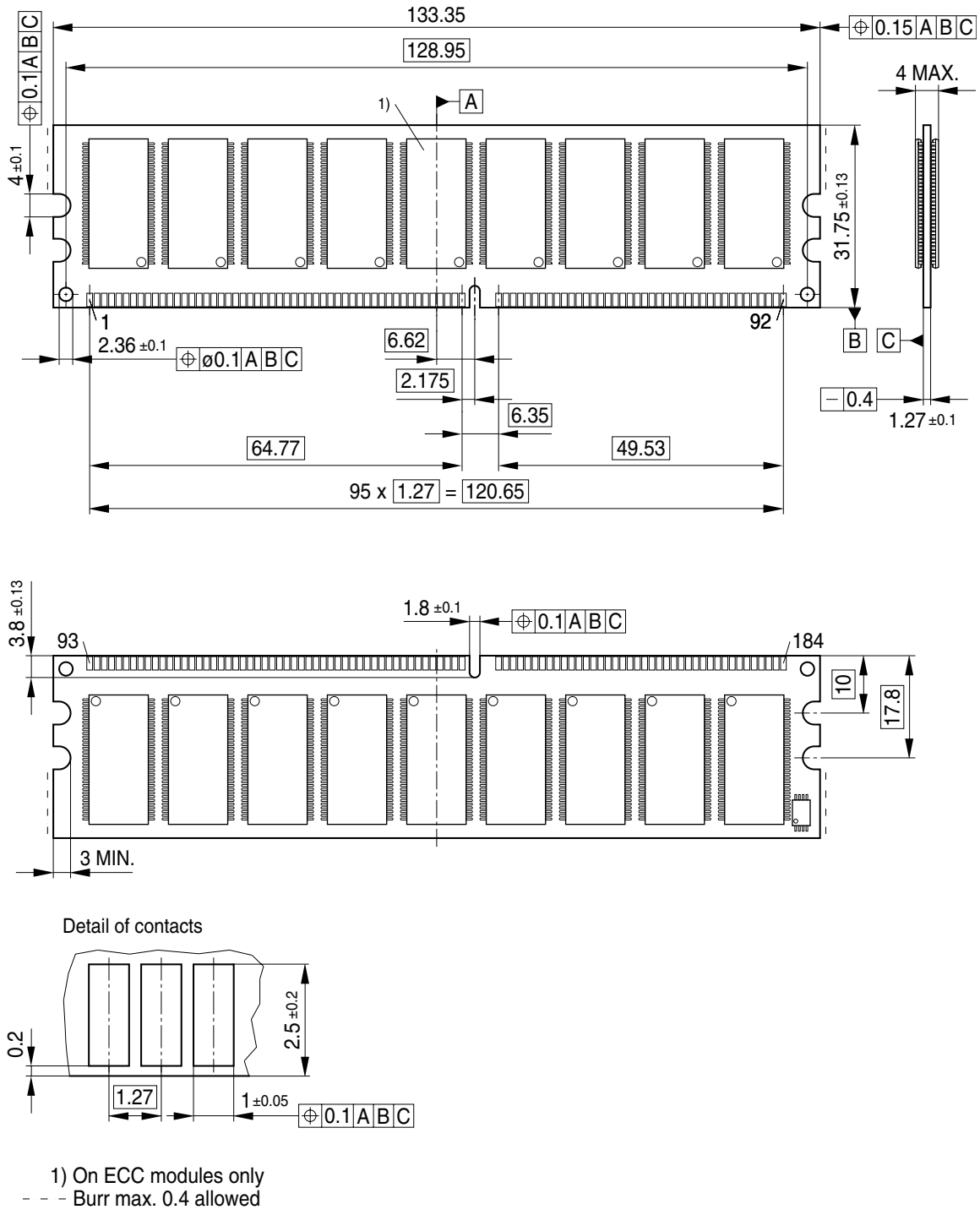


FIGURE 6
Raw Card B DDR UDIMM HYS72D128320HU–[5/6/7]–B (2 Rank Module)



1) On ECC modules only
- - - Burr max. 0.4 allowed

Table of Contents

Edition 2007-01
Published by Qimonda AG
Gustav-Heinemann-Ring 212
D-81739 München, Germany

Legal Disclaimer

The information given in this Internet Data Sheet shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Qimonda hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Qimonda Office.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Qimonda Office.
Qimonda Components may only be used in life-support devices or systems with the express written approval of Qimonda, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.