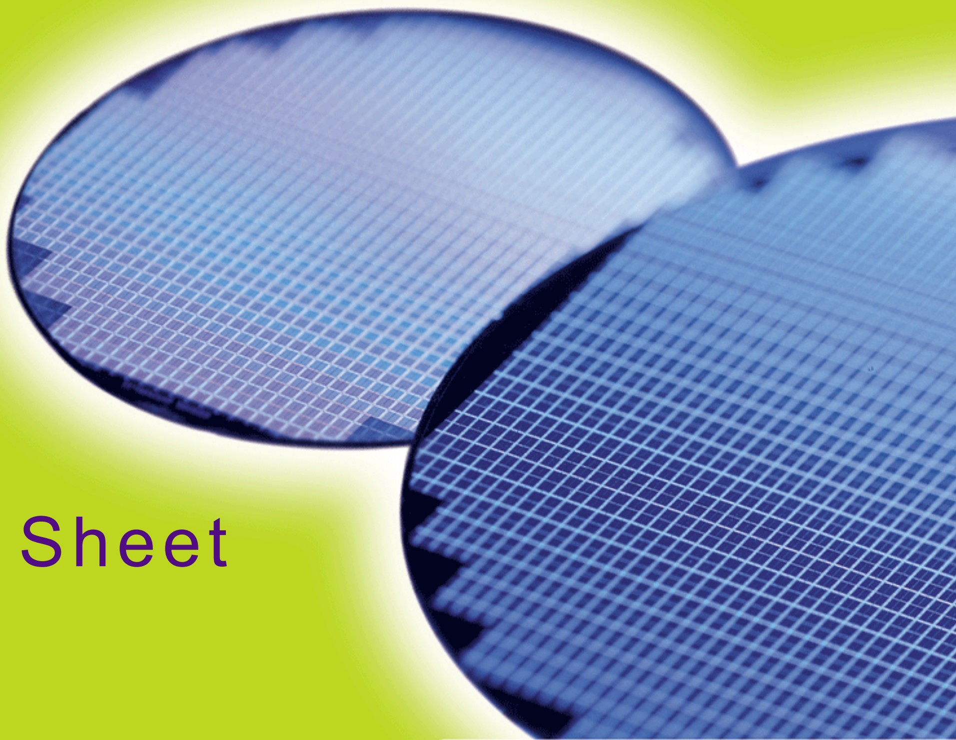
June 2007

HYB18T512161B2F–20/25

512-Mbit x16 DDR2 SDRAM
DDR2 SDRAM
RoHS compliant



Internet Data Sheet

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Page	**Subjects (major changes since last revision)**
All	Typo Changes

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1 Overview

This chapter gives an overview of the 512-Mbit Double-Data-Rate-Two SDRAM product family for graphics application and describes its main characteristics.

1.1 Features

The 512-Mbit Double-Data-Rate-Two SDRAM offers the following key features:

- 1.8 V ± 0.1V V_{DD} for [–20/–25]
- 1.8 V ± 0.1V V_{DDQ} for [–20/–25]
- DRAM organizations with 16 data in/outputs
- Double Data Rate architecture:
  – two data transfers per clock cycle
  – four internal banks for concurrent operation
- Programmable $\overline{CAS}$ Latency: 3, 4, 5, 6, 7
- Programmable Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{CK}$)
- Bi-directional, differential data strobes (DQS and $\overline{DQS}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- $\overline{DQS}$ can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted $\overline{CAS}$ by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality.
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Average Refresh Period 7.8 µs at a T_{CASE} lower than 85 °C, 3.9 µs between 85 °C and 95 °C
- Full Strength and reduced Strength (60%) Data-Output Drivers
- 2kB page size
- Packages: P-TFBGA-84
- RoHS Compliant Products[1)]

TABLE 1
Ordering Information for RoHS compliant products

Product Number	Org.	Clock (MHz)	Package
HYB18T512161B2F–20/25	×16	500/400	P-TFBGA-84

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The 512-Mb DDR2 DRAM is a high-speed Double-Data-Rate-Two CMOS DRAM device containing 536,870,912 bits and internally configured as a quad-bank DRAM. The 512-Mb device is organized as 8 Mbit × 16 I/O × 4 banks chip. These devices achieve high speed transfer rates starting at 800 Mb/sec/pin for general applications.

The device is designed to comply with all DDR2 DRAM key features:

1. posted $\overline{\text{CAS}}$ with additive latency,
2. write latency = read latency - 1,
3. normal and weak strength data-output driver,
4. Off-Chip Driver (OCD) impedance adjustment
5. On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{\text{CK}}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS-$\overline{\text{DQS}}$ pair in a source synchronous fashion.

A 15-bit address bus is used to convey row, column and bank address information in a $\overline{\text{RAS}}$-$\overline{\text{CAS}}$ multiplexing style.

An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR2 SDRAM is available in P-TFBGA package.

2 Configuration

2.1 Chip Configuration

The chip configuration of a DDR2 SDRAM is listed by function in **Table 2**. The abbreviations used in the Ball# and Buffer Type columns are explained in **Table 3** and **Table 4** respectively. The ball numbering for the FBGA package is depicted in **Figure 1**.

TABLE 2
Chip Configuration of DDR2 SDRAM

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals				
J8	CK	I	SSTL	**Clock Signal CK, Complementary Clock Signal CK** Note: *CK and $\overline{CK}$ are differential system clock inputs. All address and control inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossing of CK and $\overline{CK}$ (both direction of crossing)*
K8	$\overline{CK}$	I	SSTL	
K2	CKE	I	SSTL	**Clock Enable** Note: *CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for self-refresh entry. Input buffers excluding CKE are disabled during self-refresh. CKE is used asynchronously to detect self-refresh exit condition. Self-refresh termination itself is synchronous. After V_{REF} has become stable during power-on and initialisation sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down*
Control Signals				
K7	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
L7	$\overline{CAS}$	I	SSTL	
K3	$\overline{WE}$	I	SSTL	
L8	$\overline{CS}$	I	SSTL	**Chip Select**
Address Signals				

Ball#	Name	Ball Type	Buffer Type	Function
L2	BA0	I	SSTL	**Bank Address Bus 1:0**
L3	BA1	I	SSTL	
L1	NC	I	SSTL	
M8	A0	I	SSTL	**Address Signal 12:0, Address Signal 10/Autoprecharge**
M3	A1	I	SSTL	
M7	A2	I	SSTL	
N2	A3	I	SSTL	
N8	A4	I	SSTL	
N3	A5	I	SSTL	
N7	A6	I	SSTL	
P2	A7	I	SSTL	
P8	A8	I	SSTL	
P3	A9	I	SSTL	
M2	A10	I	SSTL	
	AP	I	SSTL	
P7	A11	I	SSTL	
R2	A12	I	SSTL	
Data Signals				
G8	DQ0	I/O	SSTL	**Data Signal 15:0** *Note: Bi-directional data bus. DQ[15:0]*
G2	DQ1	I/O	SSTL	
H7	DQ2	I/O	SSTL	
H3	DQ3	I/O	SSTL	
H1	DQ4	I/O	SSTL	
H9	DQ5	I/O	SSTL	
F1	DQ6	I/O	SSTL	
F9	DQ7	I/O	SSTL	
C8	DQ8	I/O	SSTL	
C2	DQ9	I/O	SSTL	
D7	DQ10	I/O	SSTL	
D3	DQ11	I/O	SSTL	
D1	DQ12	I/O	SSTL	
D9	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
B9	DQ15	I/O	SSTL	
Data Strobe				
B7	UDQS	I/O	SSTL	**Data Strobe Upper Byte** *Note: UDQS corresponds to the data on DQ[15:8]*
A8	$\overline{\text{UDQS}}$	I/O	SSTL	
F7	LDQS	I/O	SSTL	**Data Strobe Lower Byte** *Note: LDQS corresponds to the data on DQ[7:0]*
E8	$\overline{\text{LDQS}}$	I/O	SSTL	
Data Mask				

Ball#	Name	Ball Type	Buffer Type	Function
B3	UDM	I	SSTL	**Data Mask Upper/Lower Byte**
F3	LDM	I	SSTL	*Note: LDM and UDM are the input mask signals and control the lower or upper bytes.*
Power Supplies				
A9,C1,C3,C7,C9	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
A1	V_{DD}	PWR	–	**Power Supply**
A7,B2,B8,D2,D8	V_{SSQ}	PWR	–	**I/O Driver Power Supply**
A3,E3	V_{SS}	PWR	–	**Power Supply**
Power Supplies				
J2	V_{REF}	AI	–	**I/O Reference Voltage**
E9, G1, G3, G7, G9	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
J1	V_{DDL}	PWR	–	**Power Supply**
E1, J9, M9, R1	V_{DD}	PWR	–	**Power Supply**
E7, F2, F8, H2, H8	V_{SSQ}	PWR	–	**I/O Driver Power Supply**
J7	V_{SSDL}	PWR	–	**Power Supply**
A3, E3,J3,N1,P9	V_{SS}	PWR	–	**Power Supply**
Not Connected				
A2, E2, R3, R7, R8, L1	NC	NC	–	**Not Connected**
Other Balls				
K9	ODT	I	SSTL	**On-Die Termination Control** *Note: ODT is applied to each DQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and LDM signal. An EMRS(1) control bit enables or disables the ODT functionality.*

TABLE 3
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 4
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1
Chip Configuration, PG-TFBGA-84 (top view)

1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	$\overline{UDQS}$	V_{DDQ}
DQ14	V_{SSQ}	UDM		B		UDQS	V_{SSQ}	DQ15
V_{DDQ}	DQ9	V_{DDQ}		C		V_{DDQ}	DQ8	V_{DDQ}
DQ12	V_{SSQ}	DQ11		D		DQ10	V_{SSQ}	DQ13
V_{DD}	NC	V_{SS}		E		V_{SSQ}	$\overline{LDQS}$	V_{DDQ}
DQ6	V_{SSQ}	LDM		F		LDQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		G		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		H		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		J		VSSDL	CK	V_{DD}
	CKE	$\overline{WE}$		K		$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1		L		$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1		M		A2	A0	V_{DD}
V_{SS}	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	V_{SS}
V_{DD}	A12	NC		R		NC	NC	

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Notes

1. UDQS/$\overline{UDQS}$ is data strobe for DQ[15:8], LDQS/$\overline{LDQS}$ is data strobe for DQ[7:0]
2. LDM is the data mask signal for DQ[7:0], UDM is the data mask signal for DQ[15:8]
3. V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{DD}, V_{DDQ}, V_{SSDL}, V_{SS}, and V_{SSQ} are isolated on the device.

2.2 512 Mbit DDR2 Addressing

TABLE 5
512-Mbit DDR2 Addressing

Configuration	32-Mbit x 16	Note
Bank Address	BA[1:0]	
Number of Banks	4	
Auto-Precharge	A10 / AP	
Row Address	A[12:0]	
Column Address	A[9:0]	
Number of Column Address Bits	10	1)
Number of I/Os	16	2)
Page Size [Bytes]	2048 (2K)	3)

1) Referred to as ’colbits’
2) Referred to as ’org’
3) PageSize = $2^{colbits} \times$ org/8 [Bytes

3 Functional Description

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	PD	WR			DLL	TM	CL			BT	BL		
reg. addr		w	w			w	w	w			w	w		

TABLE 6
Mode Register Definition (BA[1:0] = 00B)

Field	Bits	Type[1]	Description
BA1	14	reg. addr.	**Bank Address [1]** 0_B **BA1** Bank Address
BA0	13		**Bank Address [0]** 0_B **BA0** Bank Address
PD	12	w	**Active Power-Down Mode Select** 0_B **PD** Fast exit 1_B **PD** Slow exit
WR	[11:9]	w	**Write Recovery**[2] *Note: All other bit combinations are illegal.* 001_B **WR** 2 010_B **WR** 3 011_B **WR** 4 100_B **WR** 5 101_B **WR** 6 110_B **WR** 7
DLL	8	w	**DLL Reset** 0_B **DLL** No 1_B **DLL** Yes
TM	7	w	**Test Mode** 0_B **TM** Normal Mode 1_B **TM** Vendor specific test mode
CL	[6:4]	w	**CAS Latency** *Note: All other bit combinations are illegal.* 010_B **CL** reserved 011_B **CL** 3 100_B **CL** 4 101_B **CL** 5 110_B **CL** 6 111_B **CL** 7

Field	Bits	Type[1]	Description
BT	3	w	**Burst Type** 0_B **BT** Sequential 1_B **BT** Interleaved
BL	[2:0]	w	**Burst Length** *Note: All other bit combinations are illegal.* 010_B **BL** 4 011_B **BL** 8

1) w = write only register bits

2) Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WR [cycles] ≥ t_{WR} (ns) / t_{CK} (ns). The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing WR_{MIN} is determined by $t_{CK.MAX}$ and WR_{MAX} is determined by $t_{CK.MIN}$.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Q_{off}	0	$\overline{DQS}$	OCD Program			R_{tt}	AL			R_{tt}	DIC	DLL
reg. addr				w	w			w	w			w	w	w

TABLE 7
Extended Mode Register Definition (BA[1:0] = 01B)

Field	Bits	Type[1]	Description
BA1	14	reg. addr.	**Bank Address [1]** 0_B **BA1** Bank Address
BA0	13		**Bank Address [0]** 1_B **BA0** Bank Address
Qoff	12	w	**Output Disable** 0_B **QOff** Output buffers enabled 1_B **QOff** Output buffers disabled
$\overline{DQS}$	10		**Complement Data Strobe (DQS Output)** 0_B **DQS** Enable 1_B **DQS** Disable
OCD Program	[9:7]		**Off-Chip Driver Calibration Program** 000_B **OCD** OCD calibration mode exit, maintain setting 001_B **OCD** Drive (1) 010_B **OCD** Drive (0) 100_B **OCD** Adjust mode 111_B **OCD** OCD calibration default

Field	Bits	Type[1]	Description
AL	[5:3]		**Additive Latency** *Note: All other bit combinations are illegal.* 000_B **AL** 0 001_B **AL** 1 010_B **AL** 2 011_B **AL** 3 100_B **AL** 4 101_B **AL** 5 110_B **AL** 6
R_{TT}	6,2		**Nominal Termination Resistance of ODT** 00_B **RTT** ∞ (ODT disabled) 01_B **RTT** 75 Ohm 10_B **RTT** 150 Ohm 11_B **RTT** 50 Ohm
DIC	1		**Off-chip Driver Impedance Control** 0_B **DIC** Full (Driver Size = 100%) 1_B **DIC** Reduced
DLL	0		**DLL Enable** 0_B **DLL** Enable 1_B **DLL** Disable

1) w = write only register bits

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0					SRF	0				PASR		

reg. addr

TABLE 8
EMRS(2) Programming Extended Mode Register Definition (BA[1:0]=10_B)

Field	Bits	Type[1]	Description
BA1	14	reg. addr.,	**Bank Address [1]** 1_B **BA1** Bank Address
BA0	13		**Bank Address [0]** 0_B **BA0** Bank Address
A	[12:8]	w	**Address Bus** 00000_B **A** Address bits
SRF	7	w	**Address Bus, High Temperature Self Refresh Rate for T_{CASE} > 85°C** 0_B **A7** disable 1_B **A7** enable [2]
A	[6:3]	w	**Address Bus** 0000_B **A** Address bits

Field	Bits	Type[1]	Description
Partial Self Refresh for 4 banks			
PASR	[2:0]	w	**Address Bus, Partial Array Self Refresh for 4 Banks**[3] 000_B **PASR0** Full Array 001_B **PASR1** Half Array (BA[1:0]=00, 01) 010_B **PASR2** Quarter Array (BA[1:0]=00) 011_B **PASR3** Not defined 100_B **PASR4** 3/4 array (BA[1:0]=01, 10, 11) 101_B **PASR5** Half array (BA[1:0]=10, 11) 110_B **PASR6** Quarter array (BA[1:0]=11) 111_B **PASR7** Not defined

1) w = write only

2) When DRAM is operated at 85°C ≤ T_{Case} ≤ 95°C the extended self refresh rate must be enabled by setting bit A7 to "1" before the self refresh mode can be entered.

3) If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified location will be lost if self refresh is entered. Data integrity will be maintained if t_{REF} conditions are met and no Self Refresh command is issued

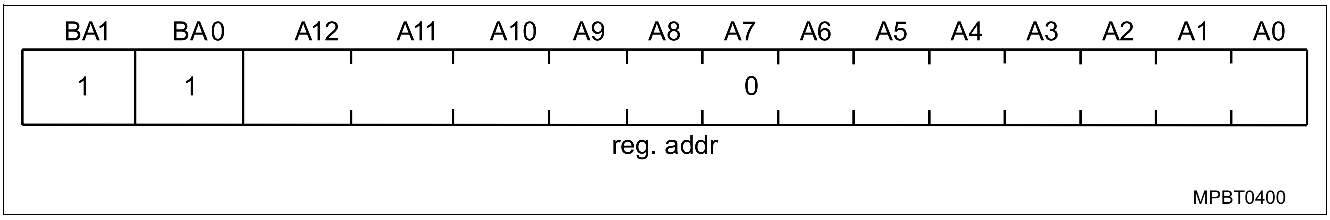


TABLE 9
EMR(3) Programming Extended Mode Register Definition (BA[1:0]=10_B)

Field	Bits	Type[1]	Description
BA1	14		**Bank Adress[1]** 1_B **BA1** Bank Address
BA0	13		**Bank Adress[0]** 1_B **BA0** Bank Address
A	[12:0]	w	**Address Bus[12:0]** 0_B **A[12:0]** Address bits

1) w = write only

TABLE 10
ODT Truth Table

Input Pin	EMRS(1) Address Bit A10	EMRS(1) Address Bit A11
DQ[7:0]	X	
DQ[15:8]	X	
LDQS	X	
$\overline{\text{LDQS}}$	0	X
UDQS	X	
$\overline{\text{UDQS}}$	0	X

Input Pin	EMRS(1) Address Bit A10	EMRS(1) Address Bit A11
LDM	X	
UDM	X	

Note: X = don’t care; 0 = bit set to low; 1 = bit set to high

TABLE 11
Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Notes

1. *PageSize and Length is a function of I/O organization:32Mb (CA[9:0]); Page Size = 2 kByte; Page Length = 1024*
2. *Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components*

4 Truth Tables

TABLE 12
Command Truth Table

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0 BA1	A[12:11]	A10	A[9:0]	Note 1)2)3)
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			4)5)
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	4)
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	4)6)
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	4)6)7)
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	4)5)
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	4)
Bank Activate	H	H	L	L	H	H	BA	Row Address			4)5)
Write	H	H	L	H	L	L	BA	Column	L	Column	4)5)8)
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	4)5)8)
Read	H	H	L	H	L	H	BA	Column	L	Column	4)5)8)
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	4)5)8)
No Operation	H	X	L	H	H	H	X	X	X	X	4)
Device Deselect	H	X	H	X	X	X	X	X	X	X	4)
Power Down Entry	H	L	H	X	X	X	X	X	X	X	4)9)
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	4)9)
			L	H	H	H					

1) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
2) “X” means “H or L (but a defined logic level)”.
3) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) All DDR2 SDRAM commands are defined by states of $\overline{\text{CS}}$, $\overline{\text{WE}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and CKE at the rising edge of the clock.
5) Bank addresses BA[1:0] determine which bank is to be operated upon. For (E)MRS BA[1:0] selects an (Extended) Mode Register.
6) V_{REF} must be maintained during Self Refresh operation.
7) Self Refresh Exit is asynchronous.
8) Burst reads or writes at BL = 4 cannot be terminated.
9) The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements

TABLE 13
Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State[1]	CKE		Command (N)[2)3)] RAS, CAS, WE, CS	Action (N)[2]	Note[4)5)]
	Previous Cycle[6] (N-1)	Current Cycle[6] (N)			
Power-Down	L	L	X	Maintain Power-Down	7)8)11)
	L	H	DESELECT or NOP	Power-Down Exit	7)9)10)11)
Self Refresh	L	L	X	Maintain Self Refresh	8)11)12)
	L	H	DESELECT or NOP	Self Refresh Exit	9)12)13)14)
Bank(s)Active	H	L	DESELECT or NOP	Active Power-Down Entry	7)9)10)11)15)
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	9)10)11)15)
	H	L	AUTOREFRESH	Self Refresh Entry	7)11)14)16)
Any State other than listed above	H	H	Refer to the Command Truth Table		17)

1) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
2) Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
3) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
4) CKE must be maintained HIGH while the device is in OCD calibration mode.
5) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
6) CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
7) The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements
8) “X” means “don’t care (including floating around V_{REF})” in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMRS(1)).
9) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
10) Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CKE} + t_{IH}$.
12) V_{REF} must be maintained during Self Refresh operation.
13) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
14) Valid commands for Self Refresh Exit are NOP and DESELCT only.
15) Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress.
16) Self Refresh mode can only be entered from the All Banks Idle state.
17) Must be a legal command as defined in the Command Truth Table.

TABLE 14
Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data; provided coincident with the corresponding data.

5 Electrical Characteristics

TABLE 15
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Unit	Notes
T_{CASE}	Operating Temperature	0 to 95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.
4) When operating this product in the 85°C to 95°C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1“. Note, when the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

5.1 Absolute Maximum Ratings

TABLE 16
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Notes
		min	max		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	2.3	V	1)
V_{DDL}	Voltage on VDDL pin relative to V_{SS}	–0.5	2.3	V	1)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	2.3	V	1)
T_J	Junction Temperature		125	°C	1)
T_{STG}	Storage Temperature	–55	150	°C	1)2)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

5.2 DC Characteristics

TABLE 17
Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)2)
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1)2)
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1)2)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	3)4)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	5)

1) HYB18T512161B2F–20/25
2) V_{DDQ} tracks with V_{DD}, V_{DDDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDDL} tied together.
3) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
4) Peak to peak ac noise on V_{REF} may not exceed ± 2% V_{REF} (dc)
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}.

TABLE 18
ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm	Rtt1(eff)	60	75	90	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2] =[1,0]; 150 Ohm	Rtt2(eff)	120	150	180	Ω	1)
Termination resistor impedance value for EMRS(1)(A6,A2)=[1,1]; 50 Ohm	Rtt3(eff)	40	50	60	Ω	1)
Deviation of V_M with respect to V_{DDQ} / 2	delta V_M	–6.00	—	+ 6.00	%	2)

1) Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IHac})$ and $I(V_{ILac})$ respectively. $Rtt(eff) = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IHac}) - I(V_{ILac}))$.
2) Measurement Definition for V_M: Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: delta $V_M = ((2 \times V_M / V_{DDQ}) - 1) \times 100\%$

TABLE 19
Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Notes
IIL	Input Leakage Current; any input 0 V < VIN < V_{DD}	–2	+2	µA	1)
IOL	Output Leakage Current; 0 V < VOUT < V_{DDQ}	–5	+5	µA	2)

1) all other pins not under test = 0 V
2) DQ’s, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$, DQS, $\overline{DQS}$ are disabled and ODT is turned off

5.3 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable $\overline{DQS}$" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}.

In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the $\overline{DQS}$ signals are internally disabled and don't care.

TABLE 20
DC & AC Logic Input Levels

Symbol	Parameter	Min.	Max.	Units
$V_{IH(dc)}$	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V
$V_{IL(dc)}$	DC input low	–0.3	V_{REF} – 0.125	V
$V_{IH(ac)}$	AC input logic high	V_{REF} + 0.250	—	V
$V_{IL(ac)}$	AC input low	—	V_{REF} – 0.250	V

TABLE 21
Single-ended AC Input Test Conditions

Symbol	Condition	Value	Unit	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1)
$V_{SWING.MAX}$	Input signal maximum peak to peak swing	1.0	V	1)
SLEW	Input signal minimum Slew Rate	1.0	V / ns	2)3)

1) Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2) The input signal minimum Slew Rate is to be maintained over the range from $V_{IH(ac).MIN}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(ac).MAX}$ for falling edges as shown in **Figure 2**
3) AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

FIGURE 2
Single-ended AC Input Test Conditions Diagram

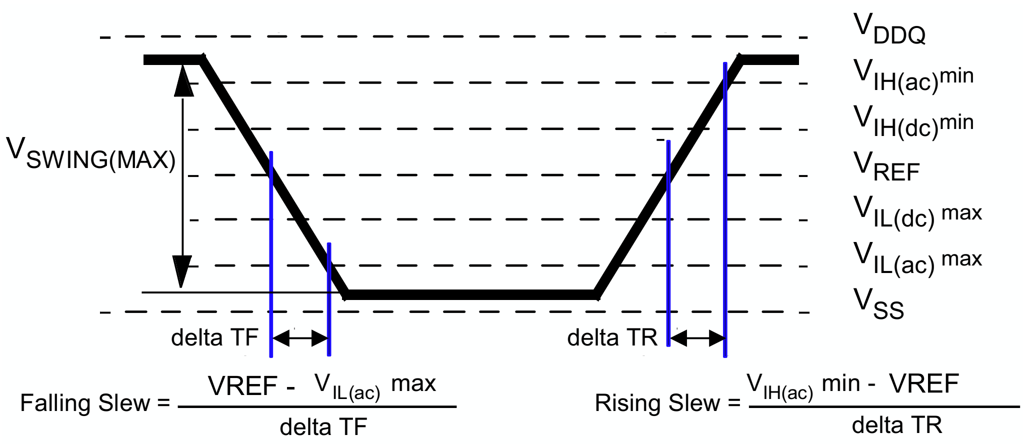
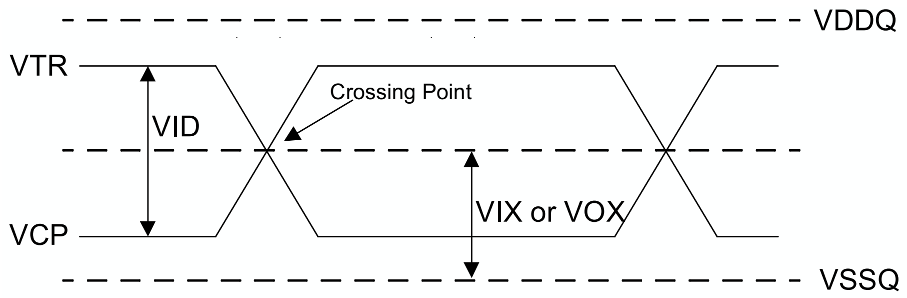


TABLE 22
Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	Min.	Max.	Unit	Notes
$V_{IN(dc)}$	DC input signal voltage	–0.3	V_{DDQ} + 0.3	—	1)
$V_{ID(dc)}$	DC differential input voltage	0.25	V_{DDQ} + 0.6	—	2)
$V_{ID(ac)}$	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	3)
$V_{IX(ac)}$	AC differential cross point input voltage	0.5 × V_{DDQ} – 0.175	0.5 × V_{DDQ} + 0.175	V	4)
$V_{OX(ac)}$	AC differential cross point output voltage	0.5 × V_{DDQ} – 0.125	0.5 × V_{DDQ} + 0.125	V	5)

1) $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$ etc.
2) $V_{ID(dc)}$ specifies the input differential voltage V_{TR}– V_{CP} required for switching. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$.
3) $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} - V_{IL(ac)}$.
4) The value of $V_{IX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ}. $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.
5) The value of $V_{OX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ}. $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

FIGURE 3
Differential DC and AC Input and Output Logic Levels Diagram



5.4 Output Buffer Characteristics

TABLE 23
Full Strength Calibrated Pull-up Driver Characteristics

Voltage (V)	Calibrated Pull-up Driver Current [mA]				
	Nominal Minimum[1)] (21 Ohms)	Nominal Low[2)](18.75 Ohms)	Nominal(18 ohms)[3)]	Nominal High[2)](17.25 Ohms)	Nominal Maximum[4)] (15 Ohms)
0.2	–9.5	–10.7	–11.4	–11.8	–13.3
0.3	–14.3	–16.0	–16.5	–17.4	–20.0
0.4	–18.3	–21.0	–21.2	–23.0	–27.0

1) The driver characteristics evaluation conditions are Nominal Minimum 95 °C (T_{CASE}). V_{DDQ} = 1.7 V, any process
2) The driver characteristics evaluation conditions are Nominal Low and Nominal High 25 °C (T_{CASE}), V_{DDQ} = 1.8 V, any process
3) The driver characteristics evaluation conditions are Nominal 25 °C (T_{CASE}), V_{DDQ} = 1.8 V, typical process
4) The driver characteristics evaluation conditions are Nominal Maximum 0 °C (T_{CASE}), V_{DDQ} = 1.9 V, any process

TABLE 24
Full Strength Calibrated Pull-down Driver Characteristics

Voltage (V)	Calibrated Pull-down Driver Current [mA]				
	Nominal Minimum[1)] (21 Ohms)	Nominal Low[2)](18.75 Ohms)	Nominal[3)](18 ohms)	Nominal High[2)](17.25 Ohms)	Nominal Maximum[4)] (15 Ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

1) The driver characteristics evaluation conditions are Nominal Minimum 95 °C (T_{CASE}). V_{DDQ} = 1.7 V, any process
2) The driver characteristics evaluation conditions are Nominal Low and Nominal High 25 °C (T_{CASE}), V_{DDQ} = 1.8V, any process
3) The driver characteristics evaluation conditions are Nominal 25 °C (T_{CASE}), V_{DDQ} = 1.8 V, typical process
4) The driver characteristics evaluation conditions are Nominal Maximum 0 °C (T_{CASE}), V_{DDQ} = 1.9 V, any process

5.5 Input / Output Capacitance

TABLE 25
Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Unit
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	1.75	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	—	0.5	pF

5.6 Overshoot and Undershoot Specification

TABLE 26
AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	–20	–25	Unit
Maximum peak amplitude allowed for overshoot area	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	V
Maximum overshoot area above V_{DD}	0.80	0.80	V.ns
Maximum undershoot area below V_{SS}	0.80	0.80	V.ns

FIGURE 4
AC Overshoot / Undershoot Diagram for Address and Control Pins

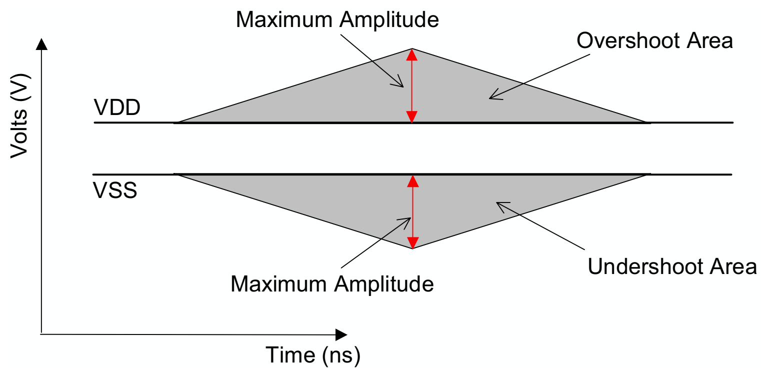
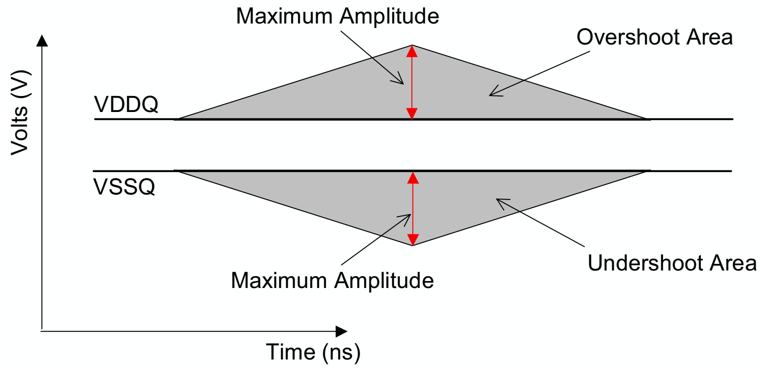


TABLE 27
AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	–20	–25	Unit
Maximum peak amplitude allowed for overshoot area	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	V
Maximum overshoot area above V_{DDQ}	0.23	0.23	V.ns
Maximum undershoot area below V_{SSQ}	0.23	0.23	V.ns

FIGURE 5
AC Overshoot / Undershoot Diagram for Clock, Data, Strobe and Mask Pins



5.7 AC Characteristics

5.7.1 Speed Grade Definitions

TABLE 28
Speed Grade Definition

Speed Grade			–20		–25		Unit	Note
Parameter		**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**		
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1)2)3)4)
	@ CL = 7	t_{CK}	2.0	8	—	—	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70k	45	70k	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the “Reference Load for Timing Measurements” according to **Chapter 7.1** only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/CK, DQS / DQS is defined in **Chapter 7.3**.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}. See **Chapter 7.1** for the reference load for timing measurements.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

5.7.2 AC Timing Parameters

List of Timing Parameters

TABLE 29
Timing Parameter by Speed Grade

Parameter	Symbol	–20		–25		Unit	Notes1) 2)3)4)5)6)
		Min.	Max.	Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	–500	+500	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	7)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	t_{DH}	145	—	250	—	ps	9)
DQ and DM input hold time (single ended data strobe)	t_{DH1}	-105	—	0	—	ps	9)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	–500	+500	ps	9)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	280	—	280	ps	10)
Write command to 1st DQS latching transition	t_{DQSS}	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}	20		125	—	ps	9)
DQ and DM input setup time (single ended data strobe)	t_{DS1}	-105		0	—	ps	9)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})	—	MIN. (t_{CL}, t_{CH})	—		11)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	—	$t_{AC.MAX}$	ps	12)
Address and control input hold time	t_{IH}	525		575	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}	400		450	—	ps	
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	12)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	12)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	

Parameter	Symbol	–20		–25		Unit	Notes[1] [2][3][4][5][6]
		Min.	Max.	Min.	Max.		
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP}–t_{QHS}$	—	$t_{HP}–t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	380	—	380	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	[13][14]
		—	3.9	—	3.9	µs	[13][15]
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	105	—	ns	[16]
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	[12]
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	[12]
Active bank A to Active bank B command period	t_{RRD}	10	—	10	—	ns	[14][17]
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	0.35 x t_{CK}	—	0.35 x t_{CK}	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	[17]
Write recovery time for write without Auto-Precharge	t_{WR}	14	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{WR}/t_{CK}		t_{CK}	[18]
Internal Write to Read command delay	t_{WTR}	7.5	—	7.5	—	ns	[19]
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	[20]
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	10 – AL	—	8 – AL	—	t_{CK}	[20]
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	200	—	t_{CK}	

1) V_{DDQ}, V_{DD} refer to **Chapter 1**.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 5** of this data sheet.
4) The CK / $\overline{\text{CK}}$ input reference level (for timing reference to CK / $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross.The DQS / $\overline{\text{DQS}}$, input reference level is the crosspoint when in differential strobe mode;The input reference level for signals other than CK/$\overline{\text{CK}}$, DQS / $\overline{\text{DQS}}$ is defined in **Chapter 5.3** of this data sheet.
5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
6) The output timing reference voltage level is V_{TT}. See **Chapter 5** for the reference load for timing measurements.
7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
9) timing is referenced to Industrial standard definition
10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
11) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

12) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
13) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
14) 0 °C ≤ T_{CASE} ≤ 85 °C
15) 85 °C < T_{CASE} ≤ 95 °C
16) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
17) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
18) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
19) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
20) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 =”1”) a slow power-down exit timing t_{XARDS} has to be satisfied.

5.7.3 ODT AC Electrical Characteristics

TABLE 30
ODT AC Electrical Characteristics and Operating Conditions for all bins

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND}.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.

6 Specifications and Conditions

TABLE 31
I_{DD} Measurement Conditions

Parameter	Symbol	Note
Operating Current - One bank Active - Precharge $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD0}	1)2)3)4)5)6)
Operating Current - One bank Active - Read - Precharge I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$, AL = 0, CL = CL(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD1}	1)2)3)4)5)6)
Precharge Power-Down Current All banks idle; CKE is LOW; $t_{CK} = t_{CK(IDD)}$;Other control and address inputs are stable; Data bus inputs are floating.	I_{DD2P}	1)2)3)4)5)6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are switching, Data bus inputs are switching.	I_{DD2N}	1)2)3)4)5)6)
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable, Data bus inputs are floating.	I_{DD2Q}	1)2)3)4)5)6)
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, CKE is LOW; Other control and address inputs are stable; Data bus inputs are floating. MRS A12 bit is set to “0” (Fast Power-down Exit).	$I_{DD3P(0)}$	1)2)3)4)5)6)
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, CKE is LOW; Other control and address inputs are stable, Data bus inputs are floating. MRS A12 bit is set to 1 (Slow Power-down Exit);	$I_{DD3P(1)}$	1)2)3)4)5)6)
Active Standby Current All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD3N}	1)2)3)4)5)6)
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX.(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching; I_{OUT} = 0 mA.	I_{DD4R}	1)2)3)4)5)6)
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD4W}	1)2)3)4)5)6)
Burst Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{RFC} = t_{RFC(IDD)}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5B}	1)2)3)4)5)6)
Distributed Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every t_{REFI} = 7.8 µs interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5D}	1)2)3)4)5)6)

Parameter	Symbol	Note
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are floating, Data bus inputs are floating.	I_{DD6}	1)2)3)4)5)6)
Operating Bank Interleave Read Current 1. All banks interleaving reads, I_{OUT} = 0 mA; BL = 4, CL = $CL_{(IDD)}$, AL = $t_{RCD(IDD)}$ -1 × $t_{CK(IDD)}$; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RRD} = $t_{RRD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address bus inputs are stable during deselects; Data bus is switching.	I_{DD7}	1)2)3)4)5)6)7)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized.
3) I_{DD} parameter are specified with ODT disabled.
4) Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
5) Definitions for I_{DD}: see **Table 32**
6) Timing parameter minimum and maximum values for I_{DD} current measurements are defined in chapter 7..
7) A = Activate, RA = Read with Auto-Precharge, D=DESELECT

TABLE 32
Definition for I_{DD}

Parameter	Description
LOW	defined as $V_{IN} \leq V_{IL(ac).MAX}$
HIGH	defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	defined as inputs are stable at a HIGH or LOW level
FLOATING	defined as inputs are $V_{REF} = V_{DDQ} / 2$
SWITCHING	defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or strobes

TABLE 33
I_{DD} Specification

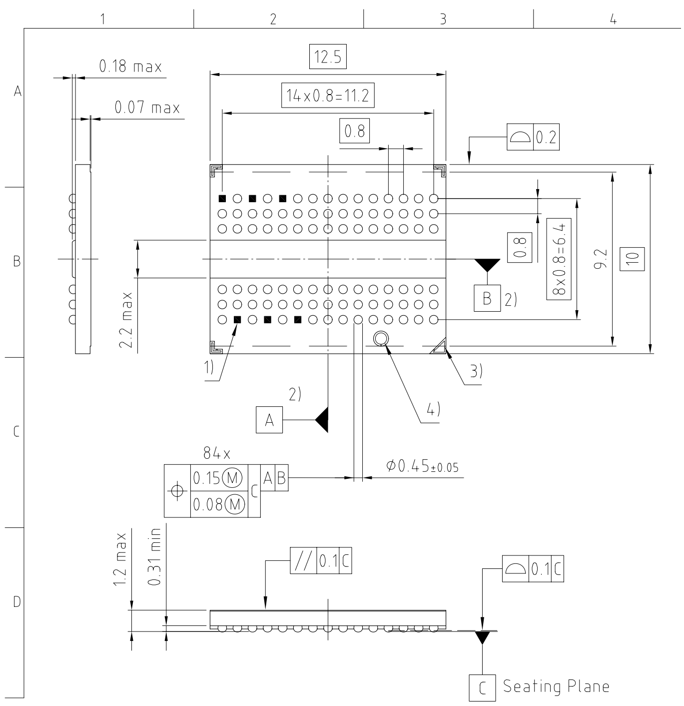
Speed Grade	–20	–25	Unit	Note
Symbol	typ.	typ.		
I_{DD0}	84	80	mA	
I_{DD1}	93	90	mA	
I_{DD2P}	4	4	mA	
I_{DD2N}	42	37	mA	
I_{DD2Q}	38	34	mA	
$I_{DD3P(0)}$	26	22	mA	1)
$I_{DD3P(1)}$	7	7	mA	2)
I_{DD3N}	47	41	mA	
I_{DD4R}	203	173	mA	
I_{DD4W}	192	162	mA	
I_{DD5B}	121	117	mA	
I_{DD5D}	5	5	mA	3)
I_{DD6}	4	4	mA	3)
I_{DD7}	206	203	mA	

1) MRS(12)=0
2) MRS(12)=1
3) $0 \le T_{CASE} \le 85°C$

7 Package

7.1 Package Dimension

FIGURE 6
Package Outline P-TFBGA-84 (top view)



4) Bad Unit Marking (BUM)
3) package orientation mark A1
2) middle of packages edges
1) dummy pads without ball ■

7.2 Package Thermal Characteristics

TABLE 34
Package thermal characteristics

JESD51	Theta_jA[1]						Theta_jC[2]
Industrial standard Board	1s0p			2s0p			
Air Flow	0 m/s	1 m/s	3 m/s	0 m/s	1 m/s	3 m/s	
Rth[K/W]	69	53	47	41	35	33	5

1) Junction to Ambient thermal resistance. The value has been obtained by simulation using the conditions stated in the Industrial standard JESD-51 standard.

2) Junction to Case thermal resistance. The value has been obtained by simulation.

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