A.HE83R540 Introduction

HE83R540 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd.

Users can chose any one of combination among 【1024 dots LCD Driver + 16 Bit I/O Port】…【896 dots LCD Driver + 24 Bit I/O Port】etc. The built-in OP comparator can be used with (light、voice、temperature、humility) sensor and used as battery low detection. The 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The 512K ROM Size can be used in the storage of speech、graphic、text etc.. . It can be applicable to the medium systems such as Small-Scale Dictionary, Data Bank, Educational Toy, Digital Voice Recording System etc. It also can be connected to SRAM or Flash RAM for recording function.

The instruction set of HE83R540 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B.HE83R540 Features

- Operation Voltage： 2.4V – 5.5V
- System Clock： DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Internal ROM： 512K Bytes
- Internal RAM： 4K Bytes
- Dual Clock System ： Normal (Fast) clock： 32.768K ~ 8MHz
  Slow clock： 32.768KHz
- Operation Mode： DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- With WDT (WATCH DOG TIMER) to prevent deadlock condition.
- 16~24 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin. 8 of them are shared with LCD segment pins.
- One built-in OP comparator.
- 1024~896 dots LCD driver (B TYPE selectable). (No LCD contrast control function)
- Build in LCD Voltage Regulator.
- One 7-bit current-type DAC output.
- PWM device.
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timers and one Time-Base timer.
- Instruction set： 32 instructions, 4 addressing mode. 12-bit DATA POINTER for RAM and 18-bit TABLE POINTER for ROM.

C. Internal Block

Please always take in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC didn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
◎	◎	◎	64KB	448KB	19-bit	◎	4KB	4-bit	8-bit	16~24	—	◎	T1,T2,TB

VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
◎	◎	◎	◎	1024~896	16*64	1/5	◎	—	—	—	—	—	—

D. Pin Description

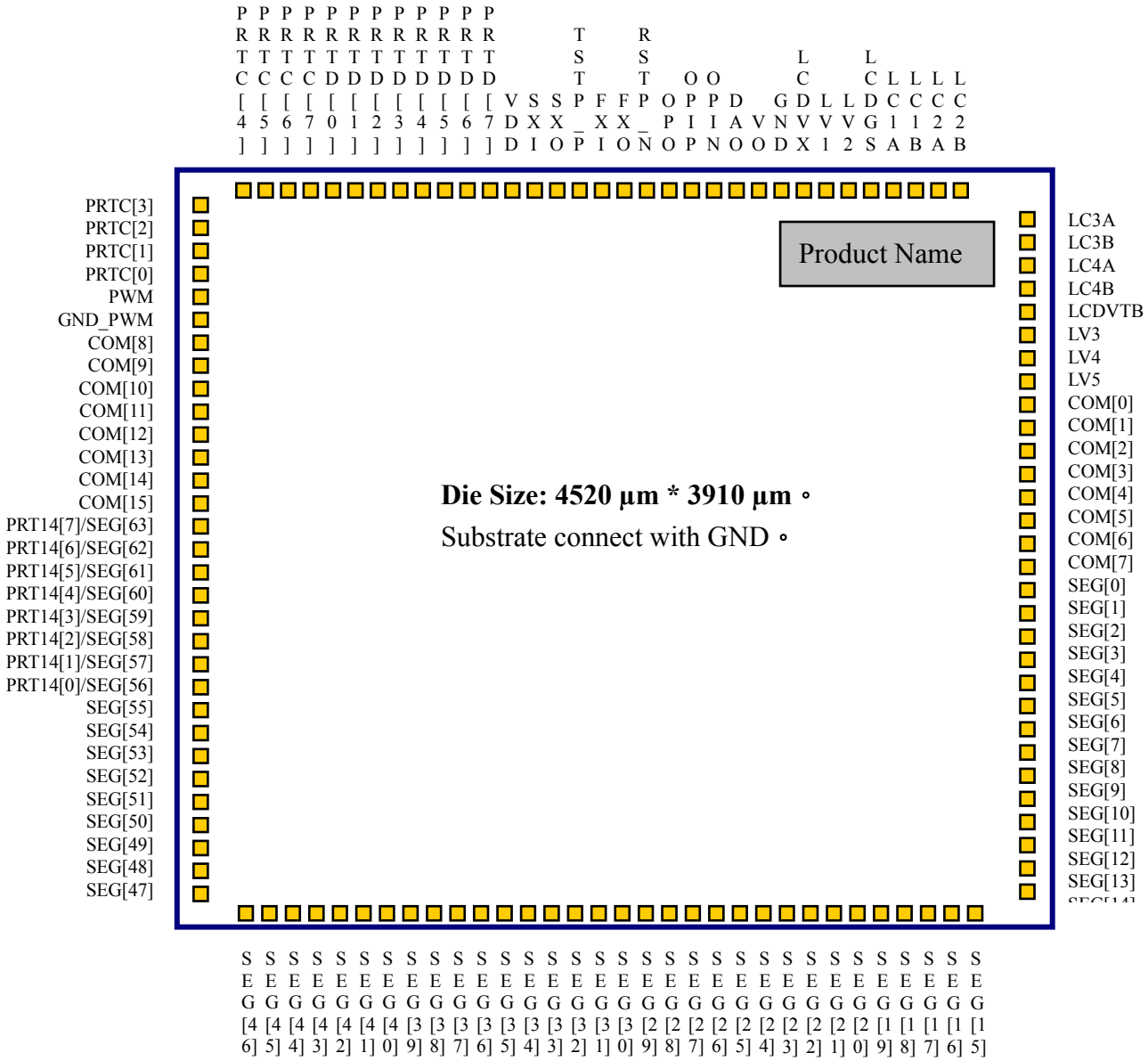
Pin#	Pin name	I/O	Function	Description
111, 110	**FXI, FXO**	B, O	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting： MO_FCK/SCKN = 00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE = 0：Internal fast osc. = 1：External fast osc. MO_FXTAL = 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL = 0：RC for 32768 Hz clock = 1：X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
114, 113	**SXI, SXO**	I, O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	
109	**RSTP_N**	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer： MO_WDTE=0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
112	**TSTP_P**	I	Test Pin	Please bond this pin and add a test point on PCB for debugging. But for improving ESD, please connect this pin with zero Ohm resistor to GND.
124..127, 1..4	**PRTC[7:0]**	B	8-pin bi-directional I/O port.	Mask options： MO_CPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
116.. 123	**PRTD[7:0]**	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask options： MO_DPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as

Pin#	Pin name	I/O	Function	Description
				input (No tri-state structure).
15..22	**PRT14[7:0]/ SEG[63:56]**	B/ O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO14[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_14PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be “1” before reading whenever use them as input (No tri-state structure).
14..7 79..86	**COM[15:0]**	O	LCD COMmon Output	LCD Data filled from F0H, please refer the LCD RAM map.
23.. 78	**SEG[55:0]**	O	LCD SEGment Output	
101	**L V1**	B	LCD Bias Voltage 1	LV5> LV4> LV3> LV2> LV1。 Adjust Resistor between LCDGS and LV2 to set LV5 for LCD glass. The formula is LV5 = 2.5*LV2。(Bias=1/5) Suggest that LV2=2.0V, so LV5=5.0V.
100	**L V2**	B	LCD Bias Voltage 2	
89	**L V3**	B	LCD Bias Voltage 3	
88	**L V4**	B	LCD Bias Voltage 4	
87	**L V5**	B	LCD Bias Voltage 5	
99	**LCDGS**	B	LCD Gain Setting Pin	~300K between LCDGS and LV2 ➔ LV2≒2.0 Volt
90	**LCDVTB**	B	Charge Pump Capacitor Pin	Larger voltage stair than LCxA, LCxB stair
102	**LCDVX**	B	Charge Pump Capacitor Pin	Smaller voltage stair than LCxA, LCxB stair
91	**LC4B**	B	Charge Pump Capacitor Pin	Different LCD Bias must be matching its Capacitor Configuration relatively. This IC is with all pins for type-IV LCD Driver. Some of charge pump pins was not using since the bias of this IC was fixed at 1/5.
92	**LC4A**	B	Charge Pump Capacitor Pin	
93	**LC3B**	B	Charge Pump Capacitor Pin	
94	**LC3A**	B	Charge Pump Capacitor Pin	
95	**LC2B**	B	Charge Pump Capacitor Pin	
96	**LC2A**	B	Charge Pump Capacitor Pin	
97	**LC1B**	B	Charge Pump Capacitor Pin	
98	**LC1A**	B	Charge Pump Capacitor Pin	
5	**PWM**	O	The PWM output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
104	**VO**	O	D/A output.	Bit 1 of VOC = ‘1’ , Turn on DA
105	**DAO**	O	DAC Voice Output	Set the bit1(DA=1) of VOC register to turn on DAC with VO output.
106	**OPIN**	I	OPAMP negative input pin.	Built-in OP comparator. Set Bit 0 of VOC = ‘1’ , Turn on OP
107	**OPIP**	I	OPAMP positive input pin.	
108	**OPO**	O	OPAMP output pin.	
115	**VDD**	P	Positive Power Input	Adding 0.1 µF capacitor as by-pass capacitor on power pins is necessary.(within 1 cm distance)
103	**GND**	P	Power Ground Input	
6	**GND_PWM**	P	Dedicated PWM Ground	

E.LCD RAM Map

Page 0	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]
COM0	80H	90H	A0H	B0H	C0H	D0H	E0H	F0H
COM1	81H	91H	A1H	B1H	C1H	D1H	E1H	F1H
COM2	82H	92H	A2H	B2H	C2H	D2H	E2H	F2H
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
COM13	8DH	9DH	ADH	BDH	CDH	DDH	EDH	FDH
COM14	8EH	9EH	AEH	BEH	CEH	DEH	EEH	FEH
COM15	8FH	9FH	AFH	BFH	CFH	DFH	EFH	FFH

F. Pin Diagram



G. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRTC[3]	-2190.00	1839.70	65	SEG[13]	2190.00	-1597.80
2	PRTC[2]	-2190.00	1724.70	66	SEG[12]	2190.00	-1482.80
3	PRTC[1]	-2190.00	1609.70	67	SEG[11]	2190.00	-1367.80
4	PRTC[0]	-2190.00	1494.70	68	SEG[10]	2190.00	-1252.80
5	PWM	-2190.00	1379.70	69	SEG[9]	2190.00	-1137.80
6	GND_PWM	-2190.00	1264.70	70	SEG[8]	2190.00	-1022.80
7	COM[8]	-2190.00	1131.40	71	SEG[7]	2190.00	-907.80
8	COM[9]	-2190.00	1016.90	72	SEG[6]	2190.00	-792.80
9	COM[10]	-2190.00	901.90	73	SEG[5]	2190.00	-593.60
10	COM[11]	-2190.00	786.90	74	SEG[4]	2190.00	-478.60
11	COM[12]	-2190.00	671.90	75	SEG[3]	2190.00	-363.60
12	COM[13]	-2190.00	556.90	76	SEG[2]	2190.00	-248.60
13	COM[14]	-2190.00	441.90	77	SEG[1]	2190.00	-133.60
14	COM[15]	-2190.00	326.90	78	SEG[0]	2190.00	-18.60
15	PRT14[7]	-2190.00	211.40	79	COM[7]	2190.00	96.40
16	PRT14[6]	-2190.00	96.40	80	COM[6]	2190.00	211.40
17	PRT14[5]	-2190.00	-18.60	81	COM[5]	2190.00	326.40
18	PRT14[4]	-2190.00	-133.60	82	COM[4]	2190.00	441.40
19	PRT14[3]	-2190.00	-248.60	83	COM[3]	2190.00	556.40
20	PRT14[2]	-2190.00	-363.60	84	COM[2]	2190.00	671.40
21	PRT14[1]	-2190.00	-478.60	85	COM[1]	2190.00	786.40
22	PRT14[0]	-2190.00	-593.60	86	COM[0]	2190.00	901.40
23	SEG[55]	-2190.00	-792.80	87	LV5	2190.00	1023.00
24	SEG[54]	-2190.00	-907.80	88	LV4	2190.00	1138.00
25	SEG[53]	-2190.00	-1022.80	89	LV3	2190.00	1253.00
26	SEG[52]	-2190.00	-1137.80	90	LCDVTB	2190.00	1368.00
27	SEG[51]	-2190.00	-1252.80	91	LC4B	2190.00	1483.00
28	SEG[50]	-2190.00	-1367.80	92	LC4A	2190.00	1598.00
29	SEG[49]	-2190.00	-1482.80	93	LC3B	2190.00	1713.00
30	SEG[48]	-2190.00	-1597.80	94	LC3A	2190.00	1828.00
31	SEG[47]	-2190.00	-1841.60	95	LC2B	1871.05	1885.00
32	SEG[46]	-1829.60	-1885.00	96	LC2A	1756.05	1885.00
33	SEG[45]	-1714.60	-1885.00	97	LC1B	1641.05	1885.00
34	SEG[44]	-1599.60	-1885.00	98	LC1A	1526.05	1885.00
35	SEG[43]	-1484.60	-1885.00	99	LCDGS	1411.05	1885.00

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
36	SEG[42]	-1369.60	-1885.00	100	LV2	1296.05	1885.00
37	SEG[41]	-1254.60	-1885.00	101	LV1	1181.05	1885.00
38	SEG[40]	-1139.60	-1885.00	102	LCDVX	1066.05	1885.00
39	SEG[39]	-1024.60	-1885.00	103	GND	949.60	1885.00
40	SEG[38]	-909.60	-1885.00	104	VO	834.60	1885.00
41	SEG[37]	-794.60	-1885.00	105	DAO	719.60	1885.00
42	SEG[36]	-679.60	-1885.00	106	OPIN	604.60	1885.00
43	SEG[35]	-564.60	-1885.00	107	OPIP	489.60	1885.00
44	SEG[34]	-449.60	-1885.00	108	OPO	374.60	1885.00
45	SEG[33]	-334.60	-1885.00	109	RSTP_N	259.60	1885.00
46	SEG[32]	-219.60	-1885.00	110	FXO	144.60	1885.00
47	SEG[31]	-104.60	-1885.00	111	FXI	29.60	1885.00
48	SEG[30]	104.60	-1885.00	112	TSTP_P	-85.40	1885.00
49	SEG[29]	219.60	-1885.00	113	SXO	-200.40	1885.00
50	SEG[28]	334.60	-1885.00	114	SXI	-315.40	1885.00
51	SEG[27]	449.60	-1885.00	115	VDD	-430.40	1885.00
52	SEG[26]	564.60	-1885.00	116	PRTD[7]	-545.40	1885.00
53	SEG[25]	679.60	-1885.00	117	PRTD[6]	-660.40	1885.00
54	SEG[24]	794.60	-1885.00	118	PRTD[5]	-859.60	1885.00
55	SEG[23]	909.60	-1885.00	119	PRTD[4]	-974.60	1885.00
56	SEG[22]	1024.60	-1885.00	120	PRTD[3]	-1089.60	1885.00
57	SEG[21]	1139.60	-1885.00	121	PRTD[2]	-1204.60	1885.00
58	SEG[20]	1254.60	-1885.00	122	PRTD[1]	-1319.60	1885.00
59	SEG[19]	1369.60	-1885.00	123	PRTD[0]	-1434.60	1885.00
60	SEG[18]	1484.60	-1885.00	124	PRTC[7]	-1549.60	1885.00
61	SEG[17]	1599.60	-1885.00	125	PRTC[6]	-1664.60	1885.00
62	SEG[16]	1714.60	-1885.00	126	PRTC[5]	-1779.60	1885.00
63	SEG[15]	1829.60	-1885.00	127	PRTC[4]	-1894.60	1885.00
64	SEG[14]	2190.00	-1841.60				

H. DC/AC Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Recommended Operating Conditions

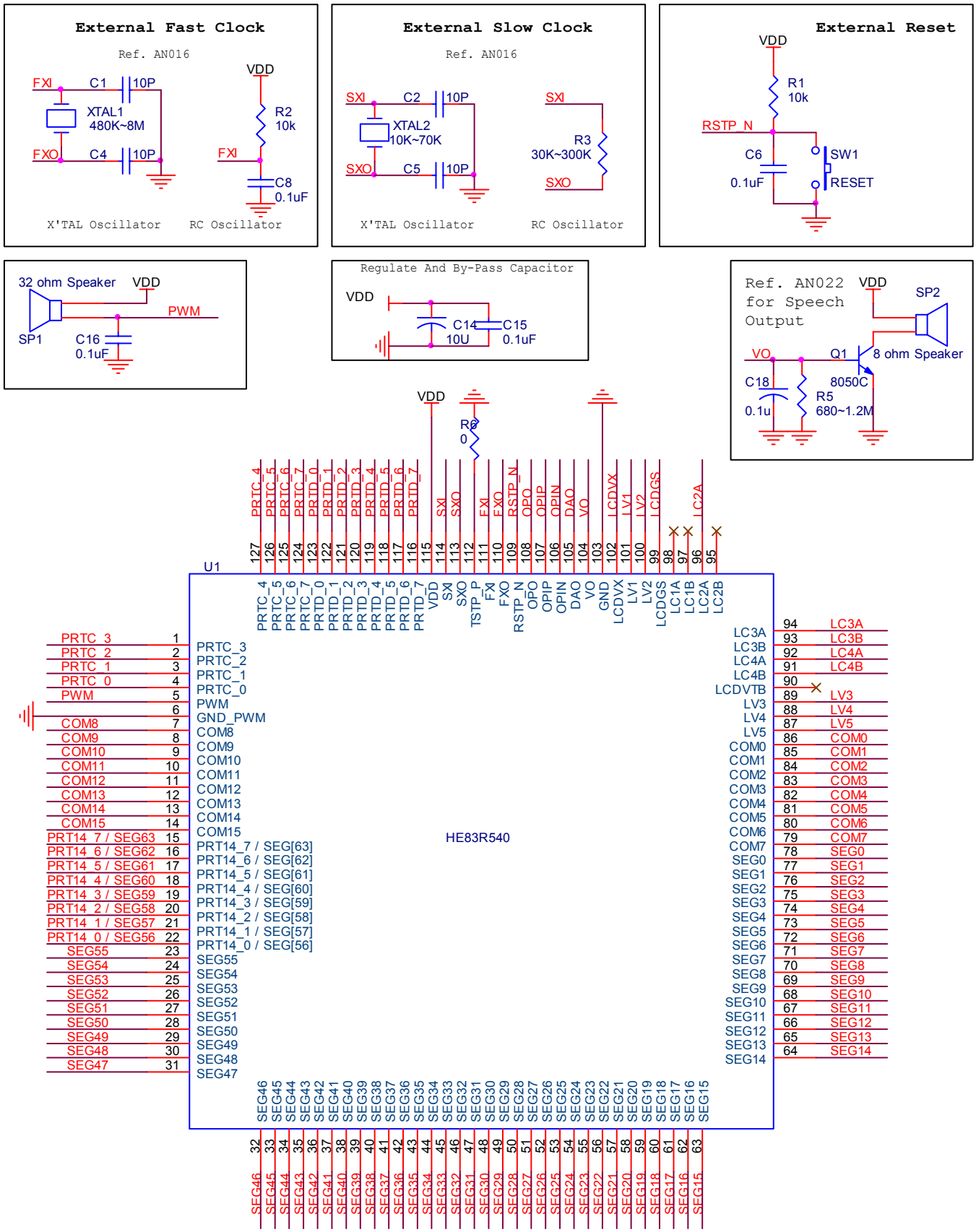
Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Testing Condition : TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		10	20	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		6	10	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable		90	100	μA
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oHPWM}	PWM Output Drive Current	PWMP, PWMN*2	V_{DD}=3V; V_{oh}=2V	12	15		mA
I_{oLPWM}	PWM Output Sink Current	PWMP, PWMN*2	V_{DD}=3V; V_{oL}=1V	33	40		mA
I_{oVO}	DAC Output Current	VO, DAO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current.
(I_{oHPWM}、I_{oLPWM} * N; N=0,1,2,3,4,5)

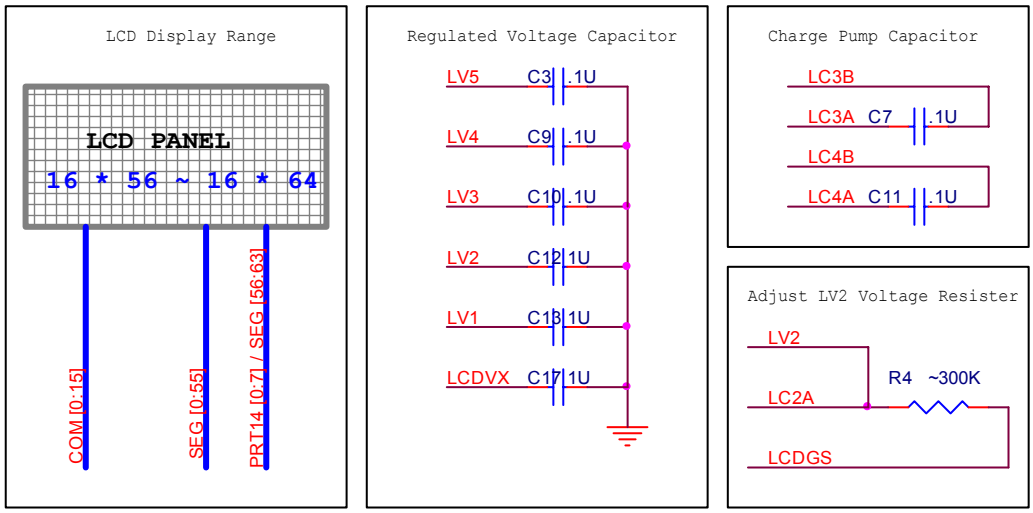
I. Application Circuit



4G LCD Charge Pump Circuit,1/5 Bias,1/16 Duty Configulation

LV5 Voltage Must < 9.0 V , Else IC will be burned down

Let LC1A,LC1B,LC2B,LCDVTB pin folating

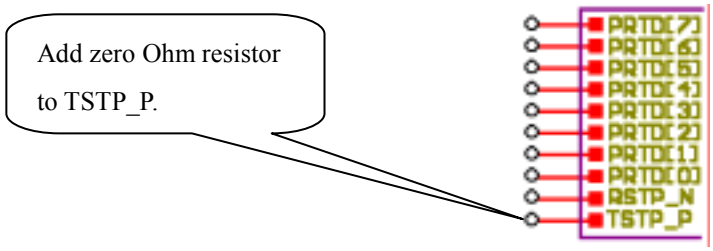


NOTE : Use Resister adjust LV2 voltage must let VDD >= LV2 + 0.4V , Else LCD charge pump will work un-well . And the LV5 voltage = LV2 *5 /2

For more detail information, please refer the new version of AN025 for this Type-IV LCD Driver.

J. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.
2. LCD driving circuit must be turn off before IC goes into sleep mode.
3. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Please connect TSTP_P pin with zero ohm resistor(or copper wire which can be cut on PCB) normally for good ESD result. KB can pull low the TSTP_P pin by remove the zero ohm resistor . The following figure is an example (Testing point with through hole).



4. LV5 must small than 9.0 Volt. Otherwise IC may breakdown.

K. Updated Record

Version	Date	Section	Original Content	New Content
V1.31	Jul 2, 2002	I		Modify Application Circuit