SiI 9002
HDMI Transmitter PHY

Applications

- DVD Player/Recorders
- Personal Video Recorders
- Set-Top Boxes
- Game Consoles
- Camcorders
- Digital Still Cameras

The SiI 9002 discrete HDMI transmitter PHY is designed to work exclusively with Silicon Image's transmitter IP that is integrated by MPEG system-on-a-chip (SoC) silicon manufacturers. The high-performance SiI 9002 is HDMI 1.2 compliant PHY that uses Silicon Image's PanelLink® Digital technology to support a range of video resolutions all the way up to 1080p. The SiI 9002 can support displays with resolutions ranging from SDTV to HDTV — all via a single-link interface.

The SiI 9002 works directly with highly integrated SoC solutions, enabling Silicon Image partners to integrate Silicon Image HDMI Digital Transmitter Logic. The SiI 9002's innovative design eases board design requirements since it is designed to accommodate high-speed parallel interfaces that reduce pin count to a bare minimum. It interfaces with the SoC via a 12-bit DMO interface that samples incoming data at the rate of one half-pixel per clock edge.

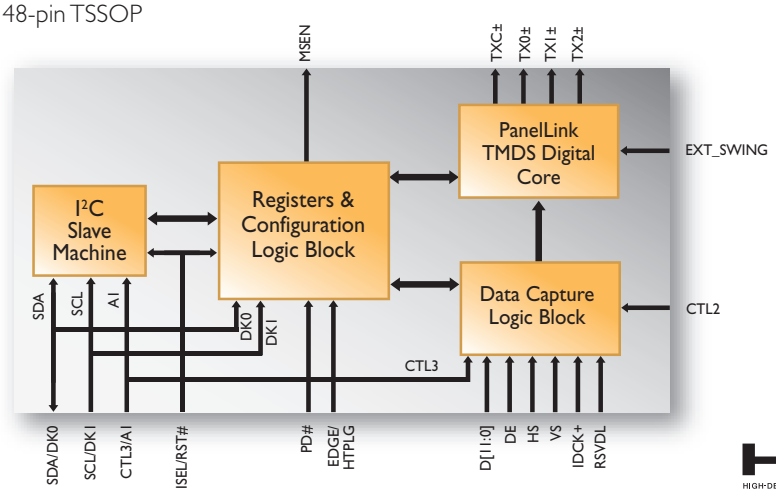
With the SiI 9002 HDMI transmitter digital IP integrated into the SoC, manufacturers are provided a low-cost, low-risk solution that enables rapid implementation of HDMI into DVD players, DVD recorders, set-top boxes and mobile devices. The SiI 9002's PanelLink Digital technology simplifies high-speed mixed-signal design by resolving many of the system-level challenges. Providing shorter design cycles and faster testing and compliance to specifications, the SiI 9002 equips system designers with a digital interface solution that enables faster time-to-market and lower overall cost.

Key Features

- HDMI 1.2, HDCP 1.1 and DVI 1.0 compliant PHY with HDMI Digital Transmitter IP
- Supports 480p/720p/1080i/1080p (60Hz) & 576p/720p/1080i/1080p (50Hz)
- 25MHz – 165MHz input/output clocks
- 12-bit HDMI digital logic output interface integrated into MPEG SoC
- 12-bit dual edge 3.3V input for low power core operation and power-down mode
- Strap pins for hardware device configuration
- Optional I²C slave programming interface and de-skewing
- 3.0 – 3.6V low-voltage interface range
- Monitor detection support through hot plug and receiver detection

Package

- 48-pin TSSOP



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HDMI Transmitter PHY Features

HDMI Data Input

- 12-bit bus using a dual-edge clock
- Selectable primary edge for input data using the edge bit
- De-skewing option to adjust data setup and hold time
- Configurable by pin settings or programmable through I²C Interface

PanelLink TMDS Digital Core

- Video information encoded onto three TMDS differential data lines
- Adjustable TMDS low-voltage swing amplitude for long cable support
- 1.65 Gb/s per data channel

Optional I²C Interface

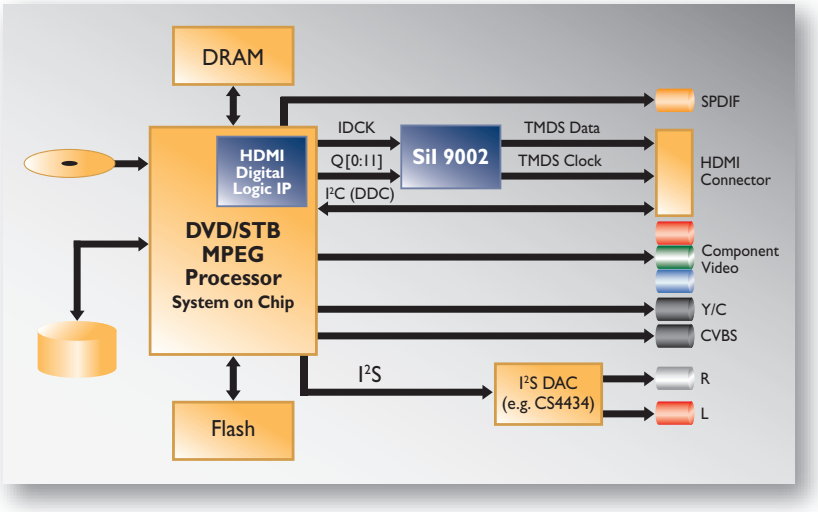
- Support I²C mode slave interface
- Running at 50KHz for host communication
- Data Latched in 12-bit mode

Hot Plug Detection Mode

- A connected display is automatically detected using the hot plug signal for reliable TV reconnection

Dual Zone PLL

- Dual-zone PLL changes its operational parameters depending on the frequency zone selected
- Operating zone optimization contributes to robust operation over long cables



Reference design supplied by MPEG silicon manufacturer, in partnership with Silicon Image

Application Block Diagram:
Example System with SiI 9002

Power Management

- 3.3 V core provides low-power operation
- Low-power standby mode

Starter Kits

Reference designs for SiI 9002 with integrated digital Transmitter IP will be provided by Silicon Image's licensed SoC partners. Please visit **www.siliconimage.com** for partner information.

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