FEMTOCLOCKS™ VCXO BASED WCDMA CLOCK GENERATOR/JITTER ATTENUATOR

ICS843002I-72

General Description

The ICS843002I-72 is a member of the HiperClockS™ family of high performance clock solutions from IDT. The ICS843002I-72 is a PLL based synchronous clock generator that is optimized for WCDMA channel card applications where jitter attenuation and frequency translation is needed. The device contains two internal PLL stages that are cascaded in series. The first PLL stage uses a VCXO which is optimized to provide reference clock jitter attenuation and to be jitter tolerant, and to provide a stable reference clock for the second PLL stage. The second PLL stage provides additional frequency multiplication (x32), and it maintains low output jitter by using a low phase noise FemtoClock™ VCO. The device performance and the PLL multiplication ratios are optimized to support WCDMA applications. The VCXO requires the use of an external, inexpensive pullable crystal. VCXO PLL uses external passive loop filter components which are used to optimize the PLL loop bandwidth and damping characteristics for the given application.

The ICS843002I-72 can accept a single-ended input. LOCK_DT reports the lock status of VCXO PLL loop. If the reference clock input is lost, it will set LOCK_DT to logic LOW.

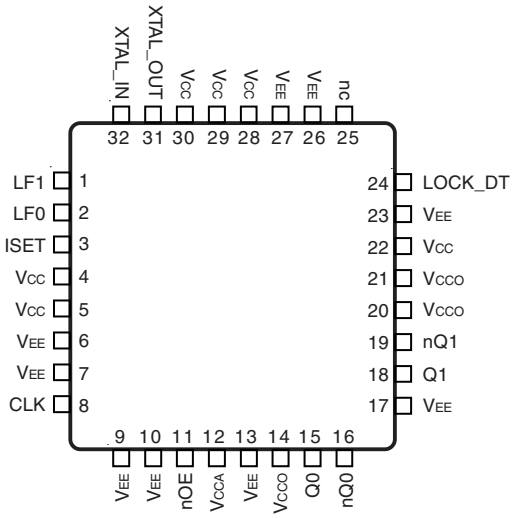
Typical ICS843002I-72 configuration in WCDMA Systems:

- 19.2MHz pullable crystal
- Input Reference clock frequency: 3.84MHz
- Output clock frequency: 122.88MHz

Features

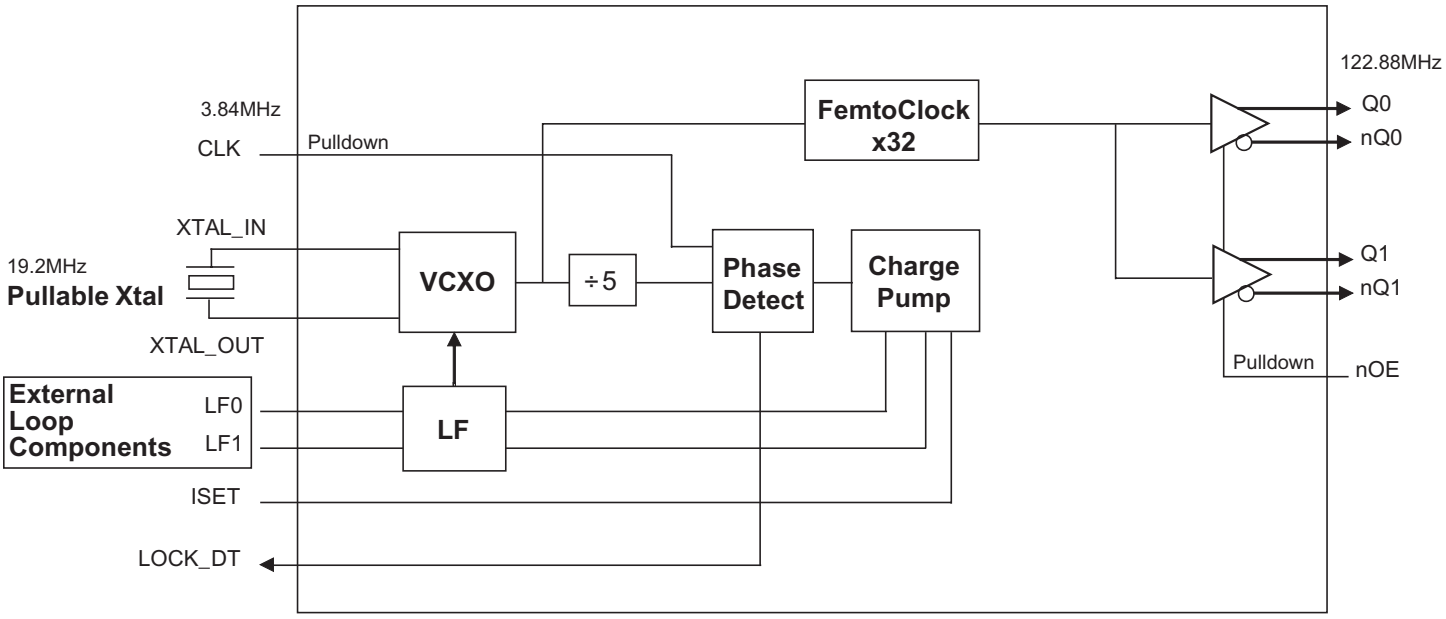
- Two differential LVPECL outputs
- CLK input accepts the following input levels: LVCMOS or LVTTL levels
- Output frequency: 122.88MHz (typical)
- FemtoClock VCO frequency range: 490MHz - 680MHz
- RMS phase jitter @ 122.88MHz, using a 19.2MHz crystal (1.875MHz to 10MHz): 0.49ps (typical)
- Deterministic jitter: 30fs (typical)
- Random jitter, RMS: 2.2ps (typical)
- Full 3.3V or mixed 3.3V core/2.5V output supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



ICS843002I-72
32-Lead VFQFN
5mm x 5mm x 0.925 package body
K Package
Top View

BLOCK DIAGRAM



NOTE 1: 19.2MHz pullable crystal shown is typical for WCDMA device applications.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 5, 22, 28, 29, 30	V_{CC}	Power		Core power supply pins.
6, 7, 9, 10, 13, 17, 23, 26, 27	V_{EE}	Power		Negative supply pins.
8	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
11	nOE	Input	Pulldown	Output enable pin. When LOW, output is enabled. LVCMOS/LVTTL interface levels. See Table 3.
12	V_{CCA}	Power		Analog supply pin.
14, 20, 21	V_{CCO}	Power		Output power supply pin.
15, 16	Q0, nQ0	Output		Differential clock output pair. LVPECL interface levels.
18, 19	Q1, nQ1	Output		Differential clock output pair. LVPECL interface levels.
24	LOCK_DT	Output		Lock detect. Logic HIGH when VCXO PLL loop is locked.
25	nc	Unused		No connect.
31, 32	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ

TABLE 3. INPUT REFERENCE SELECTION FUNCTION TABLE

Inputs	Outputs
nOE	**Q0/nQ0, Q1/nQ1**
0	Enabled
1	Hi-Z

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V±5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.13	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				140	mA
I_{CCA}	Analog Supply Current				13	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = 3.3V±5\%$, $V_{CCO} = 2.5V±5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.13	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				140	mA
I_{CCA}	Analog Supply Current				13	mA

Table 4C. LVCMOS / LVTTL DC Characteristics, $V_{CC} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ or 2.5V±5%, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK, nOE	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	InputLow Current	CLK, nOE	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V±5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO} - 2V. See "Parameter Measurement Information" section, "Output Load Test Circuit" diagrams.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO} - 2V. See "Parameter Measurement Information" section, "Output Load Test Circuit" diagrams.

TABLE 5A. AC CHARACTERISTICS, V_{CC} = V_{CCO} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			122.88		MHz
*t*jit(ø)	RMS Phase Jitter, (Random); NOTE 1	122.88MHz, Integration range: 1.875MHz - 10MHz		0.49		ps
t_{DJ}	Deterministic Jitter; NOTE 2			30		fs
t_{RJ}	Random Jitter, RMS; NOTE 2			2.2		ps
*t*sk(o)	Output Skew; NOTE 3, 4				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		550	ps
odc	Output Duty Cycle		49		51	%

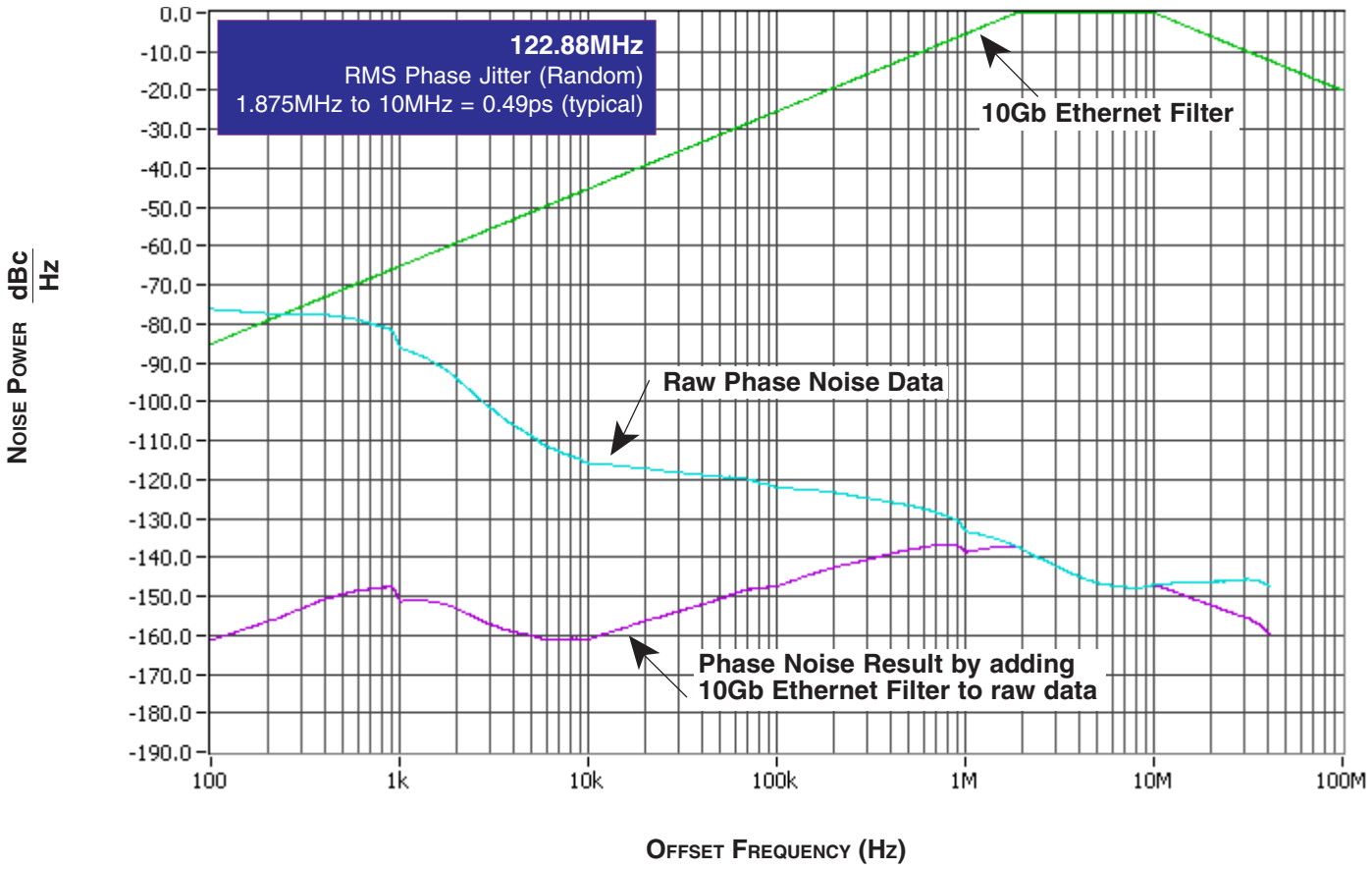
See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Measured using Wavecrest SIA-3000.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{CCO} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

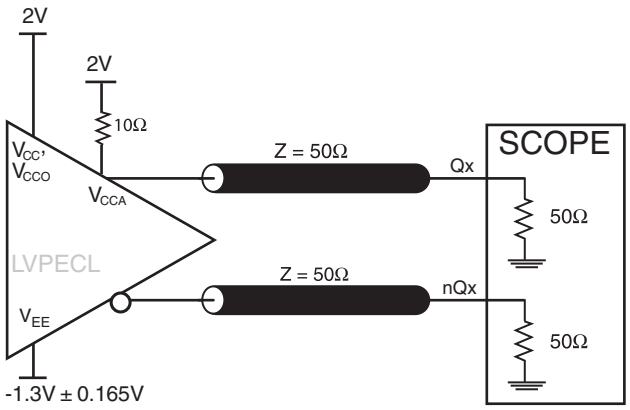
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			122.88		MHz
*t*jit(ø)	RMS Phase Jitter, (Random); NOTE 1	122.88MHz, Integration range: 1.875MHz - 10MHz		0.49		ps
t_{DJ}	Deterministic Jitter; NOTE 2			30		fs
t_{RJ}	Random Jitter, RMS; NOTE 2			2.2		ps
*t*sk(o)	Output Skew; NOTE 3, 4				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		550	ps
odc	Output Duty Cycle		49		51	%

See Parameter Measurement Information section.
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Measured using Wavecrest SIA-3000.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

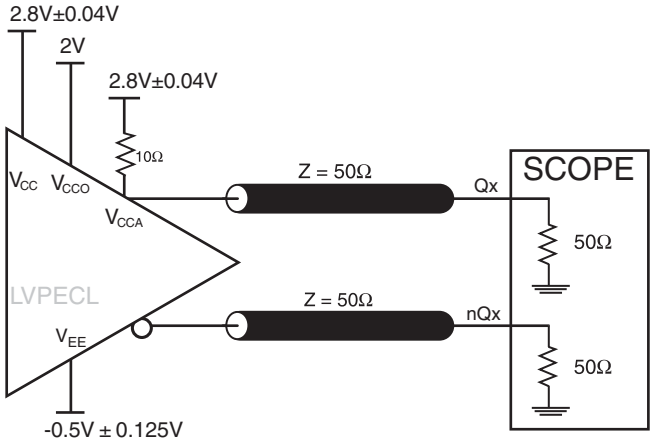
TYPICAL PHASE NOISE AT 122.88MHZ @ 3.3V/3.3V



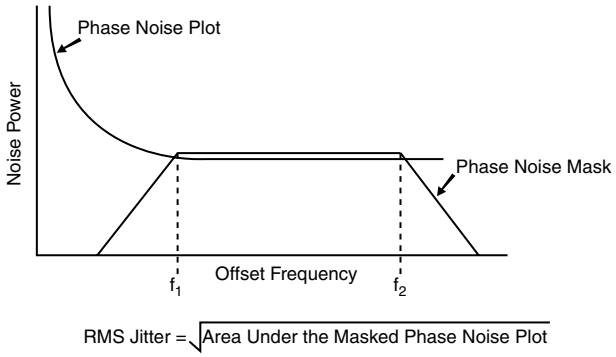
PARAMETER MEASUREMENT INFORMATION



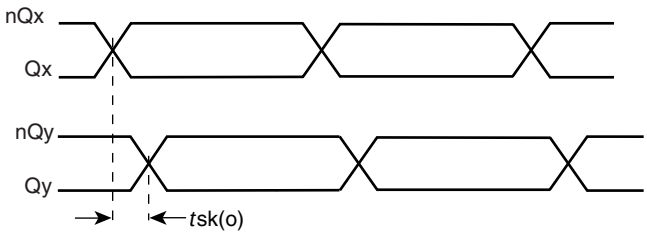
3.3V CORE/3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



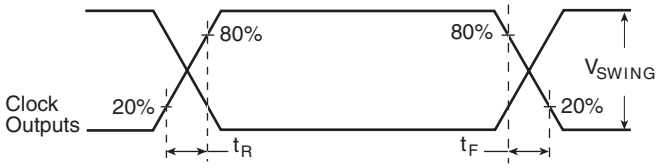
3.3V CORE/2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



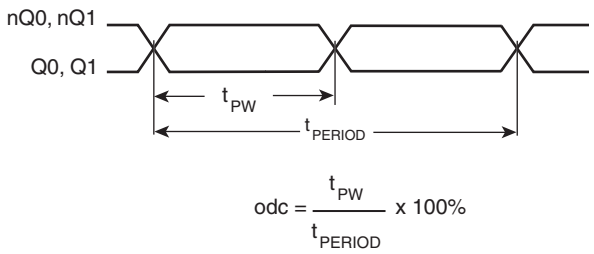
PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/tPERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843002I-72 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

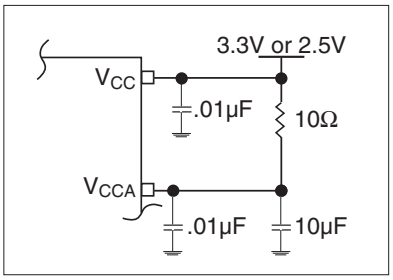


FIGURE 1. POWER SUPPLY FILTERING

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

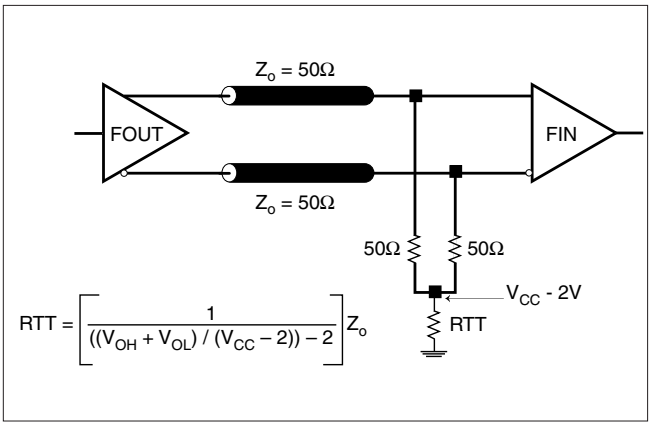


FIGURE 2A. LVPECL OUTPUT TERMINATION

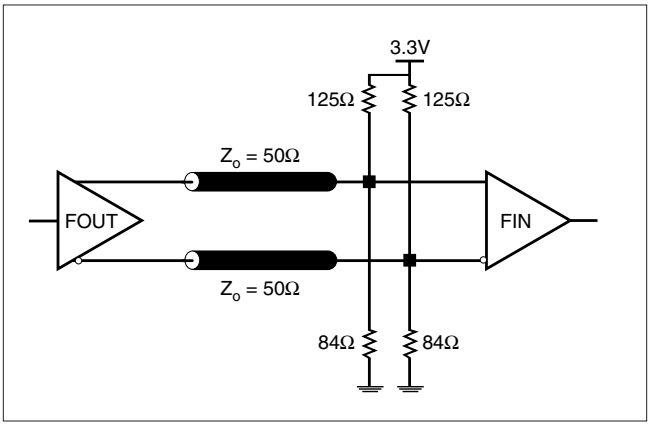


FIGURE 2B. LVPECL OUTPUT TERMINATION

Termination for 2.5V LVPECL Output

Figure 3A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

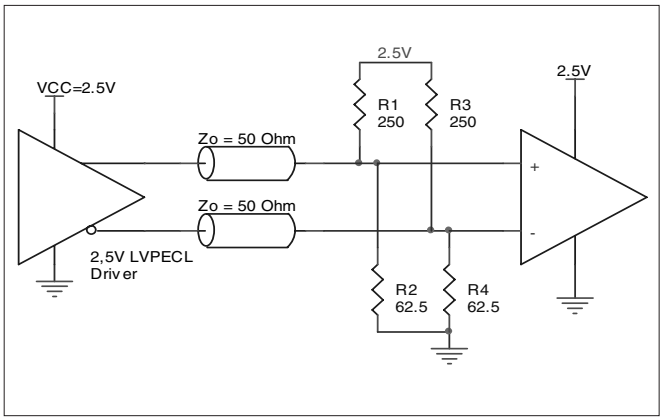


Figure 3A. 2.5V LVPECL Driver Termination Example

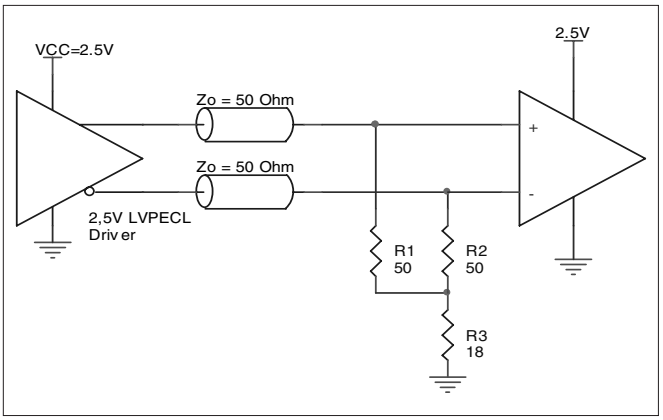


Figure 3B. 2.5V LVPECL Driver Termination Example

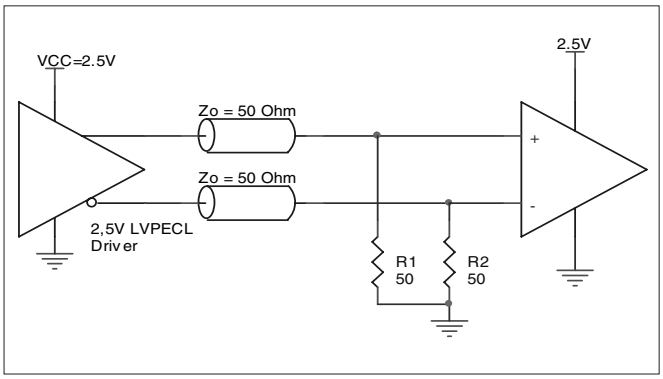


Figure 3C. 2.5V LVPECL Termination Example

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

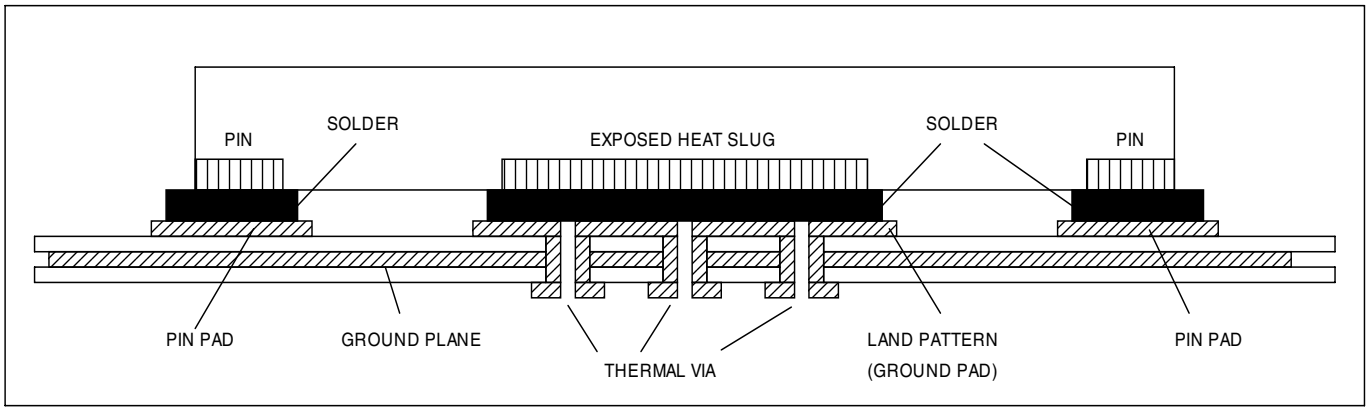


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

LAYOUT GUIDELINE

Figure 5 shows an example of ICS843002I-72 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The 19.2MHz pullable crystal is used. The bypass capacitor should be placed as close as possible to the power pins. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

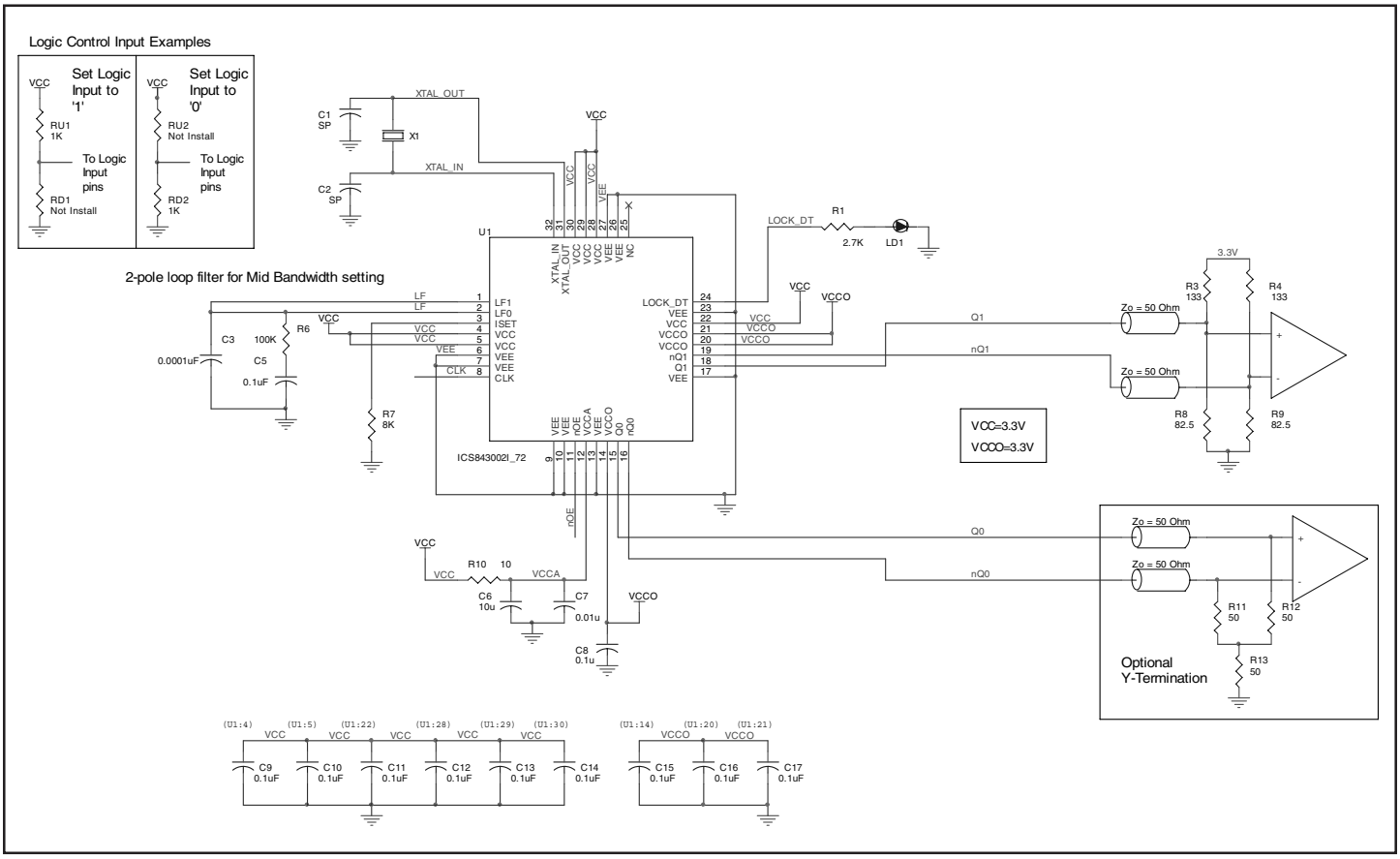


FIGURE 5. SCHEMATIC OF RECOMMENDED LAYOUT

VCXO-PLL External Components

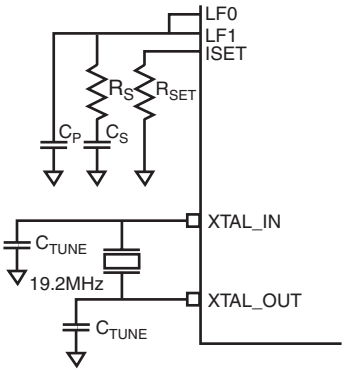
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal's C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal's C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependent on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_S, C_S and C_P values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note.*

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Unit
k_{VCXO}	VCXO Gain	7.8	kHz/V
C_{V_LOW}	Low Varactor Capacitance	2	pF
C_{V_HIGH}	High Varactor Capacitance	8	pF

VCXO-PLL Approximate Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	R_S (kΩ)	C_S (µF)	C_P (µF)	R_{SET} (kΩ)
75Hz (Low)	19.2MHz	15	1.0	0.01	8
500Hz (Mid)	19.2MHz	100	0.1	0.0001	8
1kHz (High)	19.2MHz	100	0.1	0.0001	4

Crystal Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
	Mode of Operation		Fundamental		
f_N	Frequency		19.2		MHz
f_T	Frequency Tolerance			±20	ppm
f_S	Frequency Stability			±20	ppm
	Operating Temperature Range	-40		85	°C
C_L	Load Capacitance		12		pF
C_O	Shunt Capacitance		4		pF
C_O/C_1	Pullability Ratio		220	240	
ESR	Equivalent Series Resistance			20	Ω
	Drive Level			1	mW
	Aging @ 25°C			±3 per year	ppm

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843002I-72.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843002I-72 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 140mA = **485.15mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

  Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 485.1mW + 60mW = **545.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.541W * 37°C/W = 105.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 6.*

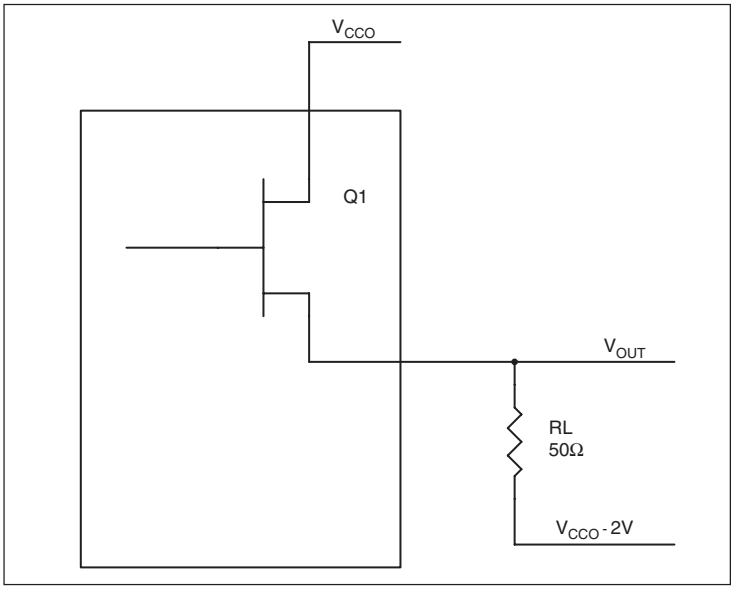


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

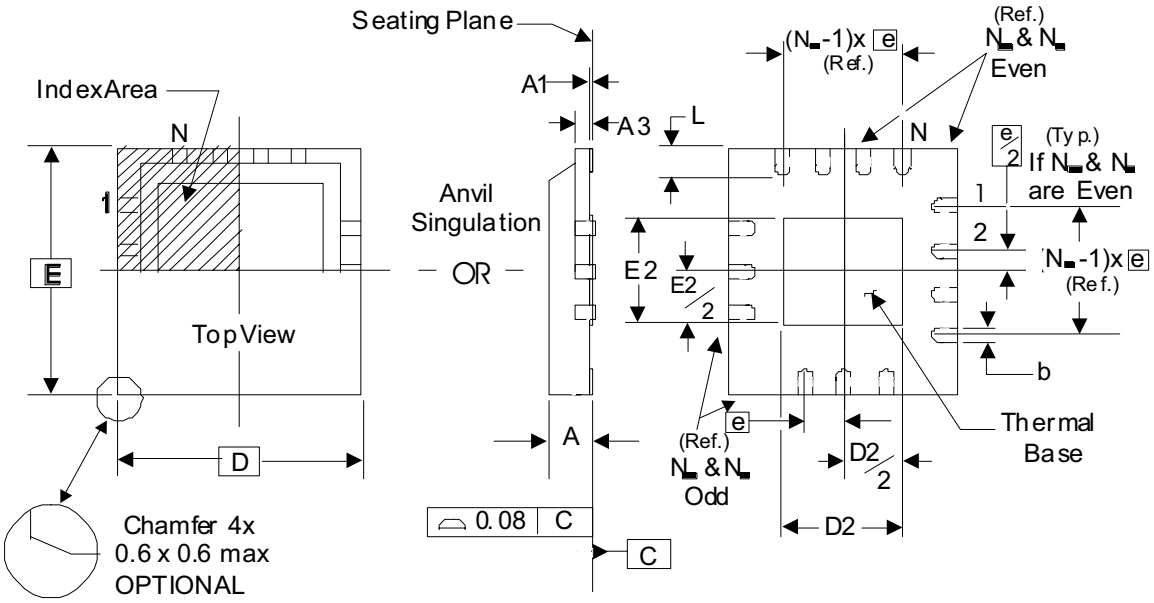
TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS843002I-72 is: 3199

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 11 below.

TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4)		
SYMBOL	**Minimum**	**Maximum**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D, E	5.0 BASIC	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843002BKI-72LF	ICS002BI72L	32 lead "Lead-Free" VFQFN	tube	-40°C to 85°C
843002BKI-72LFT	ICS002BI72L	32 lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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