TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

# TLCS-900/L Series

## TMP93CW40/41

TOSHIBA CORPORATION

Semiconductor Company

# Preface

Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

**CAUTION**

**How to release the HALT mode**

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of $f_{FPH}$) with IDLE1 or STOP mode (IDLE2, RUN is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low Voltage/Low Power

CMOS 16-Bit Microcontrollers

# TMP93CW40DF/TMP93CW41DF

## 1. Outline and Device Characteristics

TMP93CW40/W41 are high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP93CW40/CW41 enable low-voltage and low consumption power operation.

The TMP93CW40/W41 are housed in 100-pin flat package.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)
- TLCS-90 instruction mnemonic upward compatible
- 16-Mbyte linear address space
- General-purpose registers and resister bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed micro DMA: 4 channels (1.6 μs/2 bytes at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal RAM: 4 Kbytes
Internal ROM:

| | |
|---|---|
| TMP93CW40 | 128-Kbyte ROM |
| TMP93CW41 | None |

(4) External memory expansion
- Can be expanded up to 16 Mbytes (for both programs and data).
- AM8/$\overline{\text{AM16}}$ pin (select the external data bus width)
- Can mix 8- and 16-bit external data buses.
  ... Dynamic data bus sizing

(5) 8-bit timer: 2 channels

(6) 8-bit PWM timer: 2 channels

(7) 16-bit timer: 2 channels

(8) 4-bit pattern generator: 2 channels

(9) Serial interface: 2 channels

(10) 10-bit AD converter: 8 channels

(11) Watchdog timer

(12) Chip select/wait controller: 3 blocks

(13) Interrupt functions: 29

- 9 CPU interrupts ... SWI instruction, and Illegal instruction
- 14 internal interrupts
- 6 external interrupts

7-level priority can be set.

(14) I/O ports

79 pins for TMP93CW40 and 61 pins for TMP93CW41

(15) Standby function: 4 HALT modes (RUN, IDLE2, IDLE1, STOP)

(16) Clock gear function

- Dual clock operation
- Clock gear: High-frequency clock can be changed fc to fc/16.

(17) Wide operating voltage

- $V_{CC}$ = 2.7 to 5.5 V

(18) Package

| Type No. | Package |
|---|---|
| TMP93CW40DF<br>TMP93CW41DF | P-LQFP100-1414-0.50F |

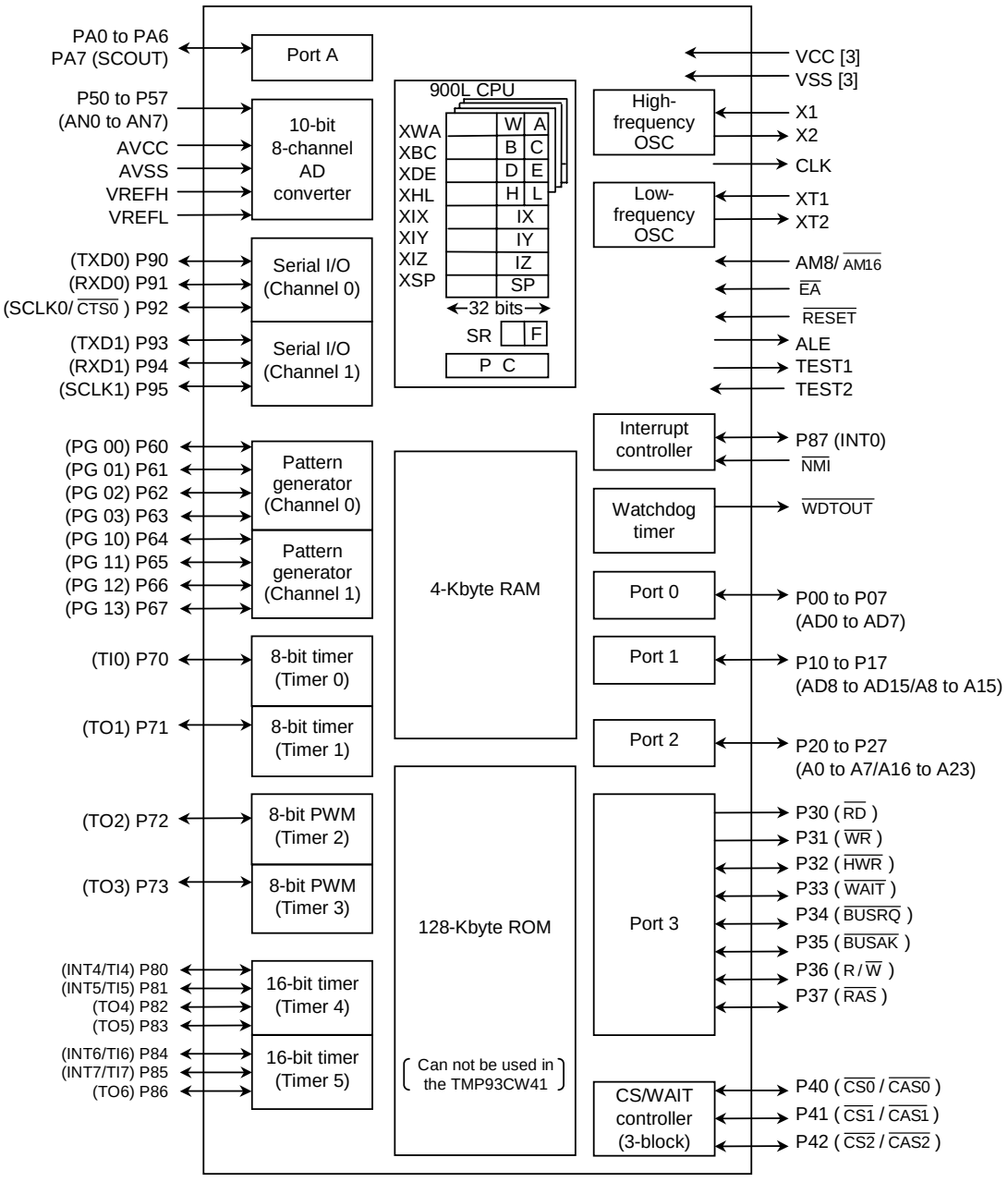


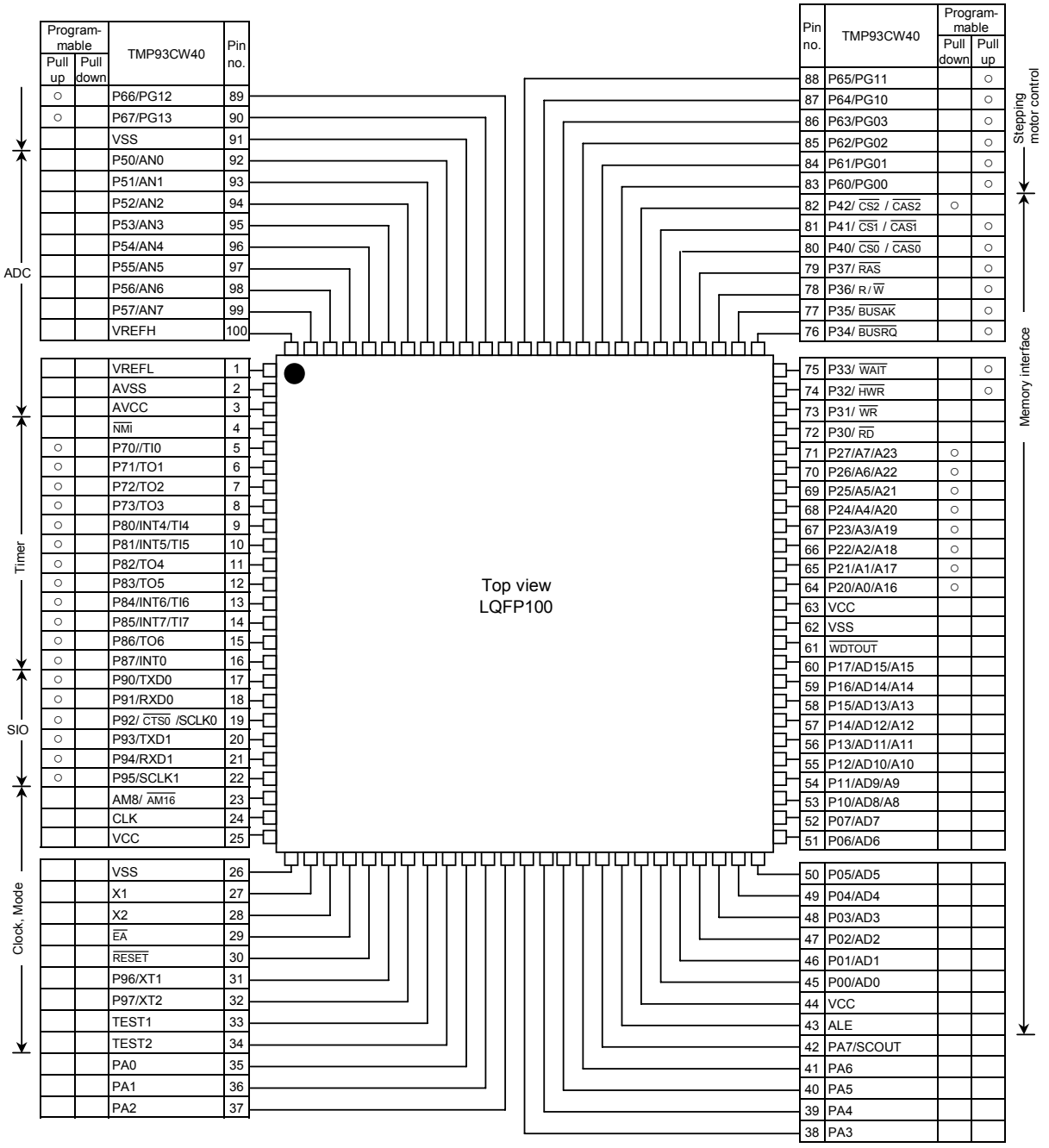

Figure 1.1 TMP93CW40/TMP93CW41 Block Diagram

# 2. Pin Assignment and Functions

The assignment of input/output pins for TMP93CW40/41, their name and outline functions are described below.

## 2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of TMP93CW40DF/W41DF.




Note: Because the TMP93CW41 does not have an internal ROM, P00 to P17 pins are fixed to AD0 to AD15 (the case of AM8/ $\overline{AM16}$ = 0), or to AD0 to AD7, A8 to A15 (the case of AM8/ $\overline{AM16}$ = 1); P30 to $\overline{RD}$; and P31 to $\overline{WR}$.

Figure 2.1.1 Pin Assignment (100-Pin LQFP)

## 2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 to Table 2.2.4 show pin names and functions.

Table 2.2.1 Pin Names and Functions (1/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P00 to P07<br>AD0 to AD7 | 8 | I/O<br>3-state | Port 0: I/O port that allows I/O to be selected on a bit basis<br>Address/Data (lower) : 0 to 7 for address/data bus |
| P10 to P17<br>AD8 to AD15<br>A8 to A15 | 8 | I/O<br>3-state<br>Output | Port 1: I/O port that allows I/O to be selected on a bit basis<br>Address data (upper) : 8 to 15 for address/data bus<br>Address: 8 to 15 for address bus |
| P20 to P27<br><br>A0 to A7<br>A16 to A23 | 8 | I/O<br><br>Output<br>Output | Port 2: I/O port that allows selection of I/O on a bit basis<br>(with pull-down resistor)<br>Address: 0 to 7 for address bus<br>Address: 16 to 23 for address bus |
| P30<br>$\overline{RD}$ | 1 | Output<br>Output | Port 30: Output port<br>Read: Strobe signal for reading external memory |
| P31<br>$\overline{WR}$ | 1 | Output<br>Output | Port 31: Output port<br>Write: Strobe signal for writing data on pins AD0 to AD7 |
| P32<br>$\overline{HWR}$ | 1 | I/O<br>Output | Port 32: I/O port (with pull-up resistor)<br>High write: Strobe signal for writing data on pins AD8 to AD15 |
| P33<br>$\overline{WAIT}$ | 1 | I/O<br>Input | Port 33: I/O port (with pull-up resistor)<br>Wait: Pin used to request CPU bus wait |
| P34<br>$\overline{BUSRQ}$ | 1 | I/O<br>Input | Port 34: I/O port (with pull-up resistor)<br>Bus request: Signal used to request high impedance for AD0 to AD15, A0 to A23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , R/$\overline{W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins.<br>(For external DMAC) |
| P35<br>$\overline{BUSAK}$ | 1 | I/O<br>Output | Port 35: I/O port (with pull-up resistor)<br>Bus acknowledge: Signal indicating that AD0 to AD15, A0 to A23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , R/$\overline{W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC) |
| P36<br>R/$\overline{W}$ | 1 | I/O<br>Output | Port 36: I/O port (with pull-up resistor)<br>Read/Write: 1 represents read or dummy cycle; 0, write cycle. |
| P37<br>$\overline{RAS}$ | 1 | I/O<br>Output | Port 37: I/O port (with pull-up resistor)<br>Row address strobe: Outputs RAS strobe for DRAM. |
| P40<br>$\overline{CS0}$<br>$\overline{CAS0}$ | 1 | I/O<br>Output<br>Output | Port 40: I/O port (with pull-up resistor)<br>Chip select 0: Outputs 0 when address is within specified address area.<br>Column address strobe 0: Outputs CAS strobe for DRAM when address is within specified address area. |

Note: With the external DMA controller, this device's built-in memory or built-in I/O cannot be accessed using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins.

Table 2.2.2 Pin Names and Functions (2/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P41<br>$\overline{CS1}$<br>$\overline{CAS1}$ | 1 | I/O<br>Output<br>Output | Port 41: I/O port (with pull-up resistor)<br>Chip select 1: Outputs 0 if address is within specified address area.<br>Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area. |
| P42<br>$\overline{CS2}$<br>$\overline{CAS2}$ | 1 | I/O<br>Output<br>Output | Port 42: I/O port (with pull-down resistor)<br>Chip select 2: Outputs 0 if address is within specified address area.<br>Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area. |
| P50 to P57<br>AN0 to AN7 | 8 | Input<br>Input | Port 5: Input port<br>Analog input: Input to AD converter |
| VREFH | 1 | Input | Pin for reference voltage input to AD converter (H) |
| VREFL | 1 | Input | Pin for reference voltage input to AD converter (L) |
| P60 to P63<br><br>PG00 to PG03 | 4 | I/O<br><br>Output | Ports 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor)<br>Pattern generator ports: 00 to 03 |
| P64 to P67<br><br>PG10 to PG13 | 4 | I/O<br><br>Output | Ports 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor)<br>Pattern generator ports: 10 to 13 |
| P70<br>TI0 | 1 | I/O<br>Input | Port 70: I/O port (with pull-up resistor)<br>Timer input 0: Timer 0 input |
| P71<br>TO1 | 1 | I/O<br>Output | Port 71: I/O port (with pull-up resistor)<br>Timer output 1: Timer 0 or 1 output |
| P72<br>TO2 | 1 | I/O<br>Output | Port 72: I/O port (with pull-up resistor)<br>PWM output 2: 8-bit PWM timer 2 output |
| P73<br>TO3 | 1 | I/O<br>Output | Port 73: I/O port (with pull-up resistor)<br>PWM output 3: 8-bit PWM timer 3 output |
| P80<br>TI4<br>INT4 | 1 | I/O<br>Input<br>Input | Port 80: I/O port (with pull-up resistor)<br>Timer input 4: Timer 4 count/capture trigger signal input<br>Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge |
| P81<br>TI5<br>INT5 | 1 | I/O<br>Input<br>Input | Port 81: I/O port (with pull-up resistor)<br>Timer input 5: Timer 4 count/capture trigger signal input<br>Interrupt request pin 5: Interrupt request pin with rising edge |
| P82<br>TO4 | 1 | I/O<br>Output | Port 82: I/O port (with pull-up resistor)<br>Timer output 4: Timer 4 output pin |
| P83<br>TO5 | 1 | I/O<br>Output | Port 83: I/O port (with pull-up resistor)<br>Timer output 5: Timer 4 output pin |

Table 2.2.3 Pin Names and Functions (3/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| P84<br>TI6<br>INT6 | 1 | I/O<br>Input<br>Input | Port 84: I/O port (with pull-up resistor)<br>Timer input 6: Timer 5 count/capture trigger signal input<br>Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge |
| P85<br>TI7<br>INT7 | 1 | I/O<br>Input<br>Input | Port 85: I/O port (with pull-up resistor)<br>Timer input 7: Timer 5 count/capture trigger signal input<br>Interrupt request pin 7: Interrupt request pin with rising edge |
| P86<br>TO6 | 1 | I/O<br>Output | Port 86: I/O port (with pull-up resistor)<br>Timer output 6: Timer 5 output pin |
| P87<br>INT0 | 1 | I/O<br>Input | Port 87: I/O port (with pull-up resistor)<br>Interrupt request pin 0: Interrupt request pin with programmable level/rising edge |
| P90<br>TXD0 | 1 | I/O<br>Output | Port 90: I/O port (with pull-up resistor)<br>Serial send data 0 |
| P91<br>RXD0 | 1 | I/O<br>Input | Port 91: I/O port (with pull-up resistor)<br>Serial receive data 0 |
| P92<br>$\overline{CTS0}$<br>SCLK0 | 1 | I/O<br>Input<br>I/O | Port 92: I/O port (with pull-up resistor)<br>Serial data send enable 0 (Clear to Send)<br>Serial Clock I/O 0 |
| P93<br>TXD1 | 1 | I/O<br>Output | Port 93: I/O port (with pull-up resistor)<br>Serial send data 1 |
| P94<br>RXD1 | 1 | I/O<br>Input | Port 94: I/O port (with pull-up resistor)<br>Serial receive data 1 |
| P95<br>SCLK1 | 1 | I/O<br>I/O | Port 95: I/O port (with pull-up resistor)<br>Serial clock I/O 1 |
| PA0 to PA6 | 7 | I/O | Port A: I/O ports |
| PA7<br>SCOUT | 1 | I/O<br>Output | Port A7: I/O port<br>System Clock Output: Outputs system clock or 1/2 oscillation clock for synchronizing to external circuit. |
| $\overline{WDTOUT}$ | 1 | Output | Watchdog timer output pin |
| $\overline{NMI}$ | 1 | Input | Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program. |
| CLK | 1 | Output | Clock output: Outputs [System Clock ÷ 2] Clock.<br>Pulled-up during reset.<br>Can be set to Output Disable for reducing noise. |
| $\overline{EA}$ | 1 | Input | External access: “0” should be inputted with TMP93CW41.<br>“1” should be inputted with TMP93CW40. |

Table 2.2.4 Pin Names and Functions (4/4)

| Pin Name | Number of Pins | I/O | Functions |
|---|---|---|---|
| AM8/ $\overline{AM16}$ | 1 | Input | Address Mode: Selects external data bus width.<br>(The case of TMP93CW40)<br>"1" should be inputted. The data bus width for external access is set by chip select/wait control register, Port 1 control register.<br>(The case of TMP93CW41)<br>"0" should be inputted with fixed 16-bit bus width or 16-bit bus interlarded with 8-bit bus.<br>"1" should be inputted with fixed 8-bit bus width. |
| ALE | 1 | Output | Address latch enable<br>Can be set to output disable for reducing noise. |
| $\overline{RESET}$ | 1 | Input | Reset: initializes LSI. (with pull-up resistor) |
| X1/X2 | 2 | Input/Output | High-frequency oscillator connecting pin |
| XT1<br>P96 | 1 | Input<br>I/O | Low-frequency oscillator connecting pin<br>Port 96: I/O port (open-drain output) |
| XT2<br>P97 | 1 | Output<br>I/O | Low-frequency oscillator connecting pin<br>Port 97: I/O port (open-drain output) |
| TEST1/TEST2 | 2 | Output/Input | TEST1 Should be connected with TEST2 pin.<br>Do not connect to any other pins |
| VCC | 3 | | Power supply pin |
| VSS | 3 | | GND pin (0 V) |
| AVCC | 1 | | Power supply pin for AD converter |
| AVSS | 1 | | GND pin for AD converter (0 V) |

Note: Pull-up/pull-down resistor can be released from the pin by software.

# 3. Operation

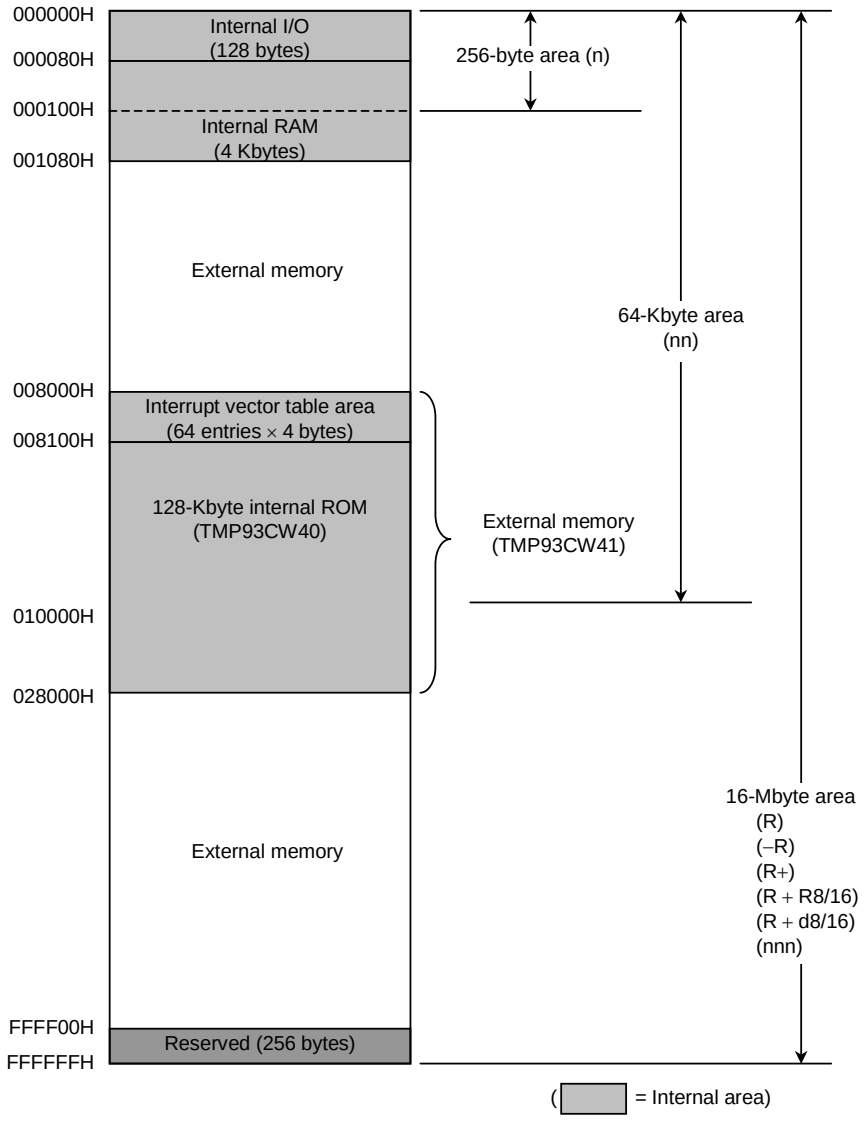
This section describes in blocks the functions and basic operations of the TMP93CW40/W41 devices.

## 3.1 CPU

The TMP93CW40/W41 devices have a built-in high-performance 16-bit CPU (900/L_CPU). (For CPU operation, see TLCS-900/L CPU in the previous section).

## 3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CW40/W41.




Note: Resetting sets the stack pointer (XSP) to 100H.
The 256-byte area from FFFF00H to FFFFFFH can not be used.

Figure 3.2.1 Memory Map

# 4. Electrical Characteristics

"X" used in an expression shows a frequency of clock $f_{FPH}$ selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value in an example is calculated at fc, gear = 1/fc (SYSCR1 < SYSCK, GEAR2:0 > = "0000").

## 4.1 Maximum Ratings (TMP93CW40F, TMP93CW41DF)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | −0.5 to 6.5 | V |
| Input voltage | $V_{IN}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Output current (total) | $\Sigma I_{OL}$ | 120 | mA |
| Output current (total) | $\Sigma I_{OH}$ | −80 | mA |
| Power dissipation (Ta = 85°C) | $P_D$ | 600 | mW |
| Soldering temperature (10 s) | $T_{SOLDER}$ | 260 | °C |
| Storage temperature | $T_{STG}$ | −65 to 150 | °C |
| Operating temperature | $T_{OPR}$ | −40 to 85 | °C |

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (1/2)

Ta = −40 to 85°C

| Parameter | | Symbol | Condition | | Min | Typ. (Note) | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage ($AV_{CC} = V_{CC}$, $AV_{CC} = V_{SS} = 0$ V) | | $V_{CC}$ | fc = 4 to 20 MHz | fs = 30 to 34 kHz | 4.5 | | 5.5 | V |
| | | | fc = 4 to 12.5 MHz | | 2.7 | | | |
| Input low voltage | AD0 to AD15 | $V_{IL}$ | $V_{CC} \geq 4.5$ V | | −0.3 | | 0.8 | V |
| | | | $V_{CC} < 4.5$ V | | | | 0.6 | |
| | Port 2 to port A (except P87) | $V_{IL1}$ | $V_{CC}$ = 2.7 to 5.5 V | | | | 0.3 $V_{CC}$ | |
| | $\overline{RESET}$ , $\overline{NMI}$ , INT0 | $V_{IL2}$ | | | | | 0.25 $V_{CC}$ | |
| | $\overline{EA}$ , AM8/ $\overline{AM16}$ | $V_{IL3}$ | | | | | 0.3 | |
| | X1 | $V_{IL4}$ | | | | | 0.2 $V_{CC}$ | |
| Input high voltage | AD0 to AD15 | $V_{IH}$ | $V_{CC} \geq 4.5$ V | | 2.2 | | $V_{CC}$ + 0.3 | |
| | | | $V_{CC} < 4.5$ V | | 2.0 | | | |
| | Port 2 to port A (except P87) | $V_{IH1}$ | $V_{CC}$ = 2.7 to 5.5 V | | 0.7 $V_{CC}$ | | | |
| | $\overline{RESET}$ , $\overline{NMI}$ , INT0 | $V_{IH2}$ | | | 0.75 $V_{CC}$ | | | |
| | $\overline{EA}$ , AM8/ $\overline{AM16}$ | $V_{IH3}$ | | | $V_{CC}$ − 0.3 | | | |
| | X1 | $V_{IH4}$ | | | 0.8 $V_{CC}$ | | | |
| Output low voltage | | $V_{OL}$ | $I_{OL}$ = 1.6 mA ($V_{CC}$ = 2.7 to 5.5 V) | | | | 0.45 | V |
| Output high voltage | | $V_{OH1}$ | $I_{OH}$ = −400 μA ($V_{CC}$ = 3 V ± 10%) | | 2.4 | | | |
| | | $V_{OH2}$ | $I_{OH}$ = −400 μA ($V_{CC}$ = 5 V ± 10%) | | 4.2 | | | |

Note: Typical values are for Ta = 25°C and $V_{CC}$ = 5 V unless otherwise noted.

## DC Characteristics (2/2)

| Parameter | Symbol | Condition | Min | Typ. (Note1) | Max | Unit |
|---|---|---|---|---|---|---|
| Darlington drive current (8 output pins max) | $I_{DAR}$ (Note 2) | $V_{EXT}$ = 1.5 V, $R_{EXT}$ = 1.1 kΩ (when $V_{CC}$ = 5 V ± 10%) | −1.0 | | −3.5 | mA |
| Input leakage current | $I_{LI}$ | $0.0 \le V_{IN} \le V_{CC}$ | | 0.02 | ±5 | μA |
| Output leakage current | $I_{LO}$ | $0.2 \le V_{IN} \le V_{CC} - 0.2$ | | 0.05 | ±10 | |
| Powerdown voltage (at Stop, RAM Back-up) | $V_{STOP}$ | $V_{IL2}$ = 0.2 $V_{CC}$, $V_{IH2}$ = 0.8 $V_{CC}$ | 2.0 | | 6.0 | V |
| $\overline{RESET}$ pull-up resistor | $R_{RST}$ | $V_{CC}$ = 5 V ± 10% | 50 | | 150 | kΩ |
| | | $V_{CC}$ = 3 V ± 10% | 80 | | 200 | |
| Pin capacitance | $C_{IO}$ | fc = 1 MHz | | | 10 | pF |
| Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0 | $V_{TH}$ | | 0.4 | 1.0 | | V |
| Programmable pull-down resistor | $R_{KL}$ | $V_{CC}$ = 5 V ± 10% | 10 | | 80 | kΩ |
| | | $V_{CC}$ = 3 V ± 10% | 30 | | 150 | |
| Programmable pull-up resistor | $R_{KH}$ | $V_{CC}$ = 5 V ± 10% | 50 | | 150 | |
| | | $V_{CC}$ = 3 V ± 10% | 100 | | 300 | |
| NORMAL (Note 3) | $I_{CC}$ | $V_{CC}$ = 5 V ± 10%, fc = 20 MHz | | 19 | 25 | mA |
| NORMAL2 (Note 4) | | | | 24 | 30 | |
| RUN | | | | 17 | 25 | |
| IDLE2 | | | | 10 | 15 | |
| IDLE1 | | | | 3.5 | 5 | |
| NORMAL (Note 3) | | $V_{CC}$ = 3 V ± 10%, fc = 12.5 MHz (Typ: $V_{CC}$ = 3.0 V) | | 6.5 | 10 | mA |
| NORMAL2 (Note 4) | | | | 9.5 | 13 | |
| RUN | | | | 5.0 | 9 | |
| IDLE2 | | | | 3.0 | 5 | |
| IDLE1 | | | | 0.8 | 1.5 | |
| SLOW (Note 3) | | $V_{CC}$ = 3 V ± 10%, fs = 32.768 kHz (Typ: $V_{CC}$ = 3.0 V) | | 20 | 45 | μA |
| RUN | | | | 16 | 40 | |
| IDLE2 | | | | 10 | 30 | |
| IDLE1 | | | | 5 | 25 | |
| STOP | | Ta ≤ 50°C | | 0.2 | 10 | μA |
| | | Ta ≤ 70°C | | | 20 | |
| | | Ta ≤ 85°C | | | 50 | |

Note 1: Typical values are for Ta = 25°C and $V_{CC}$ = 5 V unless otherwise Noted.

Note 2: $I_{DAR}$ is guranteed for total of up to 8 ports.

Note 3: The condition of measurement of $I_{CC}$ (NORMAL/SLOW).
Only CPU operates. Output ports are open and Input ports fixed.

Note 4: The condition of measurement of $I_{CC}$ (NORMAL2).
CPU and all peripherals operate. Output ports are open and input ports fixed.

## 4.3 AC Characteristics

(1) $V_{CC} = 5\ V \pm 10\%$

| No. | Parameter | Symbol | Variable | | 16 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | Osc. period ( = x) | $t_{OSC}$ | 50 | 31250 | 62.5 | | 50 | | ns |
| 2 | CLK pulse width | $t_{CLK}$ | 2x – 40 | | 85 | | 60 | | ns |
| 3 | A0 to A23 valid → CLK hold | $t_{AK}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 4 | CLK valid → A0 to A23 hold | $t_{KA}$ | 1.5x – 70 | | 24 | | 5 | | ns |
| 5 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 6 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 7 | ALE high pulse width | $t_{LL}$ | x – 40 | | 23 | | 10 | | ns |
| 8 | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall | $t_{LC}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 9 | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise | $t_{CL}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 10 | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACL}$ | x – 25 | | 38 | | 25 | | ns |
| 11 | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 44 | | 25 | | ns |
| 12 | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold | $t_{CA}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 13 | A0 to A15 valid → D0 to D15 input | $t_{ADL}$ | | 3.0x – 55 | | 133 | | 95 | ns |
| 14 | A0 to A23 valid → D0 to D15 input | $t_{ADH}$ | | 3.5x – 65 | | 154 | | 110 | ns |
| 15 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 60 | | 65 | | 40 | ns |
| 16 | $\overline{RD}$ low pulse width | $t_{RR}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 17 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | 0 | | ns |
| 18 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 15 | | 48 | | 35 | | ns |
| 19 | $\overline{WR}$ low pulse width | $t_{WW}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 20 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 55 | | 70 | | 45 | | ns |
| 21 | $\overline{WR}$ rise → D0 to D15 hold | $t_{WD}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 22 | A0 to A23 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode] | $t_{AWH}$ | | 3.5x – 90 | | 129 | | 85 | ns |
| 23 | A0 to A15 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode] | $t_{AWL}$ | | 3.0x – 80 | | 108 | | 70 | ns |
| 24 | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold [(1 + N) WAIT mode] | $t_{CW}$ | 2.0x + 0 | | 125 | | 100 | | ns |
| 25 | A0 to A23 valid → Port input | $t_{APH}$ | | 2.5x – 120 | | 36 | | 5 | ns |
| 26 | A0 to A23 valid → Port hold | $t_{APH2}$ | 2.5x + 50 | | 206 | | 175 | | ns |
| 27 | $\overline{WR}$ rise → Port valid | $t_{CP}$ | | 200 | | 200 | | 200 | ns |
| 28 | A0 to A23 valid → $\overline{RAS}$ fall | $t_{ASRH}$ | 1.0x – 40 | | 23 | | 10 | | ns |
| 29 | A0 to A15 valid → $\overline{RAS}$ fall | $t_{ASRL}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 30 | $\overline{RAS}$ fall → D0 to D15 input | $t_{RAC}$ | | 2.5x – 70 | | 86 | | 55 | ns |
| 31 | $\overline{RAS}$ fall → A0 to A15 hold | $t_{RAH}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 32 | $\overline{RAS}$ low pulse width | $t_{RAS}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 33 | $\overline{RAS}$ high pulse width | $t_{RP}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 34 | $\overline{CAS}$ fall → $\overline{RAS}$ rise | $t_{RSH}$ | 1.0x – 40 | | 23 | | 10 | | ns |
| 35 | $\overline{RAS}$ rise → $\overline{CAS}$ rise | $t_{RSC}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 36 | $\overline{RAS}$ fall → $\overline{CAS}$ fall | $t_{RCD}$ | 1.0x – 40 | | 23 | | 10 | | ns |
| 37 | $\overline{CAS}$ fall → D0 to D15 input | $t_{CAC}$ | | 1.5x – 65 | | 29 | | 10 | ns |
| 38 | $\overline{CAS}$ low pulse width | $t_{CAS}$ | 1.5x – 30 | | 64 | | 40 | | ns |

AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, $C_L = 50$ pF
  (However $C_L = 100$ pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × $V_{CC}$/Low 0.2 × $V_{CC}$ (Except for AD0 to AD15)

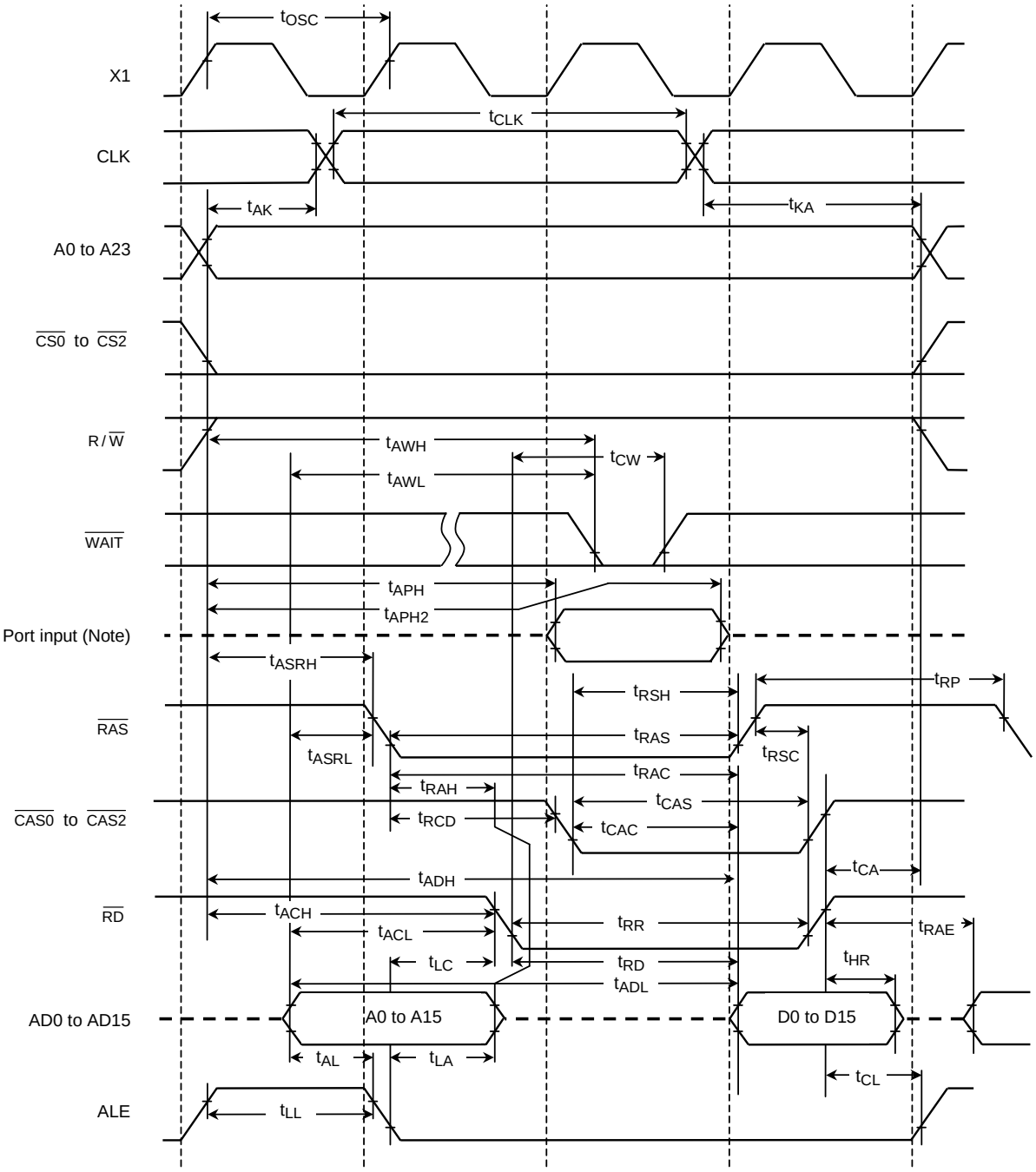
(2) $V_{CC} = 3\ V \pm 10\%$

| No. | Parameter | Symbol | Variable | | 12.5 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | Osc. period ( = x) | $t_{OSC}$ | 80 | 31250 | 80 | | ns |
| 2 | CLK pulse width | $t_{CLK}$ | 2x – 40 | | 120 | | ns |
| 3 | A0 to A23 valid → CLK hold | $t_{AK}$ | 0.5x – 30 | | 10 | | ns |
| 4 | CLK valid → A0 to A23 hold | $t_{KA}$ | 1.5x – 80 | | 40 | | ns |
| 5 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 35 | | 5 | | ns |
| 6 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 35 | | 5 | | ns |
| 7 | ALE high pulse width | $t_{LL}$ | x – 60 | | 20 | | ns |
| 8 | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall | $t_{LC}$ | 0.5x – 35 | | 5 | | ns |
| 9 | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise | $t_{CL}$ | 0.5x – 40 | | 0 | | ns |
| 10 | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACL}$ | x – 50 | | 30 | | ns |
| 11 | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 70 | | ns |
| 12 | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold | $t_{CA}$ | 0.5x – 40 | | 0 | | ns |
| 13 | A0 to A15 valid → D0 to D15 input | $t_{ADL}$ | | 3.0x – 110 | | 130 | ns |
| 14 | A0 to A23 valid → D0 to D15 input | $t_{ADH}$ | | 3.5x – 125 | | 155 | ns |
| 15 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 115 | | 45 | ns |
| 16 | $\overline{RD}$ low pulse width | $t_{RR}$ | 2.0x – 40 | | 120 | | ns |
| 17 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | ns |
| 18 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 25 | | 55 | | ns |
| 19 | $\overline{WR}$ low pulse width | $t_{WW}$ | 2.0x – 40 | | 120 | | ns |
| 20 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 120 | | 40 | | ns |
| 21 | $\overline{WR}$ rise → D0 to D15 hold | $t_{WD}$ | 0.5x – 40 | | 0 | | ns |
| 22 | A0 to A23 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode] | $t_{AWH}$ | | 3.5x – 130 | | 150 | ns |
| 23 | A0 to A15 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode] | $t_{AWL}$ | | 3.0x – 100 | | 140 | ns |
| 24 | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold [(1 + N) WAIT mode] | $t_{CW}$ | 2.0x + 0 | | 160 | | ns |
| 25 | A0 to A23 valid → Port input | $t_{APH}$ | | 2.5x – 195 | | 5 | ns |
| 26 | A0 to A23 valid → Port hold | $t_{APH2}$ | 2.5x + 50 | | 250 | | ns |
| 27 | $\overline{WR}$ rise → Port valid | $t_{CP}$ | | 200 | | 200 | ns |
| 28 | A0 to A23 valid → $\overline{RAS}$ fall | $t_{ASRH}$ | 1.0x – 60 | | 20 | | ns |
| 29 | A0 to A15 valid → $\overline{RAS}$ fall | $t_{ASRL}$ | 0.5x – 40 | | 0 | | ns |
| 30 | $\overline{RAS}$ fall → D0 to D15 input | $t_{RAC}$ | | 2.5x – 90 | | 110 | ns |
| 31 | $\overline{RAS}$ fall → A0 to A15 hold | $t_{RAH}$ | 0.5x – 25 | | 15 | | ns |
| 32 | $\overline{RAS}$ low pulse width | $t_{RAS}$ | 2.0x – 40 | | 120 | | ns |
| 33 | $\overline{RAS}$ high pulse width | $t_{RP}$ | 2.0x – 40 | | 120 | | ns |
| 34 | $\overline{CAS}$ fall → $\overline{RAS}$ rise | $t_{RSH}$ | 1.0x – 55 | | 25 | | ns |
| 35 | $\overline{RAS}$ rise → $\overline{CAS}$ rise | $t_{RSC}$ | 0.5x – 25 | | 15 | | ns |
| 36 | $\overline{RAS}$ fall → $\overline{CAS}$ fall | $t_{RCD}$ | 1.0x – 40 | | 40 | | ns |
| 37 | $\overline{CAS}$ fall → D0 to D15 input | $t_{CAC}$ | | 1.5x – 120 | | 0 | ns |
| 38 | $\overline{CAS}$ low pulse width | $t_{CAS}$ | 1.5x – 40 | | 80 | | ns |

AC measuring conditions

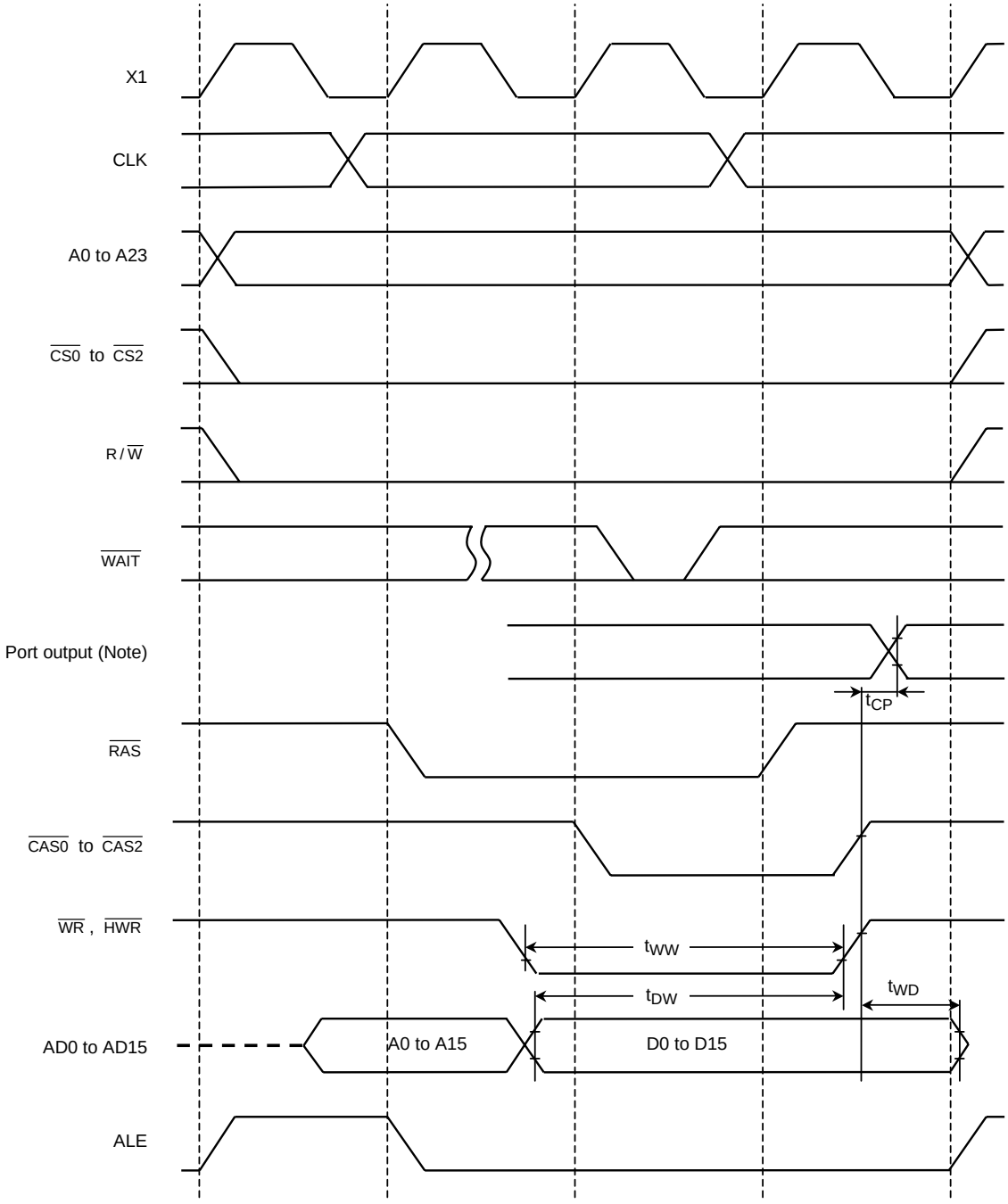
- Output level: High $0.7 \times V_{CC}$/Low $0.3 \times V_{CC}$, $C_L = 50$ pF
- Input level: High $0.9 \times V_{CC}$/Low $0.1 \times V_{CC}$

(1) Read cycle




Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle




Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

## 4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

| Parameter | Symbol | Power Supply | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Analog reference voltage (+) | $V_{REFH}$ | $V_{CC} = 5 V \pm 10\%$ | $V_{CC} - 1.5$ V | $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC} = 3 V \pm 10\%$ | $V_{CC} - 0.2$ V | $V_{CC}$ | $V_{CC}$ | |
| Analog reference voltage (–) | $V_{REFL}$ | $V_{CC} = 5 V \pm 10\%$ | $V_{SS}$ | $V_{SS}$ | $V_{SS} + 0.2$ V | |
| | | $V_{CC} = 3 V \pm 10\%$ | $V_{SS}$ | $V_{SS}$ | $V_{SS} + 0.2$ V | |
| Analog input voltage range | $V_{AIN}$ | | $V_{REFL}$ | | $V_{REFH}$ | |
| Analog current for analog reference voltage <VREFON> = 1 | $I_{REF}$ ($V_{REFL} = 0$ V) | $V_{CC} = 5 V \pm 10\%$ | | 0.5 | 1.5 | mA |
| | | $V_{CC} = 3 V \pm 10\%$ | | 0.3 | 0.9 | |
| <VREFON> = 0 | | $V_{CC} = 2.7$ to 5.5 V | | 0.02 | 5.0 | μA |
| Error (excluding quantizing error) | – | $V_{CC} = 5 V \pm 10\%$ | | ±1.0 | ±3.0 | LSB |
| | | $V_{CC} = 3 V \pm 10\%$ | | ±1.0 | ±3.0 | |

Note 1: 1LSB = $(V_{REFH} - V_{REFL}) / 2^{10}$ [V]

Note 2: Minimum operation frequency

The operation of the AD converter is guaranteed only when fc (high-frequency oscillator) is used. (It is not guaranteed when fs is used.) Additionally, it is guaranteed when the clock frequency which is selected by the clock gear is 4 MHz or more.

Note 3: The value $I_{CC}$ includes the current which flows through the AVCC pin.

## 4.5 Serial Channel Timing

### (1) I/O interface mode

#### a. SCLK input mode

| Parameter | Symbol | Variable | | 32.768 kHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| SCLK cycle | $t_{SCY}$ | 16X | | 488 μs | | 1280 | | 800 | | ns |
| Output data → Rising edge or falling edge (Note 2) of SCLK | $t_{OSS}$ | $t_{SCY}/2 - 5X - 50$ | | 91.5 μs | | 190 | | 100 | | ns |
| SCLK rising edge or falling edge (Note 2) → Output data hold | $t_{OHS}$ | 5x – 100 | | 152 μs | | 300 | | 150 | | ns |
| SCLK rising edge or falling edge (Note 2) → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| SCLK rising edge or falling edge (Note 2) → Effective data input | $t_{SRD}$ | | $t_{SCY} - 5X - 100$ | | 336 μs | | 780 | | 450 | ns |

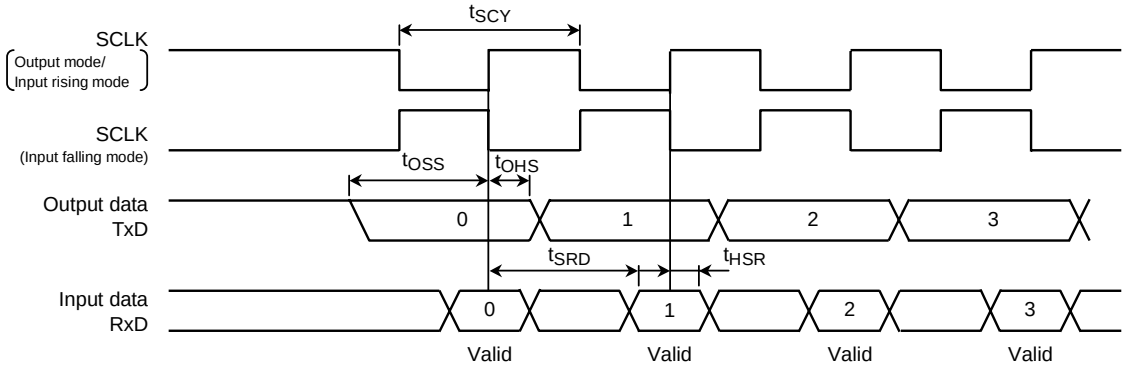
Note 1: When fs is used as system clock ($f_{SYS}$) or fs is used as input clock to prescaler.

Note 2: SCLK rising/falling timing ... SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

#### b. SCLK output mode

| Parameter | Symbol | Variable | | 32.768 kHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| SCLK cycle (programmable) | $t_{SCY}$ | 16x | 8192x | 488 | 250 ms | 1.28 | 655.36 | 0.8 | 409.6 | μs |
| Output data → SCLK rising edge | $t_{OSS}$ | $t_{SCY} - 2x - 150$ | | 427 μs | | 970 | | 550 | | ns |
| SCLK rising edge → Output data hold | $t_{OHS}$ | 2x – 80 | | 60 μs | | 80 | | 20 | | ns |
| SCLK rising edge → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| SCLK rising edge → Effective data input | $t_{SRD}$ | | $t_{SCY} - 2x - 150$ | | 428 μs | | 970 | | 550 | ns |

Note: When fs is used as system clock ($f_{SYS}$) or fs is used as input clock to prescaler.



## 4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6 and TI7)

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Clock cycle | $t_{VCK}$ | 8X + 100 | | 740 | | 500 | | ns |
| Low level clock pulse width | $t_{VCKL}$ | 4X + 40 | | 360 | | 240 | | ns |
| High level clock pulse width | $t_{VCKH}$ | 4X + 40 | | 360 | | 240 | | ns |

## 4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $\overline{NMI}$, INT0 low level pulse width | $t_{INTAL}$ | 4X | | 320 | | 200 | | ns |
| $\overline{NMI}$, INT0 high level pulse width | $t_{INTAH}$ | 4X | | 320 | | 200 | | ns |

(2) INT4 to 7 interrupts, capture

Input pulse width of INT4 to 7 depends on the operation clock of CPU and Timer (9-bit prescaler). The following shows the pulse width in each clock.

| System Clock Selected <SYSCK> | Prescaler Clock Selected <PRCK1:0> | $t_{INTBL}$ (INT4 to 7 low level pulse width) | | $t_{INTBH}$ (INT4 to 7 high level pulse width) | | Unit |
|---|---|---|---|---|---|---|
| | | Variable | 20 MHz | Variable | 20 MHz | |
| | | Min | Min | Min | Min | |
| 0 (fc) | 00 ($f_{FPH}$) | 8X + 100 | 500 | 8X + 100 | 500 | ns |
| | 01 (fs) | 8XT + 0.1 | 244.3 | 8XT + 0.1 | 244.3 | μs |
| | 10 (fc/16) | 128X + 0.1 | 6.5 | 128X + 0.1 | 6.5 | |
| 1 (fs) (Note 2) | 00 ($f_{FPH}$) | 8XT + 0.1 | 244.3 | 8XT + 0.1 | 244.3 | |
| | 01 (fs) | | | | | |

Note 1: XT represents the cycle of the low frequency clock fs. Calculated at fs = 32.768 kHz.

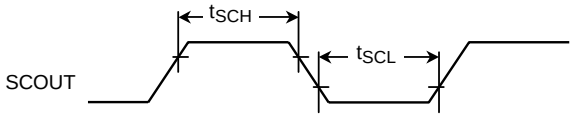
Note 2: When fs is used as the system clock, fc/16 can not be selected for the prescaler clock.

## 4.8 SCOUT pin AC characteristics

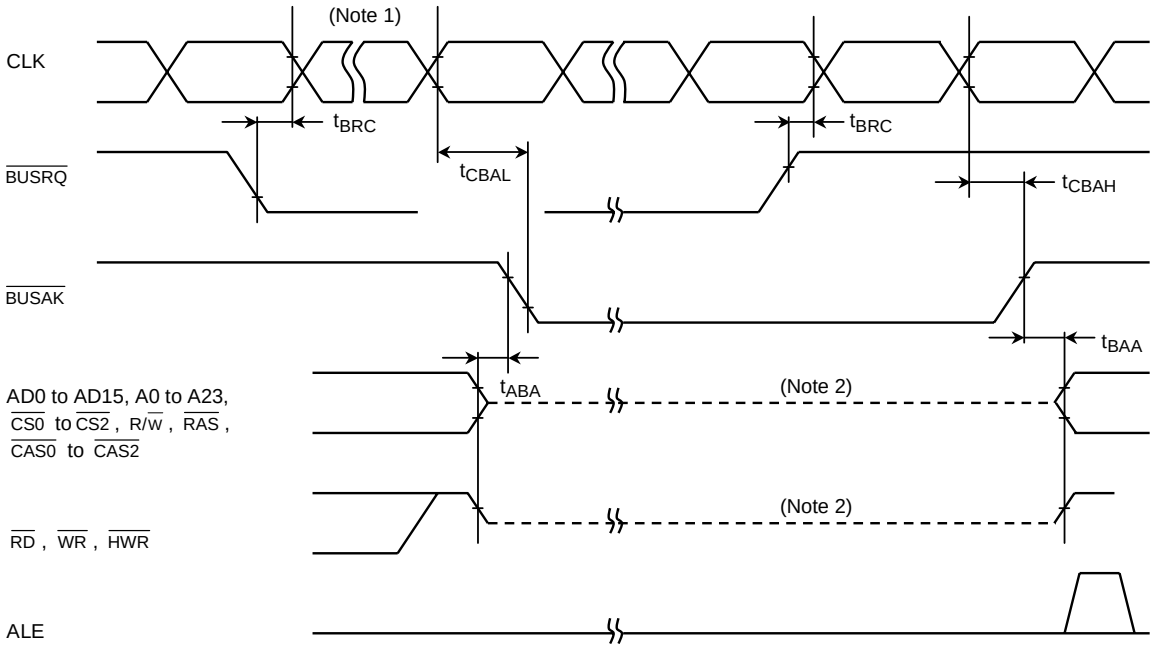
| Parameter | | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| High-level pulse width | $V_{CC}$ = 5 V ± 10% | $t_{SCH}$ | 0.5X – 10 | | 30 | | 15 | | ns |
| | $V_{CC}$ = 3 V ± 10% | | 0.5X – 20 | | 20 | | – | – | |
| Low-level pulse width | $V_{CC}$ = 5 V ± 10% | $t_{SCL}$ | 0.5X – 10 | | 30 | | 15 | | ns |
| | $V_{CC}$ = 3 V ± 10% | | 0.5X – 20 | | 20 | | – | – | |

Measurement condition

- Output level: High 2.2 V/Low 0.8 V, $C_L$ = 10 pF



## 4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$)/Bus Acknowledge ($\overline{BUSAK}$)




| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $\overline{BUSRQ}$ set-up time to CLK | $t_{BRC}$ | 120 | | 120 | | 120 | | ns |
| CLK → $\overline{BUSAK}$ falling edge | $t_{CBAL}$ | | 1.5x + 120 | | 240 | | 195 | ns |
| CLK → $\overline{BUSAK}$ rising edge | $t_{CBAH}$ | | 0.5x + 40 | | 80 | | 65 | ns |
| Output buffer off to $\overline{BUSAK}$ | $t_{ABA}$ | 0 | 80 | 0 | 80 | 0 | 80 | ns |
| $\overline{BUSAK}$ to output buffer on | $t_{BAA}$ | 0 | 80 | 0 | 80 | 0 | 80 | ns |

Note 1: The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2: This line only shows the output buffer is off-state.
It doesn't indicate the signal level is fixed.
Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level-fix will be delayed.
The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.

## 5. Package Dimensions

P-LQFP100-1414-0.50F

Unit: mm