TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L Series

TMP93CM40

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2, RUN is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low Voltage/Low Power

CMOS 16-Bit Microcontroller

TMP93CM40F

1. Outline and Device Characteristics

The TMP93CM40 is high-speed, advanced 16-bit microcontroller developed for controlling medium to large-scale equipment. They enable low voltage and low-power-consumption operation.

The TMP93CM40 is housed in 100-pin flat packages.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)
- TLCS-90 instruction mnemonic upward compatible
- 16-Mbyte linear address space
- General-purpose registers, register bank system
- 16-bit multiplication, 16-bit division, bit transfer and bit manipulation instructions
- Micro DMA: 4 channels (1.6 μs per 2 bytes at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal RAM: 2 Kbytes
Internal ROM: 32 Kbytes

(4) External memory expansion
- Can be expanded up to 16 Mbytes (for both programs and data).
- AM8/$\overline{\text{AM16}}$ pin (select the external data bus width)
- Can mix 8- and 16-bit external data buses. (Dynamic bus sizing)

(5) 8-bit timer: 2 channels

(6) 8-bit PWM timer: 2 channels

(7) 16-bit timer: 2 channels

(8) 4-bit pattern generator: 2 channels

(9) Serial interface: 2 channels

(10) 10-bit AD converter: 8 channels

(11) Watchdog timer

(12) Chip select and wait controller: 3 blocks

(13) Interrupt functions: 29

- 9 CPU interrupts (SWI instruction, and illegal instruction)
- 14 internal interrupts
- 6 external interrupts

7-level priority can be set.

(14) I/O ports: 79

(15) Standby function: 4 HALT modes (RUN, IDLE2, IDLE1, STOP)

(16) Clock gear function

- Dual clock operation
- Clock gear: High-frequency clock can be changed from fc to fc/16.

(17) Wide range of operating voltage

- Vcc = 2.7 to 5.5 V

(18) Package

Type No.	Package
TMP93CM40F	P-QFP100-1414-0.50

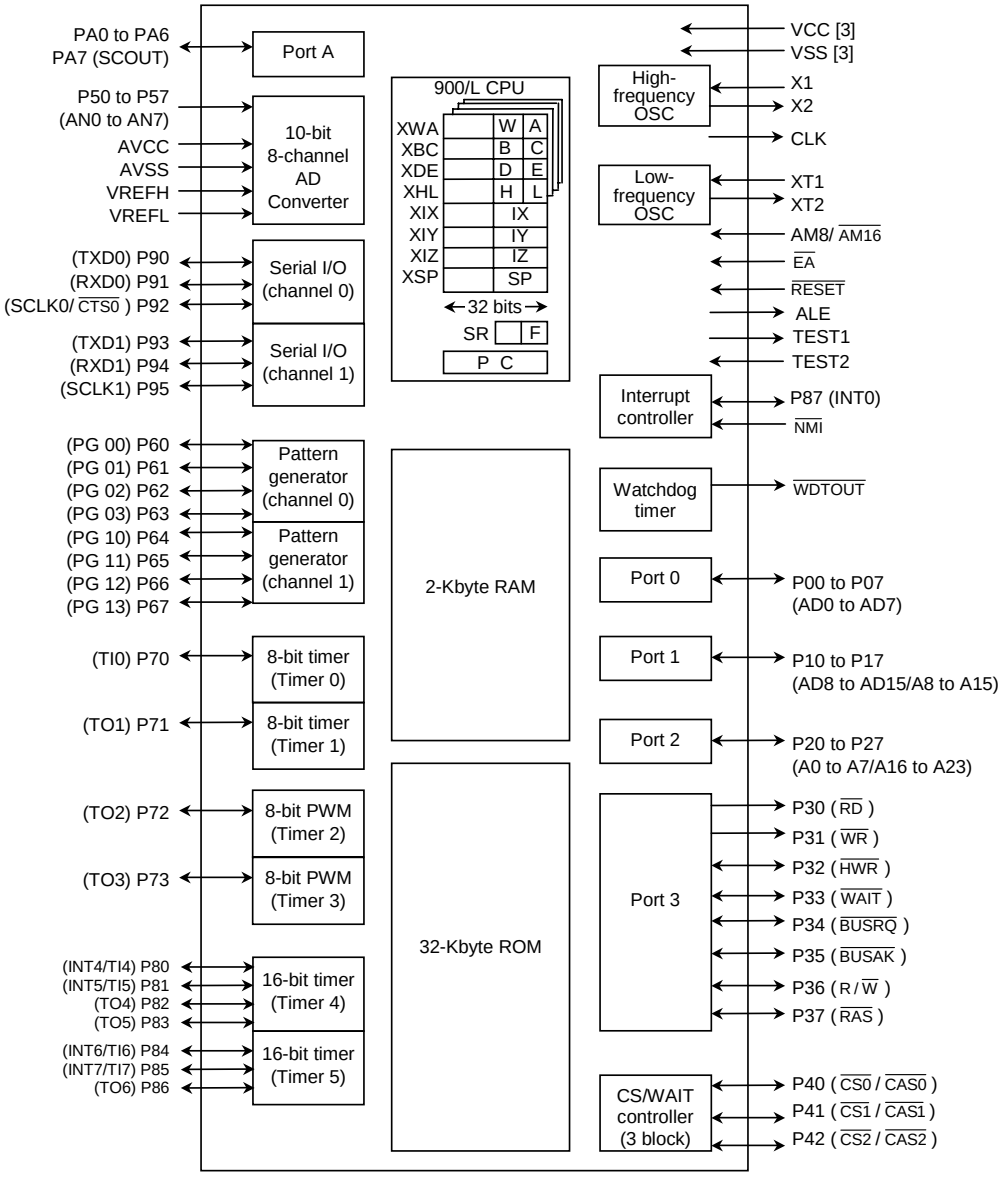


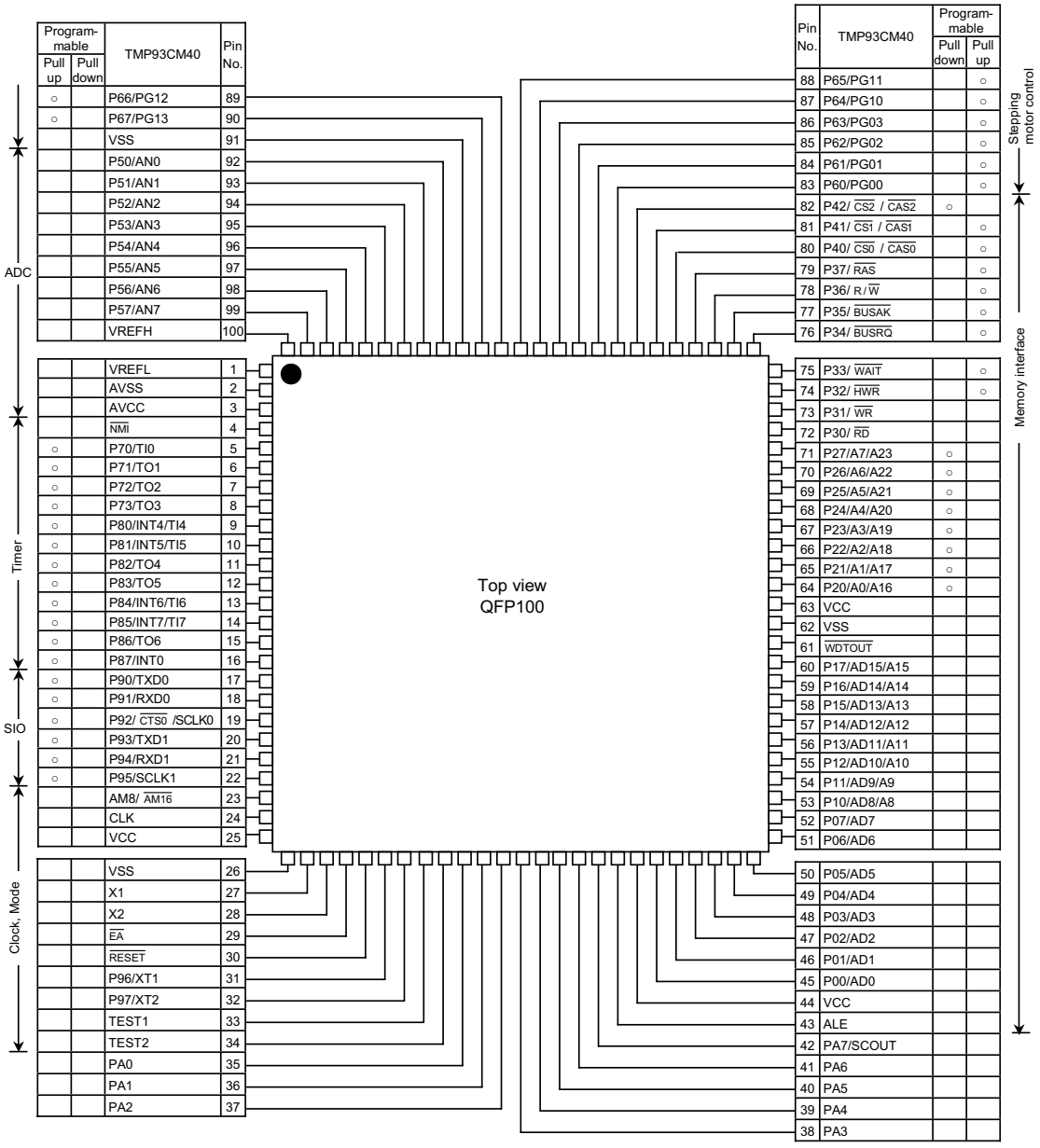
Figure 1.1 TMP93CM40 Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CM40, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CM40F.



Pin No.	TMP93CM40	Programmable Pull up	Programmable Pull down
89	P66/PG12	○	
90	P67/PG13	○	
91	VSS		
92	P50/AN0		
93	P51/AN1		
94	P52/AN2		
95	P53/AN3		
96	P54/AN4		
97	P55/AN5		
98	P56/AN6		
99	P57/AN7		
100	VREFH		
1	VREFL		
2	AVSS		
3	AVCC		
4	$\overline{NMI}$		
5	P70/TI0	○	
6	P71/TO1	○	
7	P72/TO2	○	
8	P73/TO3	○	
9	P80/INT4/TI4	○	
10	P81/INT5/TI5	○	
11	P82/TO4	○	
12	P83/TO5	○	
13	P84/INT6/TI6	○	
14	P85/INT7/TI7	○	
15	P86/TO6	○	
16	P87/INT0	○	
17	P90/TXD0	○	
18	P91/RXD0	○	
19	P92/ $\overline{CTS0}$ /SCLK0	○	
20	P93/TXD1	○	
21	P94/RXD1	○	
22	P95/SCLK1	○	
23	AM8/ $\overline{AM16}$		
24	CLK		
25	VCC		
26	VSS		
27	X1		
28	X2		
29	$\overline{EA}$		
30	$\overline{RESET}$		
31	P96/XT1		
32	P97/XT2		
33	TEST1		
34	TEST2		
35	PA0		
36	PA1		
37	PA2		
38	PA3		
39	PA4		
40	PA5		
41	PA6		
42	PA7/SCOUT		
43	ALE		
44	VCC		
45	P00/AD0		
46	P01/AD1		
47	P02/AD2		
48	P03/AD3		
49	P04/AD4		
50	P05/AD5		
51	P06/AD6		
52	P07/AD7		
53	P10/AD8/A8		
54	P11/AD9/A9		
55	P12/AD10/A10		
56	P13/AD11/A11		
57	P14/AD12/A12		
58	P15/AD13/A13		
59	P16/AD14/A14		
60	P17/AD15/A15		
61	$\overline{WDTOUT}$		
62	VSS		
63	VCC		
64	P20/A0/A16	○	
65	P21/A1/A17	○	
66	P22/A2/A18	○	
67	P23/A3/A19	○	
68	P24/A4/A20	○	
69	P25/A5/A21	○	
70	P26/A6/A22	○	
71	P27/A7/A23	○	
72	P30/ $\overline{RD}$		
73	P31/ $\overline{WR}$		
74	P32/ $\overline{HWR}$		○
75	P33/ $\overline{WAIT}$		○
76	P34/ $\overline{BUSRQ}$		○
77	P35/ $\overline{BUSAK}$		○
78	P36/ R/ $\overline{W}$		○
79	P37/ $\overline{RAS}$		○
80	P40/ $\overline{CS0}$ / $\overline{CAS0}$		○
81	P41/ $\overline{CS1}$ / $\overline{CAS1}$		○
82	P42/ $\overline{CS2}$ / $\overline{CAS2}$	○	
83	P60/PG00		○
84	P61/PG01		○
85	P62/PG02		○
86	P63/PG03		○
87	P64/PG10		○
88	P65/PG11		○

Figure 2.1.1 Pin Assignment (100-pin QFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 to Table 2.2.4 show pin names and functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin Names	Number of Pins	I/O	Functions
P00 to P07	8	I/O	Port 0: I/O port that allows I/O to be selected at the bit level.
AD0 to AD7		3-state	Address and data (lower): Bits 0 to 7 for address and data bus.
P10 to P17	8	I/O	Port 1: I/O port that allows I/O to be selected at the bit level.
AD8 to AD15		3-state	Address and data (upper): Bits 8 to 15 for address and data bus.
A8 to A15		Output	Address: Bits 8 to 15 for address bus.
P20 to P27	8	I/O	Port 2: I/O port that allows to be selected at the bit level (with pull-down resistor).
A0 to A7		Output	Address: Bits 0 to 7 for address bus.
A16 to A23		Output	Address: Bits 16 to 23 for address bus.
P30	1	Output	Port 30: Output port.
$\overline{RD}$		Output	Read: Strobe signal for reading external memory.
P31	1	Output	Port 31: Output port.
$\overline{WR}$		Output	Write: Strobe signal for writing data on pins AD0 to AD7.
P32	1	I/O	Port 32: I/O port (with pull-up resistor).
$\overline{HWR}$		Output	High write: Strobe signal for writing data on pins AD8 to AD15.
P33	1	I/O	Port 33: I/O port (with pull-up resistor).
$\overline{WAIT}$		Input	Wait: Pin used to request CPU bus wait.
P34	1	I/O	Port 34: I/O port (with pull-up resistor).
$\overline{BUSRQ}$		Input	Bus request: Signal used to request bus release.
P35	1	I/O	Port 35: I/O port (with pull-up resistor).
$\overline{BUSAK}$		Output	Bus acknowledge: Signal used to acknowledge bus release.
P36	1	I/O	Port 36: I/O port (with pull-up resistor).
R/$\overline{W}$		Output	Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor).
$\overline{RAS}$		Output	Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40	1	I/O	Port 40: I/O port (with pull-up resistor).
$\overline{CS0}$		Output	Chip select 0: Outputs 0 when address is within specified address area.
$\overline{CAS0}$		Output	Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note: This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.2 Pin Names and Functions (2/4)

Pin Names	Number of Pins	I/O	Functions
P41	1	I/O	Port 41: I/O port (with pull-up resistor).
$\overline{CS1}$		Output	Chip select 1: Outputs 0 if address is within specified address area.
$\overline{CAS1}$		Output	Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42	1	I/O	Port 42: I/O port (with pull-down resistor).
$\overline{CS2}$		Output	Chip select 2: Outputs 0 if address is within specified address area.
$\overline{CAS2}$		Output	Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57	8	Input	Port 5: Pin used to input port.
AN0 to AN7		Input	Analog input: Pin used to input to AD converter.
VREFH	1	Input	Pin for reference voltage input to AD converter. (H)
VREFL	1	Input	Pin for reference voltage input to AD converter. (L)
P60 to P63	4	I/O	Port 60 to 63: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor).
PG00 to PG03		Output	Pattern generator ports: 00 to 03.
P64 to P67	4	I/O	Port 64 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor).
PG10 to PG13		Output	Pattern generator ports: 10 to 13.
P70	1	I/O	Port 70: I/O port (with pull-up resistor).
TI0		Input	Timer input 0: Timer 0 input.
P71	1	I/O	Port 71: I/O port (with pull-up resistor).
TO1		Output	Timer output 1: Timer 0 or 1 output.
P72	1	I/O	Port 72: I/O port (with pull-up resistor).
TO2		Output	PWM output 2: 8-bit PWM timer 2 output.
P73	1	I/O	Port 73: I/O port (with pull-up resistor).
TO3		Output	PWM output 3: 8-bit PWM timer 3 output.
P80	1	I/O	Port 80: I/O port (with pull-up resistor).
TI4		Input	Timer input 4: Timer 4 count/capture trigger signal input.
INT4		Input	Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge.
P81	1	I/O	Port 81: I/O port (with pull-up resistor).
TI5		Input	Timer input 5: Timer 4 count/capture trigger signal input.
INT5		Input	Interrupt request pin 5: Interrupt request pin with rising edge.
P82	1	I/O	Port 82: I/O port (with pull-up resistor).
TO4		Output	Timer output 4: Timer 4 output pin.
P83	1	I/O	Port 83: I/O port (with pull-up resistor).
TO5		Output	Timer output 5: Timer 4 output pin.

Table 2.2.3 Pin Names and Functions (3/4)

Pin Names	Number of Pins	I/O	Functions
P84	1	I/O	Port 84: I/O port (with pull-up resistor).
TI6		Input	Timer input 6: Timer 5 count/capture trigger signal input.
INT6		Input	Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge.
P85	1	I/O	Port 85: I/O port (with pull-up resistor).
TI7		Input	Timer input 7: Timer 5 count/capture trigger signal input.
INT7		Input	Interrupt request pin 7: Interrupt request pin with rising edge.
P86	1	I/O	Port 86: I/O port (with pull-up resistor).
TO6		Output	Timer output 6: Timer 5 output pin.
P87	1	I/O	Port 87: I/O port (with pull-up resistor).
INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge.
P90	1	I/O	Port 90: I/O port (with pull-up resistor).
TXD0		Output	Serial send data 0.
P91	1	I/O	Port 91: I/O port (with pull-up resistor).
RXD0		Input	Serial receive data 0.
P92	1	I/O	Port 92: I/O port (with pull-up resistor).
$\overline{CTS0}$		Input	Serial data send enable 0. (Clear to send)
SCLK0		I/O	Serial Clock I/O 0.
P93	1	I/O	Port 93: I/O port (with pull-up resistor).
TXD1		Output	Serial send data 1.
P94	1	I/O	Port 94: I/O port (with pull-up resistor).
RXD1		Input	Serial receive data 1.
P95	1	I/O	Port 95: I/O port (with pull-up resistor).
SCLK1		I/O	Serial clock I/O 1.
PA0 to PA6	7	I/O	Port A0 to A6: I/O port.
PA7	1	I/O	Port A7: I/O port.
SCOUT		Output	System clock output: outputs f_{FPH} or f_{SYS} clock.
$\overline{WDTOUT}$	1	Output	Watchdog timer output pin.
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges.
CLK	1	Output	Clock output: Outputs [$f_{SYS} \div 2$] clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{EA}$	1	Input	External access: The VCC pin should be connected.

Table 2.2.4 Pin Names and Functions (4/4)

Pin Names	Number of Pins	I/O	Functions
AM8/ $\overline{AM16}$	1	Input	Address mode: Selects external data bus width. The VCC pin should be connected. The data bus width for external access is set by the chip select/wait control register, port 1 control register.
ALE	1	Output	Address latch enable. Can be disabled for reducing noise.
$\overline{RESET}$	1	Input	Reset: Initializes TMP93CM40. (with pull-up resistor)
X1/X2	2	Input/Output	High frequency oscillator connecting pin.
P96 XT1	1	I/O Input	Port 96: I/O port. (Open-drain output) Low frequency oscillator connecting pin.
P97 XT2	1	I/O Output	Port 97: I/O port. (Open-drain output) Low-frequency oscillator connecting pin.
TEST1/TEST2	2	Output /Input	TEST1 should be connected with TEST2 pin. Do not connect to any other pins.
VCC	3		Power supply pin. (All VCC pins should be connected with the power supply pin.)
VSS	3		GND pin (0 V). (All VSS pins should be connected with GND (0 V).)
AVCC	1		Power supply pin for AD converter.
AVSS	1		GND pin for AD converter (0 V).

Note: All pins that have built-in pull-up/pull-down resistors (other than the $\overline{RESET}$ pin) can be disconnected from the built-in pull-up/pull-down resistor by software.

3. Operation

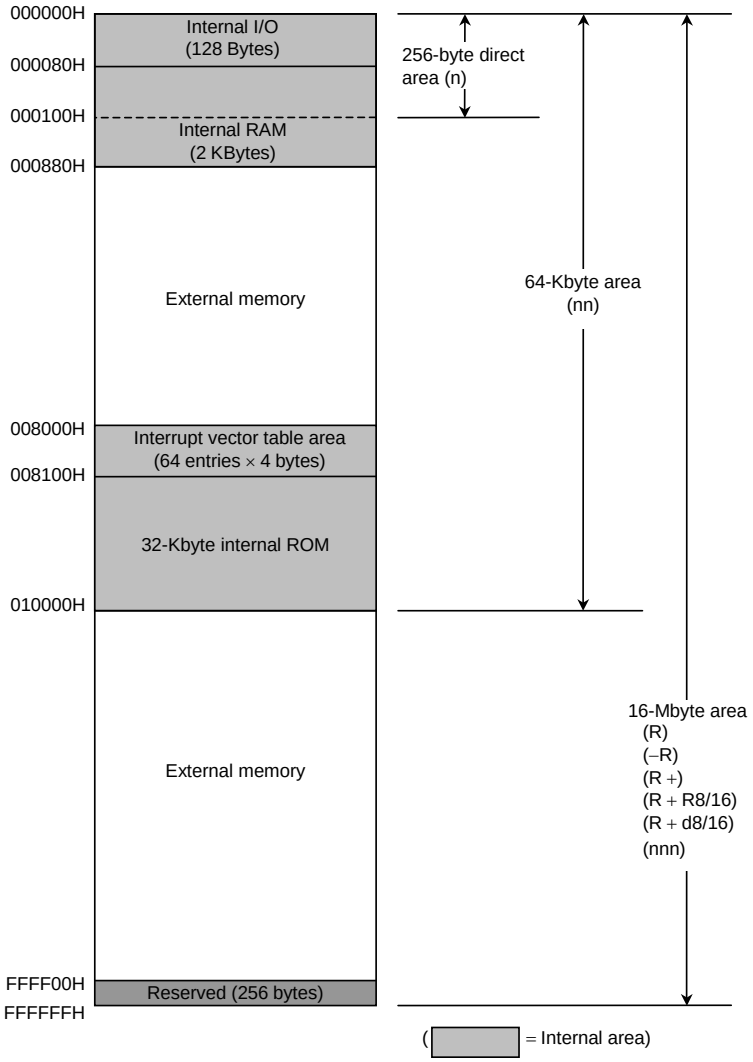
This section describes the functions and basic operation of all blocks of the TMP93CM40 devices.

3.1 CPU

The TMP93CM40 has a built-in high performance 16-bit CPU (900/L CPU). (For a description of this CPU's operation, see the sub section TLCS-900/L CPU in the previous section.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CM40.



Note: The 256-byte area from FFFF00H to FFFFFFH cannot be used.

Figure 3.2.1 Memory Map

4. Electrical Characteristics

"X" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of "X" changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear = 1/fc (SYSCR1<SYSCK, GEAR2:0> = "0000")

4.1 Maximum Ratings (TMP93CM40F)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 6.5	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output current (total)	ΣI_{OL}	120	mA
Output current (total)	ΣI_{OH}	−80	mA
Power dissipation (Ta = 85°C)	P_D	600	mW
Soldering temperature (10 s)	T_{SOLDER}	260	°C
Storage temperature	T_{STG}	−65 to 150	°C
Operating temperature	T_{OPR}	−40 to 85	°C

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Power supply voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS} = 0$ V)		V_{CC}	fc = 4 to 16 MHz fs = 30 to 34 kHz (Ta = −40 to 85°C)	4.5		5.5	V
			fc = 4 to 20 MHz fs = 30 to 34 kHz (Ta = −20 to 70°C)				
			fc = 4 to 10 MHz fs = 30 to 34 kHz (Ta = −40 to 85°C)	2.7 (Note 2)			
Input low voltage	AD0 to AD15	V_{IL}	$V_{CC} \geq 4.5$ V	−0.3		0.8	V
			$V_{CC} < 4.5$ V			0.6	
	Port 2 to port A (except P87)	V_{IL1}	V_{CC} = 2.7 to 5.5 V			0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, INT0	V_{IL2}				0.25 V_{CC}	
	$\overline{EA}$, AM8/ $\overline{AM16}$	V_{IL3}				0.3	
	X1, Port 5	V_{IL4}				0.2 V_{CC}	
Input high voltage	AD0 to AD15	V_{IH}	$V_{CC} \geq 4.5$ V	2.2		V_{CC} + 0.3	
			$V_{CC} < 4.5$ V	2.0			
	Port 2 to port A (except P87)	V_{IH1}	V_{CC} = 2.7 to 5.5 V	0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, INT0	V_{IH2}		0.75 V_{CC}			
	$\overline{EA}$, AM8/ $\overline{AM16}$	V_{IH3}		V_{CC} − 0.3			
	X1	V_{IH4}		0.8 V_{CC}			
Output low voltage		V_{OL}	I_{OL} = 1.6 mA (V_{CC} = 2.7 to 5.5 V)			0.45	V
Output high voltage		V_{OH1}	I_{OH} = −400 μA (V_{CC} = 3 V ± 10%)	2.4			
		V_{OH2}	I_{OH} = −400 μA (V_{CC} = 5 V ± 10%)	4.2			

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: The operation of the AD converter is guaranteed at 5 V ± 10%.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Darlington drive current (8 output pins max)	I_{DAR} (Note 2)	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ (only when V_{CC} = 5 V ± 10%)	−1.0		−3.5	mA
Input leakage current	I_{LI}	0.0 ≤ V_{IN} ≤ V_{CC}		0.02	±5	μA
Output leakage current	I_{LO}	0.2 ≤ V_{IN} ≤ V_{CC} − 0.2		0.05	±10	
Power down voltage (at STOP, RAM back-up)	V_{STOP}	V_{IL2} = 0.2 V_{CC}, V_{IL2} = 0.8 V_{CC}	2.0		6.0	V
$\overline{RESET}$ pull-up resistor	R_{RST}	V_{CC} = 5 V ± 10%	50		150	kΩ
		V_{CC} = 3 V ± 10%	80		200	
Pin capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}		0.4	1.0		V
Programmable pull-down resistor	R_{KL}	V_{CC} = 5 V ± 10%	10		80	kΩ
		V_{CC} = 3 V ± 10%	30		150	
Programmable pull-up resistor	R_{KH}	V_{CC} = 5 V ± 10%	50		150	
		V_{CC} = 3 V ± 10%	100		300	
NORMAL (Note 3)	I_{CC}	V_{CC} = 5 V ± 10% fc = 20 MHz		19	25	mA
NORMAL2 (Note 4)				24	30	
RUN				17	25	
IDLE2				10	15	
IDLE1				3.5	5	
NORMAL (Note 3)		V_{CC} = 3 V ± 10% fc = 10 MHz (Typ: V_{CC} = 3.0 V)		5.5	8	mA
NORMAL2 (Note 4)				8.5	11	
RUN				4.0	7	
IDLE2				2.5	4	
IDLE1				0.7	1.2	
SLOW (Note 3)		V_{CC} = 3 V ± 10% fs = 32.768 kHz (Typ: V_{CC} = 3.0 V)		20	35	μA
RUN				16	30	
IDLE2				10	20	
IDLE1				5	15	
STOP		V_{CC} = 2.7 to 5.5 V		0.2	10	μA

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: I_{DAR} is guaranteed for up to eight ports.

Note 3: I_{CC} measurement conditions (NORMAL, SLOW): Only CPU is operational; output pins are open and input pins are fixed.

Note 4: I_{CC} measurement conditions (NORMAL 2): All functions are operational; output pins are open and input pins are fixed.

4.3 AC Electrical Characteristics

(1) $V_{CC} = 5\ V \pm 10\%$

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. period (= x)	t_{OSC}	50	31250	62.5		50		ns
2	CLK pulse width	t_{CLK}	2x – 40		85		60		ns
3	A0 to A23 fall → CLK hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK valid → A0 to A 23 hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to A15 valid → ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall → A0 to A15 hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE high pulse width	t_{LL}	x – 40		23		10		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ALC}	x – 25		38		25		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to A23 valid → $\overline{WAIT}$ input $\left[\begin{smallmatrix}(1+N)\ WAIT\\ mode\end{smallmatrix}\right]$	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to A15 valid → $\overline{WAIT}$ input $\left[\begin{smallmatrix}(1+N)\ WAIT\\ mode\end{smallmatrix}\right]$	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold $\left[\begin{smallmatrix}(1+N)\ WAIT\\ mode\end{smallmatrix}\right]$	t_{CW}	2.0x + 0		125		100		ns
25	A0 to A23 valid → Port input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to A23 valid → Port hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise → Port valid	t_{CP}		200		200		200	ns
28	A0 to A23 valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x – 40		23		10		ns
29	A0 to A15 valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x – 15		16		10		ns
30	$\overline{RAS}$ fall → D0 to D15 input	t_{RAC}		2.5x – 70		86		55	ns
31	$\overline{RAS}$ fall → A0 to A15 hold	t_{RAH}	0.5x – 15		16		10		ns
32	$\overline{RAS}$ low pulse width	t_{RAS}	2.0x – 40		85		60		ns
33	$\overline{RAS}$ high pulse width	t_{RP}	2.0x – 40		85		60		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x – 40		23		10		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		6		0		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		23		10		ns
37	$\overline{CAS}$ fall → D0 to D15 input	t_{CAC}		1.5x – 65		29		10	ns
38	$\overline{CAS}$ low pulse width	t_{CAS}	1.5x – 30		64		40		ns

AC measuring condition

- Output level: High 2.2 V/Low 0.8 V, $C_L = 50$ pF
  (However, $C_L = 100$ pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC} /Low 0.2 × V_{CC} (except AD0 to AD15)

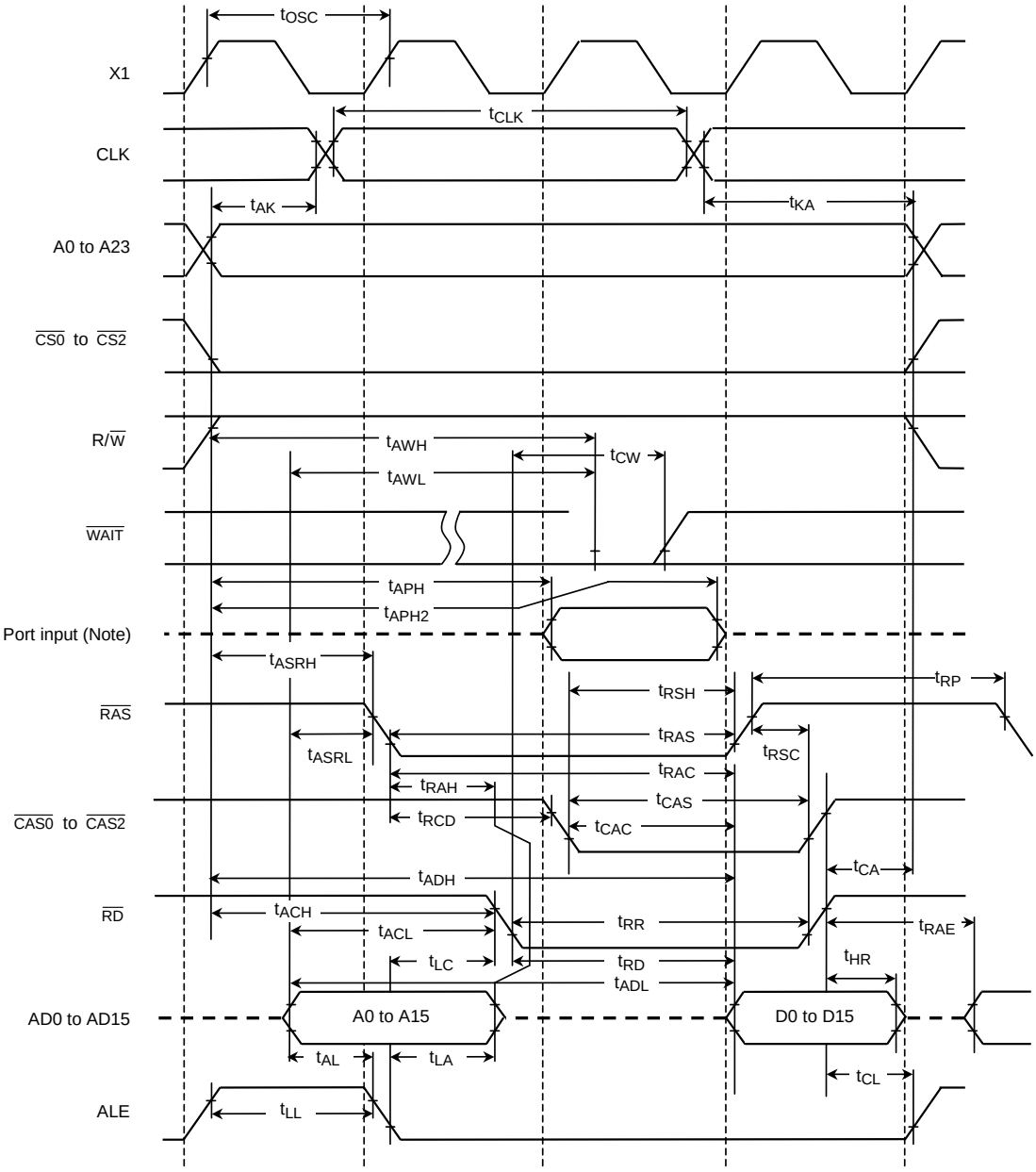
(2) V_{CC} = 3 V ± 10% (TMP93CM40F is guaranteed up to 10 MHz operation.)

No.	Parameter	Symbol	Variable		10 MHz		Unit
			Min	Max	Min	Max	
1	Osc. period (= x)	t_{OSC}	100	31250	100		ns
2	CLK pulse width	t_{CLK}	2x – 40		160		ns
3	A0 to A23 fall → CLK hold	t_{AK}	0.5x – 30		20		ns
4	CLK valid → A0 to A 23 hold	t_{KA}	1.5x – 80		70		ns
5	A0 to A15 valid → ALE fall	t_{AL}	0.5x – 35		15		ns
6	ALE fall → A0 to A15 hold	t_{LA}	0.5x – 35		15		ns
7	ALE high pulse width	t_{LL}	x – 60		40		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	t_{LC}	0.5x – 35		15		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise	t_{CL}	0.5x – 40		10		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ALC}	x – 50		50		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5x – 50		100		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold	t_{CA}	0.5x – 40		10		ns
13	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 110		190	ns
14	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5x – 125		225	ns
15	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0x – 115		85	ns
16	$\overline{RD}$ low pulse width	t_{RR}	2.0x – 40		160		ns
17	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	x – 25		75		ns
19	$\overline{WR}$ low pulse width	t_{WW}	2.0x – 40		160		ns
20	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 120		80		ns
21	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	0.5x – 40		10		ns
22	A0 to A23 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode]	t_{AWH}		3.5x – 130		220	ns
23	A0 to A15 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode]	t_{AWL}		3.0x – 100		200	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold [(1 + N) WAIT mode]	t_{CW}	2.0x + 0		200		ns
25	A0 to A23 valid → Port input	t_{APH}		2.5x – 245		5	ns
26	A0 to A23 valid → Port hold	t_{APH2}	2.5x + 50		300		ns
27	$\overline{WR}$ rise → Port valid	t_{CP}		200		200	ns
28	A0 to A23 valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x – 60		40		ns
29	A0 to A15 valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x – 40		10		ns
30	$\overline{RAS}$ fall → D0 to D15 input	t_{RAC}		2.5x – 90		160	ns
31	$\overline{RAS}$ fall → A0 to A15 hold	t_{RAH}	0.5x – 25		25		ns
32	$\overline{RAS}$ low pulse width	t_{RAS}	2.0x – 40		160		ns
33	$\overline{RAS}$ high pulse width	t_{RP}	2.0x – 40		160		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x – 55		45		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		25		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		60		ns
37	$\overline{CAS}$ fall → D0 to D15 input	t_{CAC}		1.5x – 120		30	ns
38	$\overline{CAS}$ low pulse width	t_{CAS}	1.5x – 40		110		ns

AC measuring condition

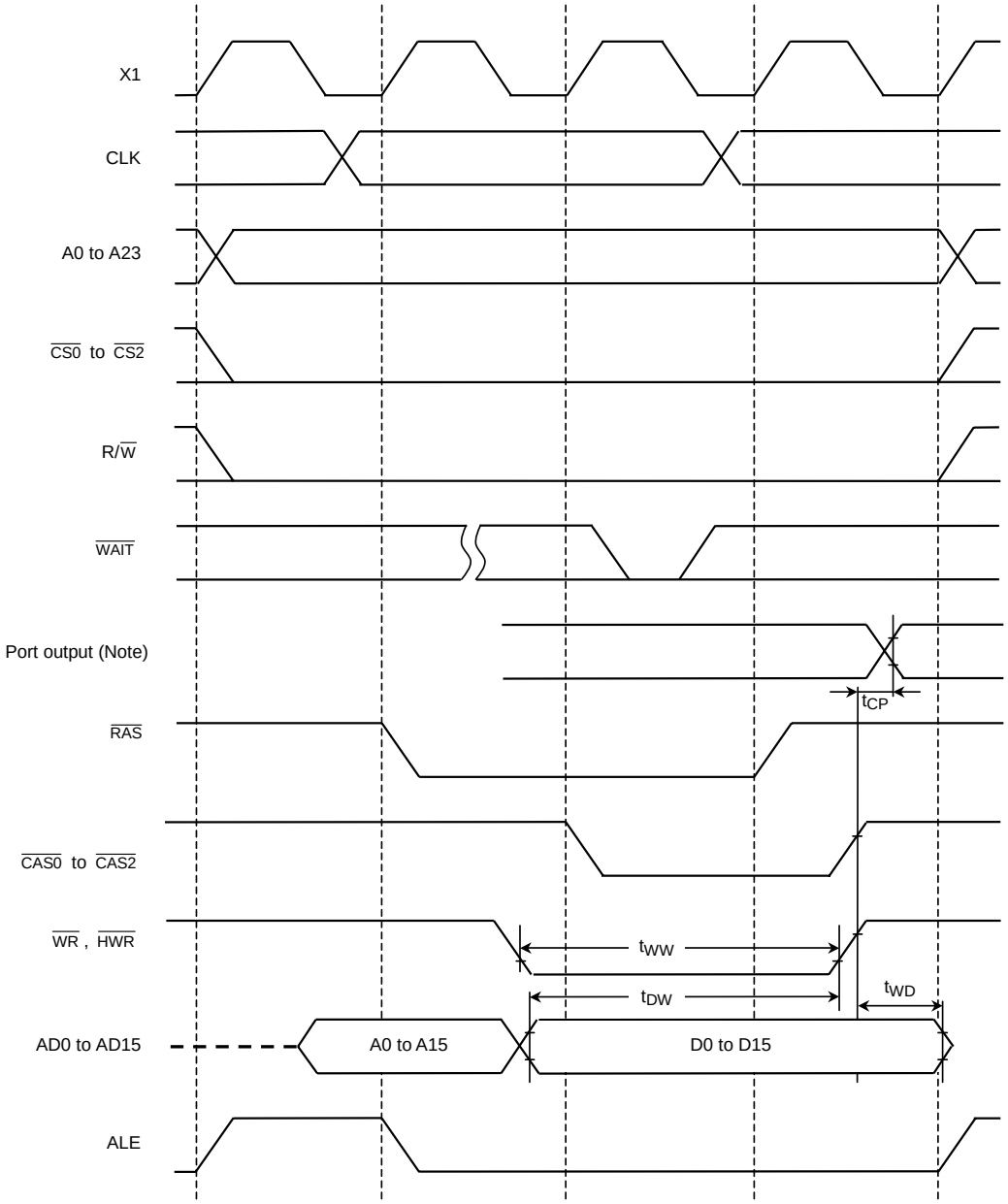
- Output level: High 0.7 × V_{CC}/Low 0.3 × V_{CC}, C_L = 50 pF
- Input level: High 0.9 × V_{CC}/Low 0.1 × V_{CC}

(1) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Min	Typ.	Max	Unit
Analog reference voltage (+)	V_{REFH}	V_{CC} − 0.2 V	V_{CC}	V_{CC}	V
Analog reference voltage (−)	V_{REFL}	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	V_{AIN}	V_{REFL}		V_{REFH}	
Analog current for analog reference voltage V_{CC} = 5 V ± 10% <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)		0.5	1.5	mA
V_{CC} = 5 V ± 10% <VREFON> = 0			0.02	5.0	μA
Error (not including quantizing errors)	–		±3.0	±6	LSB

Note 1: $1LSB = (V_{REFH} - V_{REFL}) / 2^{10}$ [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

Note 4: The operation of this AD converter is guaranteed at 5 V ± 10%.

4.5 Serial Channel Timing

(1) I/O interface mode

a. SCLK input mode

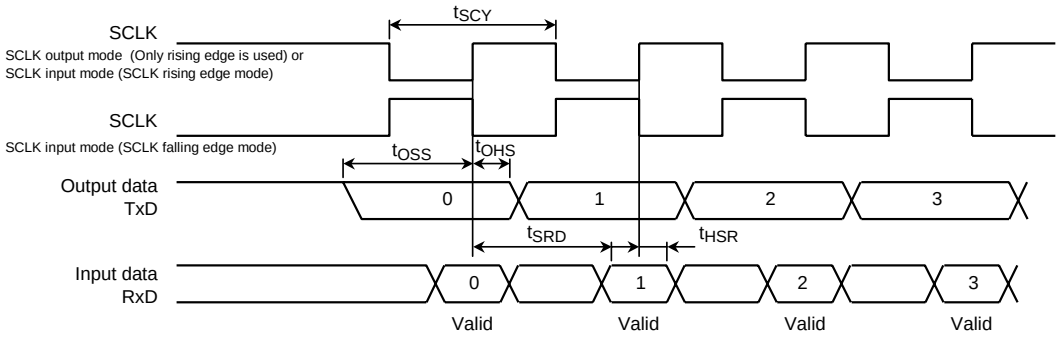
Parameter	Symbol	Variable		32.768 kHz (Note 1)		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16x		488 μs		1600		800		ns
Output data → Rising edge or falling edge (Note 2) of SCLK	t_{OSS}	$t_{SCY}/2 - 5x - 50$		91.5 μs		250		100		ns
SCLK rising edge or falling edge (Note 2) → Output data hold	t_{OHS}	$5x - 100$		152 μs		400		150		ns
SCLK rising edge or falling edge (Note 2) → Input data hold	t_{HSR}	0		0		0		0		ns
SCLK rising edge or falling edge (Note 2) → Effective data input	t_{SRD}		$t_{SCY} - 5x - 100$		336 μs		1000		450	ns

Note 1: System clock is fs, or input clock to prescaler is divisor clock of fs.

Note 2: The rising edge is used in SCLK rising mode.
The falling edge is used SCLK falling mode.

b. SCLK output mode

Parameter	Symbol	Variable		32.768 kHz (Note)		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488	250 ms	1.6	819.2	0.8	409.6	μs
Output data → SCLK rising edge	t_{OSS}	$t_{SCY} - 5X - 150$		427 μs		1250		550		ns
SCLK rising edge → Output data hold	t_{OHS}	$2x - 80$		60 μs		120		20		ns
SCLK rising edge → Input data hold	t_{HSR}	0		0		0		0		ns
SCLK rising edge → Effective data input	t_{SRD}		$t_{SCY} - 2x - 150$		428 μs		1250		550	ns



Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6 and TI7)

Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock cycle	t_{VCK}	8X + 100		900		500		ns
Low level clock pulse width	t_{VCKL}	4X + 40		440		240		ns
High level clock pulse width	t_{VCKH}	4X + 40		440		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 low level pulse width	t_{INTAL}	4X		400		200		ns
$\overline{NMI}$, INT0 high level pulse width	t_{INTAH}	4X		400		200		ns

(2) INT4 to 7 interrupt, capture

The INT4 to 7 input pulse width depends on the CPU operation clock and timer (9-bit prescaler). The following shows the pulse width for each clock.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT4 to 7 low-level pulse width)		t_{INTBH} (INT4 to 7 high-level pulse width)		Unit
		Variable	20 MHz	Variable	20 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{IFPH})	8X + 100	500	8X + 100	500	ns
	01 (fs)	8XT + 0.1	244.3	8XT + 0.1	244.3	μs
	10 (fc/16)	128X + 0.1	6.5	128X + 0.1	6.5	
1 (fs) (Note 2)	00 (f_{IFPH})	8XT + 0.1	244.3	8XT + 0.1	244.3	
	01 (fs)					

Note 1: XT represents the frequency of the low-frequency clock fs. It is calculated at fs = 32.768 kHz.

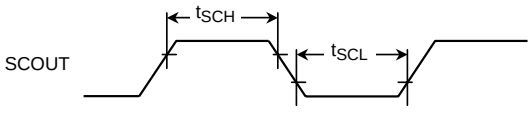
Note 2: When using fs as the system clock, fc/16 cannot be selected as the prescaler clock.

4.8 SCOUT Pin AC Characteristics

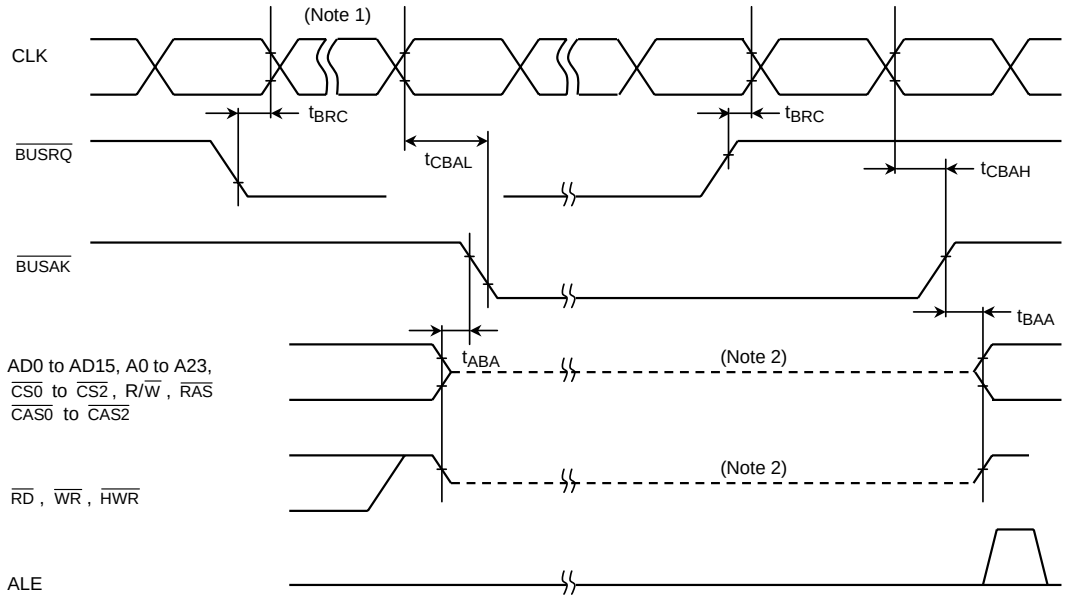
Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
High-level pulse width V_{CC} = 5 V ± 10%	t_{SCH}	0.5X – 10		40		15		ns
High-level pulse width V_{CC} = 3 V ± 10%		0.5X – 20		30		–	–	
Low-level pulse width V_{CC} = 5 V ± 10%	t_{SCL}	0.5X – 10		40		15		ns
Low-level pulse width V_{CC} = 3 V ± 10%		0.5X – 20		30		–	–	

Measurement condition

- Output level: High 2.2 V/Low 0.8 V, C_L = 10pF



4.9 Timing Chart for Bus Request ($\overline{BUSRQ}$)/Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ set-up time to CLK	t_{BRC}	120		120		120		ns
CLK → $\overline{BUSAK}$ falling edge	t_{CBAL}		0.5x + 120		270		195	ns
CLK → $\overline{BUSAK}$ rising edge	t_{CBAH}		0.5x + 40		90		65	ns
Output buffer off to $\overline{BUSAK}$ ↘	t_{ABA}	0	80	0	80	0	80	ns
$\overline{BUSAK}$ ↗ to output buffer on	t_{BAA}	0	80	0	80	0	80	ns

Note 1: Even if the $\overline{BUSRQ}$ signal goes low, the bus will not be released while the $\overline{WAIT}$ signal is low. The bus will only be released when $\overline{BUSRQ}$ goes low while $\overline{WAIT}$ is high.

Note 2: This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Recommended Oscillator

The TMP93CM40 is evaluated with various resonators. The evaluation results are displayed below to enable appropriate selection for any given application.

Note: The load capacitance of the resonator consists of the load capacitors C1 and C2 which are to be connected, and the floating capacitance of the target board.
Even if the specified values of C1 and C2 are used, there is a possibility that the oscillator will malfunction due to varying load capacitance on the target boards. Hence the oscillator's wiring patterns on the board should be designed to be as short as possible.
It is recommended that evaluation of the resonators be conducted on the target board.

(1) Examples of resonator connection

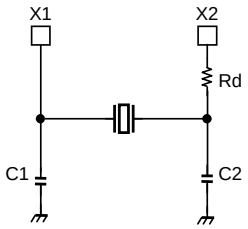


Figure 1: Example of High-frequency Resonator Connection

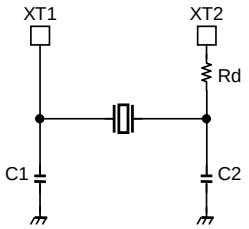


Figure 2: Example of Low-frequency Resonator Connection

(2) Ceramic resonator: Murata Manufacturing. Co., Ltd. (Note 1)

Ta = −20 to 80°C

Parameter	Frequency (MHz)	Recommended Resonator	Recommended Value			V_{CC} [V]
			C_1 [pF]	C_2 [pF]	R_d [kΩ]	
High-frequency oscillation	4.00	CSA4.00MGU	30	30	0	2.7 to 5.5
		CST4.00MGWU	(30) (Note 2)	(30) (Note 2)		
	10.00	CSA10.00MTZ093	30	30		
		CST10.00MTW093	(30) (Note 2)	(30) (Note 2)		
	16.00	CSA16.00MXZ040	5	5		4.5 to 5.5
	20.00	CSA20.00MXZ040	5	5		

Note 1: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
For up-to-date information, please refer to the following URL:
http://www.murata.com/

Note 2: For built-in condenser type

5. Package Dimensions

P-QFP100-1414-0.50

Unit: mm