

32-bit Microcontroller

CMOS

FR60 MB91319 Series

MB91F318A/FV319A

■ DESCRIPTION

The MB91319 series is the microcontrollers which use a high-performance 32-bit RISC-CPU and contains various types of I/O resources for the embedded control that requires high-performance and high-speed CPU processing.

It is suitable for the embedded control in TV or PDP, requiring high-performance CPU processing power.

This product is one of the FR60 family based on the FR30/40 family CPU with enhanced bus access. It is applicable to faster-speed application.

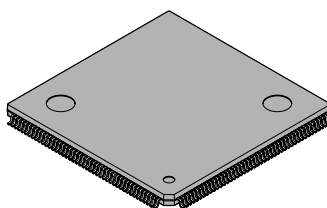
■ FEATURE

- FR CPU
 - 32-bit RISC, load/store architecture with a five-stage pipeline
 - Operating frequency : 40 MHz (Use of PLL : Oscillation 10 MHz)
 - 16-bit fixed length instructions (basic instructions) , 1 instruction per cycle
 - Memory-to-memory transfer, bit manipulation, instruction for barrel shift etc. : Instruction set optimized for embedded applications
 - Function entry/exit instructions, multiple-register load/store instructions : Instructions adapted for high-level languages
 - Register interlock functions: Facilitating coding in assemblers

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■ PACKAGE

176-pin plastic LQFP



(FPT-176P-M07)

MB91319 Series

- Built-in multiplier with instruction-level support
 - 32-bit multiplication with sign : 5 cycles
 - 16-bit multiplication with sign : 3 cycles
 - Interrupt (PC, PS save) : 6 cycles, 16 priority levels
 - Harvard architecture allowing program access and data access to be executed simultaneously
 - Instruction prefetch function implemented by a four-word queue in the CPU
 - Instruction compatible with FR family
- Bus interface
 - This bus interface is used for internal macro IF (USB, OSDC)
 - CS1, CS2, and CS3 areas are connected as following :
 CS1 area : Reserved, CS2 area : USB function, CS3 area : OSDC

- Internal memory

Memory	MB91FV319A	MB91F318A
RAM	64 KB	48 KB
FLASH (for program)	1 MB	1 MB
Memory for font	512 KB FLASH	384 KB MASK ROM

- DMAC (DMA Controller)
 - 5 channels (ch0 and ch1 are connected to USB function.)
 - Two forwarding factors (internal peripheral/software)
 - Specifying of addressing mode 32-bit full address (increased/decreased/fixed)
 - Transfer modes (demand transfer, burst transfer, step transfer, block transfer)
 - Selectable transfer data size : 8, 16, or 32-bit
- Bit search module (for REALOS)
 - Search for the position of the bit “1”/“0”-changed first in one word from the MSB
- Reload timer (including a channel for REALOS)
 - 16-bit timer: 3 channels
 - The internal clock is selectable from 2/8/32 divisions.
- UART
 - Full duplex double buffer
 - 5 channels
 - Selectable parity ON/OFF
 - Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable
 - Internal timer for dedicated baud rate
 - External clock can be used as transfer clock.
 - Assorted error detection functions (for parity, frame, and overrun errors)

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- I²C Interface *
 - 4 channels (built-in bridge function)
 - Master/slave sending and receiving
 - Clock synchronization function
 - Detecting transmitting direction function
 - Bus error detection function
 - Standard mode (Max 100 Kbps) /High speed mode (Max 400 Kbps) supported
 - Built-in FIFO function with 16-byte data each for transmit/receive
 - Arbitration function
 - Slave address and general call address detection function
 - Start condition repeated generation and detection
 - 10-bit/7-bit slave address
- Interrupt controller
 - Total of external interrupt is 5. (one non-maskable interrupt pin ($\overline{\text{NMI}}$) and four normal interrupt pins (INT3 to INT0))
 - Interrupt from internal peripheral
 - Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt
 - At the STOP, available use for Wake Up
- A/D converter
 - 10-bit resolution, 10 channels
 - Serial compared conversion type : Conversion time : approx. 10 μ s
 - Conversion mode (single conversion mode, scan conversion mode)
 - Start-up factor (Software/external trigger)
- PPG
 - 4 channels are incorporated.
 - 16-bit down counter, 16-bit data register with buffer for setting cycles
 - The internal clock is selectable from 1/4/16/64 divisions.
- PWC
 - 1 channel (1 input) is incorporated.
 - 16-bit up counter
 - Easy digital low pass filter
- Multi function timer
 - 4 channels are incorporated.
 - Low pass filter eliminating noise below the clock setting
 - Capable of pulse width measurement according to fine settings using seven types of clock signals
 - Event count function from pin input
 - Interval timer function using seven kinds of clock and external input clock
- USB function
 - Full speed • double buffer of USB2.0 version
 - CONTROL IN/OUT, BULK IN/OUT, INTERRUPT IN

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MB91319 Series

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- OSDC function
 - RGB: each 3 bits (16 colors available among 512 colors)
 - Analog RGB output: Max 50 MHz
 - Digital RGB output: Max 90 MHz
 - A font in 24 × 32 dots can be displayed up to 80 × 32.
 - Two-layered display of MAIN/CC (Font in CC layer is fixed at 18 dots in horizontal axis)
 - 4096 characters at the maximum (including 16 characters for font RAM)

- Closed caption decoder function
 - 2 channels are incorporated.
 - CC decode function
 - ID-1 (480i/480p) decode function

- PLL for video clock
 - 3 PLLs generating dot clock and VBI clock

- Other interval timer
 - 16-bit timer : 3 channels
 - Watchdog timer

- I/O port
 - Max 88 ports

- Other features
 - Built-in oscillation circuit as clock source
 - $\overline{\text{INIT}}$ is prepared as a reset pin.
 - Watchdog timer reset and software reset are also available.
 - Stop mode and sleep mode are supported as low-power consumption mode.
 - Gear function
 - Built-in timebase timer
 - Package : LQFP-176, 0.5mm pitch, 24 mm × 24 mm
 - CMOS technology : 0.25 μm (EVA, FLASH)
 - Power supply voltage : 3.3 V \pm 0.3 V, 2.5 V \pm 0.2 V 2-power supply

- * : "Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips."

PIN ASSIGNMENT

(TOP VIEW)

	176	VSYNC		132	P02/SCK4/TIN2
	175	DCKI		131	P01/SO4/TIN1
	174	DCKO		130	P00/SI4/TINO
	173	FH		129	P74
	172	VOB1		128	P73
	171	VOB2		127	P72
	170	VDDI		126	P71
	169	R2		125	P70
	168	R1		124	VDDE
	167	R0		123	VSS
	166	G2		122	VDDI
	165	G1		121	P57
	164	G0		120	P56
	163	B2		119	P55
	162	B1		118	P54
	161	B0		117	P53
	160	UDP		116	P52/SCK3
	159	UDM		115	P51/SO3
	158	VDDE		114	P50/SI3
	157	X0B		113	P47/SCL2
	156	VSS		112	P46/SO2
	155	X1B		111	P45/SI2
	154	VDDI		110	P44/SDA4
	153	PB7		109	P43/SDA3
	152	PB6		108	P42/SCL4
	151	PB5		107	P41/SCL3
	150	PB4		106	P40/SDA2
	149	PB3		105	P37/SCL2
	148	PB2		104	P36/TRG3
	147	PB1		103	P35/TRG2
	146	PB0		102	P34/TRG1
	145	P17		101	P33/TRG0
	144	P16/ATRQ		100	NMI
	143	P15/PPG3		99	PA2/INT3
	142	P14/PPG2		98	PA1/INT2
	141	P13/PPG1		97	PA0/INT1
	140	P12/PPG0		96	VDDI
	139	P11/TMO3		95	X1A
	138	P10/TMO2		94	VSS
	137	P07/TMO1		93	X0A
	136	P06/TMO0		92	VDDE
	135	P05/TO2		91	P97/INT0
	134	P04/TO1		90	P96/TMI3
	133	P03/TO0		89	P95/TMI2
HSYNC1	1		88	P94/TMI1	
HSYNC2	2		87	P93/TMI0	
HSYNC3	3		86	P92/RIN	
VDDE	4		85	P91/SCK1	
VSS	5		84	P90/SO1	
VGS1/VC1	6		83	P87/SI1	
CPO1	7		82	P86/SCK0	
VSSP1	8		81	P85/SO0	
VDDP1	9		80	P84/SI0	
VGS2/VC2	10		79	P83/SDA1	
CPO2	11		78	P82/SCL1	
VSSP2	12		77	P81/SDA0	
VDDP2	13		76	P80/SCL0	
VGS3/VC3	14		75	NIT	
CPO3	15		74	MD3	
VSSP3	16		73	MD2	
VDDP3	17		72	MD1	
VDDR	18		71	MDO	
VREF	19		70	ICD3	
VR0	20		69	ICD2	
ROUT	21		68	ICD1	
VSSR	22		67	ICD0	
VDDG	23		66	ICS2	
GOUT	24		65	ICS1	
VSSG	25		64	ICS0	
Vddb	26		63	IBREAK	
BOUT	27		62	CLK	
VSSB	28		61	TRST	
VIN0	29		60	VDDI	
VIN1	30		59	X1	
VDDIS	31		58	VSS	
VSSS	32		57	X0	
VDDI	33		56	VDDE	
AVCC	34		55	P32	
AVRH	35		54	P31	
AVSS/AVRL	36		53	P30	
PC0/AN0	37		52	P27	
PC1/AN1	38		51	P26	
PC2/AN2	39		50	P25	
PC3/AN3	40		49	P24	
PC4/AN4	41		48	P23	
PC5/AN5	42		47	P22	
PC6/AN6	43		46	P21/ANG	
PC7/AN7	44		45	P20/ANG	

(FPT-176P-M07)

MB91319 Series

■ PIN DESCRIPTION

Pin No.	Pin Name	Circuit type	Function
1	HSYNC1	G	Vertical synchronous input 1
2	HSYNC2	G	Vertical synchronous input 2
3	HSYNC3	G	Vertical synchronous input 3
4	VDDE	—	I/O power supply
5	VSS	—	Ground
6	VGS1/VCI1	—	Guard band ground
7	CPO1	K	Charge pump output
8	VSSP1	—	Dot clock PLL ground
9	VDDP1	—	Dot clock PLL power supply
10	VGS2/VCI2	—	Guard band ground
11	CPO2	K	Charge pump output
12	VSSP2	—	Dot clock PLL ground
13	VDDP2	—	Dot clock PLL power supply
14	VGS3/VCI3	—	Guard band ground
15	CPO3	K	Charge pump output
16	VSSP3	—	Dot clock PLL ground
17	VDDP3	—	Dot clock PLL power supply
18	VDDR	—	D/A power supply for R
19	VRef (1.1 V)	K	Power supply reference input
20	VR0 (2.7 k Ω)	K	Resistor connection pin
21	ROUT	K	R output (analog)
22	VSSR	—	D/A ground for R
23	VDDG	—	D/A power supply for G
24	GOUT	K	G output (analog)
25	VSSG	—	D/A ground for G
26	Vddb	—	D/A power supply for B
27	BOUT	K	B output (analog)
28	VSSB	—	D/A ground for B
29	VIN0	K	Data slicer input 0
30	VIN1	K	Data slicer input 1
31	VDDIS	—	Data slicer power supply
32	VSSS	—	Data slicer ground
33	VDDI	—	Internal logic power supply
34	AVCC	—	A/D power supply
35	AVRH	—	A/D reference power supply

(Continued)

Pin No.	Pin Name	Circuit type	Function
36	AVSS/AVRL	—	A/D ground
37	PC0	E	General-purpose port
	AN0		Analog input
38	PC1	E	General-purpose port
	AN1		Analog input
40	PC3	E	General-purpose port
	AN3		Analog input
41	PC4	E	General-purpose port
	AN4		Analog input
42	PC5	E	General-purpose port
	AN5		Analog input
43	PC6	E	General-purpose port
	AN6		Analog input
44	PC7	E	General-purpose port
	AN7		Analog input
45	P20	E	General-purpose port
	AN8		Analog input
46	P21	E	General-purpose port
	AN9		Analog input
47	P22	C	General-purpose port
48	P23	C	General-purpose port
49	P24	C	General-purpose port
50	P25	C	General-purpose port
51	P26	C	General-purpose port
52	P27	C	General-purpose port
53	P30	C	General-purpose port
54	P31	C	General-purpose port
55	P32	C	General-purpose port
56	VDDE	—	3.3 V power supply
57	X0	A	10 MHz oscillation pin
58	VSS	—	Ground
59	X1	A	10 MHz oscillation pin
60	VDDI	—	Internal logic power supply
61	$\overline{\text{TRST}}$	B	DSU tool reset (In MB91F318A, this pin is the open pin so do not connect with other pins.)

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MB91319 Series

Pin No.	Pin Name	Circuit type	Function
62	ICLK	M	DSU clock (In MB91F318A, this pin is the open pin so do not connect with other pins.)
63	IBREAK	L	DSU break (In MB91F318A, this pin is the open pin so do not connect with other pins.)
64	ICS0	O	DSU status (In MB91F318A, this pin is the open pin so do not connect with other pins.)
65	ICS1	O	DSU status (In MB91F318A, this pin is the open pin so do not connect with other pins.)
66	ICS2	O	DSU status (In MB91F318A, this pin is the open pin so do not connect with other pins.)
67	ICD0	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
68	ICD1	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
69	ICD2	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
70	ICD3	P	DSU data (In MB91F318A, this pin is the open pin so do not connect with other pins.)
71	MD0	F	Mode pin
72	MD1	F	Mode pin
73	MD2	F	Mode pin
74	MD3	L	Mode pin
75	INIT	B	Initial (reset) pin
76	P80	J	General-purpose port
	SCL0		I ² C clock pin
77	P81	J	General-purpose port
	SDA0		I ² C data pin
78	P82	J	General-purpose port
	SCL1		I ² C clock pin
79	P83	J	General-purpose port
	SDA1		I ² C data pin
80	P84	C	General-purpose port
	SI0		UART0 serial input
81	P85	C	General-purpose port
	SO0		UART0 serial output
82	P86	C	General-purpose port
	SCK0		UART0 clock input/output

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Pin No.	Pin Name	Circuit type	Function
83	P87	C	General-purpose port
	SI1		UART1 serial input
84	P90	C	General-purpose port
	SO1		UART1 serial output
85	P91	C	General-purpose port
	SCK1		UART1 clock input/output
86	P92	C	General-purpose port
	RIN		PWC input
87	P93	C	General-purpose port
	TMI0		Multi-functional timer 0 input
88	P94	C	General-purpose port
	TMI1		Multi-functional timer 1 input
89	P95	C	General-purpose port
	TMI2		Multi-functional timer 2 input
90	P96	C	General-purpose port
	TMI3		Multi-functional timer 3 input
91	P97	O	General-purpose port
	INT0		External interrupt input 0
92	VDDE	—	3.3 V power supply
93	X0A	A	32 kHz oscillation pin
94	VSS	—	Ground
95	X1A	A	32 kHz oscillation pin
96	VDDI	—	Internal logic power supply
97	PA0	O	General-purpose port
	INT1		External interrupt input 1
98	PA1	O	General-purpose port
	INT2		External interrupt input 2
99	PA2	O	General-purpose port
	INT3		External interrupt input 3
100	$\overline{\text{NMI}}$	B	$\overline{\text{NMI}}$ input
101	P33	C	General-purpose port
	TRG0		PPG0 trigger input
102	P34	C	General-purpose port
	TRG1		PPG1 trigger input

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Pin No.	Pin Name	Circuit type	Function
103	P35	C	General-purpose port
	TRG2		PPG2 trigger input
104	P36	C	General-purpose port
	TRG3		PPG3 trigger input
105	P37	N	General-purpose port
	SCL2		I ² C clock pin
106	P40	N	General-purpose port
	SDA2		I ² C data pin
107	P41	N	General-purpose port
	SCL3		I ² C clock pin
108	P42	N	General-purpose port
	SCL4		I ² C clock pin
109	P43	N	General-purpose port
	SDA3		I ² C data pin
110	P44	N	General-purpose port
	SDA4		I ² C data pin
111	P45	C	General-purpose port
	SI2		UART2 serial input
112	P46	C	General-purpose port
	SO2		UART2 serial output
113	P47	C	General-purpose port
	SCK2		UART2 clock output
114	P50	C	General-purpose port
	SI3		UART3 serial input
115	P51	C	General-purpose port
	SO3		UART3 serial output
116	P52	C	General-purpose port
	SCK3		UART3 clock output
117	P53	C	General-purpose port
118	P54	C	General-purpose port
119	P55	C	General-purpose port
120	P56	C	General-purpose port
121	P57	C	General-purpose port
122	VDDI	—	Internal logic power supply
123	VSS	—	Ground

(Continued)

Pin No.	Pin Name	Circuit type	Function
124	VDDE	—	3.3 V power supply
125	P70	C	General-purpose port
126	P71	C	General-purpose port
127	P72	C	General-purpose port
128	P73	C	General-purpose port
129	P74	C	General-purpose port
130	P00	C	General-purpose port
	SI4		UART4 serial input
	TIN0		Reload timer 0 trigger input
131	P01	C	General-purpose port
	SO4		UART4 serial output
	TIN1		Reload timer 1 trigger input
132	P02	C	General-purpose port
	SCK4		UART4 clock input
	TIN2		Reload timer 2 trigger input
133	P03	C	General-purpose port
	TO0		Reload timer 0 output
134	P04	C	General-purpose port
	TO1		Reload timer 1 output
135	P05	C	General-purpose port
	TO2		Reload timer 2 output
136	P06	C	General-purpose port
	TMO0		Multi-functional timer 0 output
137	P07	C	General-purpose port
	TMO1		Multi-functional timer 1 output
138	P10	C	General-purpose port
	TMO2		Multi-functional timer 2 output
139	P11	C	General-purpose port
	TMO3		Multi-functional timer 3 output
140	P12	C	General-purpose port
	PPG0		PPG0 output
141	P13	C	General-purpose port
	PPG1		PPG1 output
142	P14	C	General-purpose port
	PPG2		PPG2 output

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MB91319 Series

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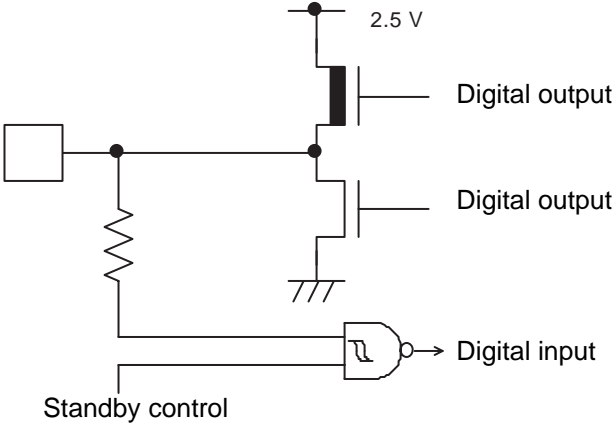
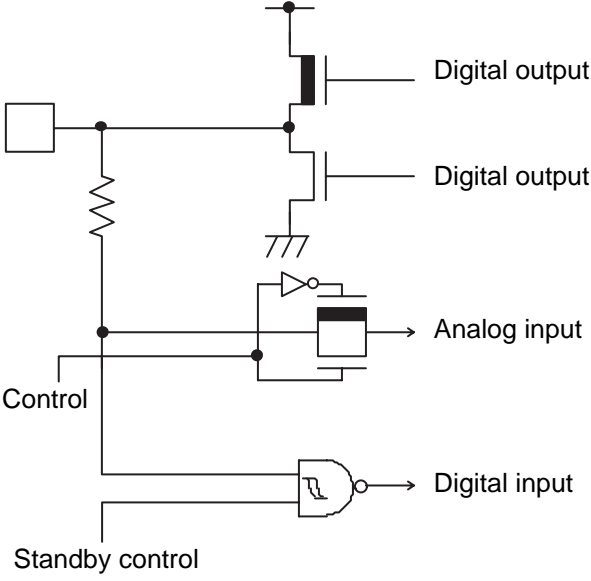
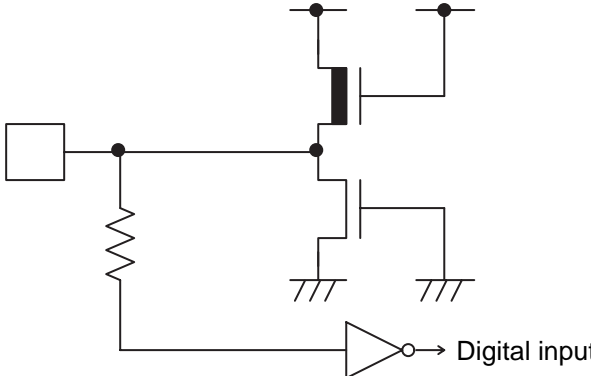
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143	P15	C	General-purpose port
	PPG3		PPG3 output
144	P16	C	General-purpose port
	ATRG		A/D conversion trigger input
145	P17	C	General-purpose port
146	PB0	C	General-purpose port
147	PB1	C	General-purpose port
148	PB2	I	General-purpose port
149	PB3	C	General-purpose port
150	PB4	C	General-purpose port
151	PB5	C	General-purpose port
152	PB6	H	General-purpose port
153	PB7	C	General-purpose port
154	VDDI	—	Internal power supply
155	X1B	A	48 MHz oscillation pin
156	VSS	—	Ground
157	X0B	A	48 MHz oscillation pin
158	VDDE	—	3.3 V power supply
159	UDM	USB	USB function
160	UDP		USB function
161	B0	D	RGB digital output
162	B1	D	RGB digital output
163	B2	D	RGB digital output
164	G0	D	RGB digital output
165	G1	D	RGB digital output
166	G2	D	RGB digital output
167	R0	D	RGB digital output
168	R1	D	RGB digital output
169	R2	D	RGB digital output
170	VDDI	—	Internal logic power supply
171	VOB2	D	Translucent color period output
172	VOB1	D	OSD display period output
173	FH	D	Horizontal synchronous output
174	DCKO	D	Dot clock output
175	DCKI	G	Dot clock input
176	VSYNC	G	Vertical synchronous output

■ I/O CIRCUIT TYPE

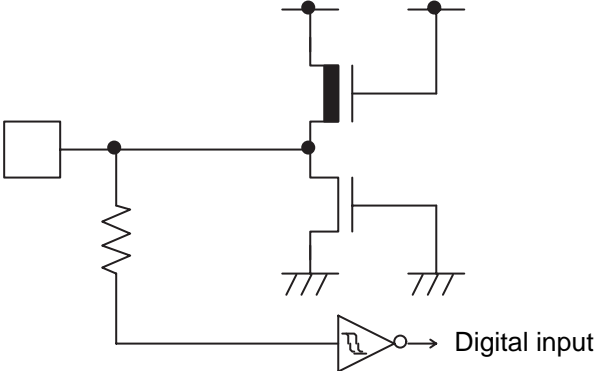
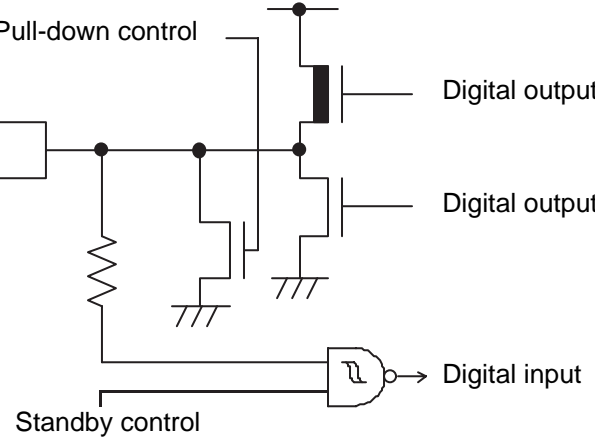
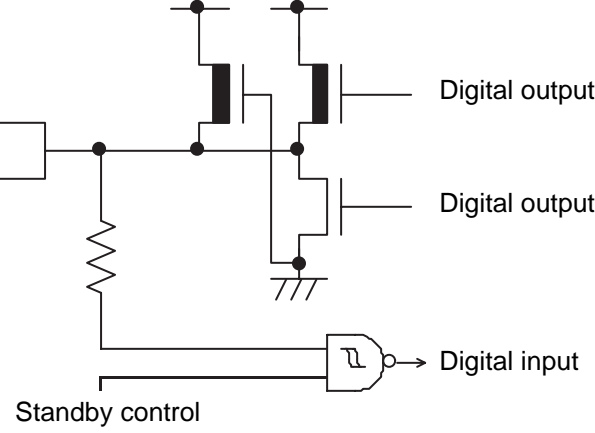
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A	<p style="text-align: center;">Standby control</p>	<p>Oscillation circuit</p>
B	<p style="text-align: right;">Digital input</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input • With pull-up resistor
C	<p style="text-align: right;">Digital output</p> <p style="text-align: right;">Digital output</p> <p style="text-align: right;">Digital input</p> <p style="text-align: center;">Standby control</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control

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MB91319 Series

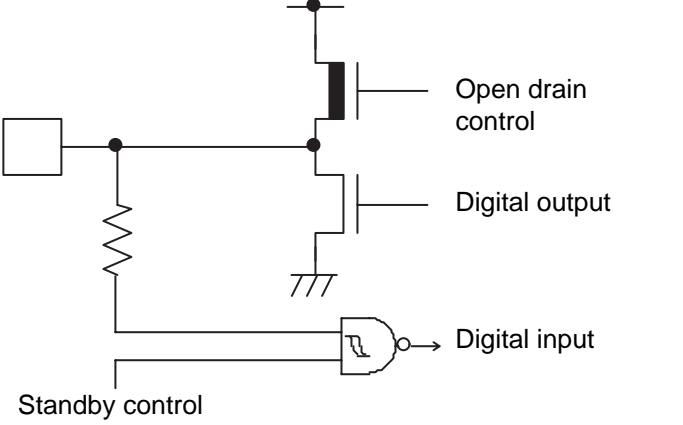
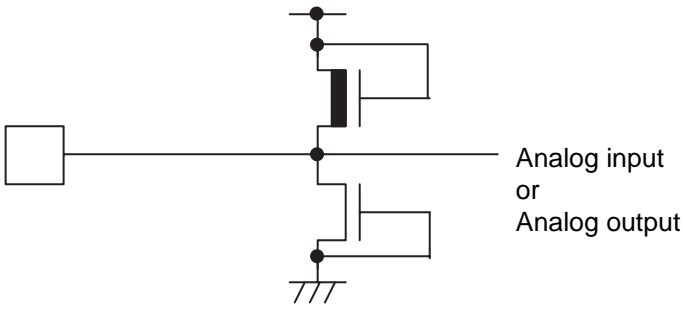
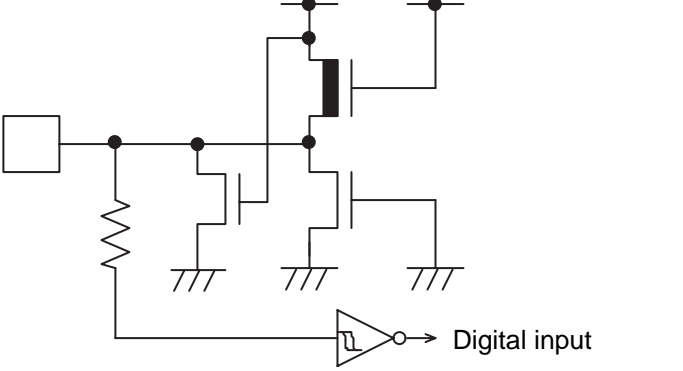
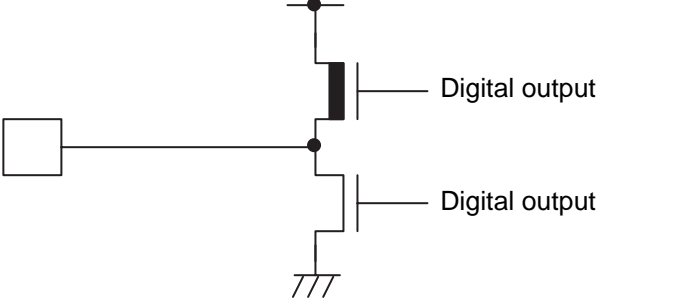
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D		<ul style="list-style-type: none"> • 2.5 V CMOS level output • CMOS level hysteresis input • With standby control
E		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control • With analog input switch
F		<ul style="list-style-type: none"> • CMOS level input • Without standby control

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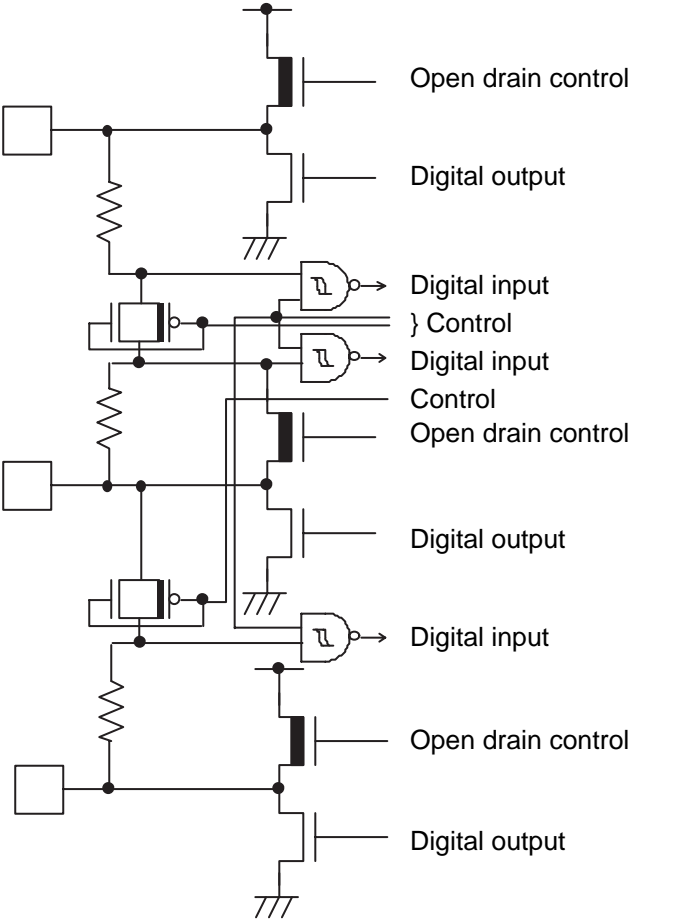
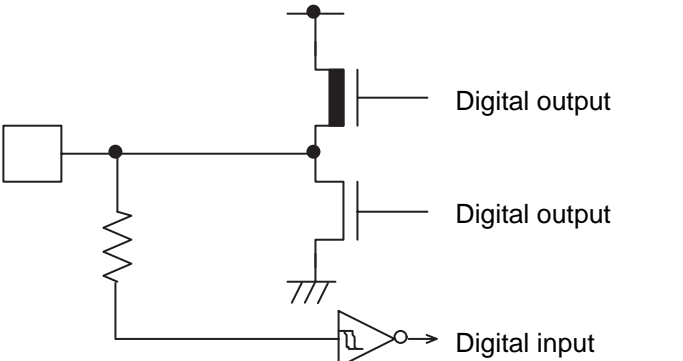
Type	Circuit type	Remarks
G		<ul style="list-style-type: none"> • CMOS level hysteresis input • Without standby control
H		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control • With pull-down resistor
I		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control • With pull-up resistor

(Continued)

MB91319 Series

Type	Circuit type	Remarks
J	 <p>Open drain control</p> <p>Digital output</p> <p>Digital input</p> <p>Standby control</p>	<ul style="list-style-type: none"> • Open drain output • CMOS level hysteresis input • With standby control
K	 <p>Analog input or Analog output</p>	Analog pin
L	 <p>Digital input</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input • With pull-down resistor
M	 <p>Digital output</p> <p>Digital output</p>	CMOS level output

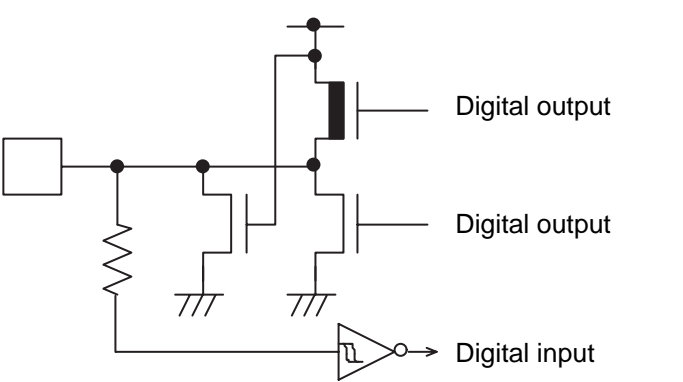
(Continued)

Type	Circuit type	Remarks
N	 <p>Open drain control</p> <p>Digital output</p> <p>Digital input</p> <p>} Control</p> <p>Digital input</p> <p>Control</p> <p>Open drain control</p> <p>Digital output</p> <p>Digital input</p> <p>Open drain control</p> <p>Digital output</p>	<ul style="list-style-type: none"> • 3 ports for I²C • CMOS level hysteresis input • CMOS level output • With stop control
O	 <p>Digital output</p> <p>Digital output</p> <p>Digital input</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • Without standby control

(Continued)

MB91319 Series

(Continued)

Type	Circuit type	Remarks
P		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • Without standby control • With pull-down resistor

■ HANDLING DEVICES

- Preventing Latchup

Latch-up may occur in a CMOS IC if a voltage greater than V_{CC} or less than V_{SS} is applied to an input or output pin or if an above-rating voltage is applied between V_{CC} and V_{SS} pins. A latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the maximum rating.

- Treatment of Unused Input Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

- Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins near this device.

- Crystal Oscillator Circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout.

- Mode Pins (MD0 to MD3)

These pins should be connected directly to V_{CC} or V_{SS} . To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

- Tool Reset Pins ($\overline{\text{TRST}}$)

When not using the tool, be sure to input the same signal as $\overline{\text{INIT}}$ to these pins. Apply the same treatment to mass-produced products as well.

- Operation at Power-on

Be sure to execute setting initialized reset (INIT) with $\overline{\text{INIT}}$ pin immediately after start-up.

Immediately after the power supply is turned on, hold the Low level input to the $\overline{\text{INIT}}$ pin for the settling time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit. (For INIT via the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value.)

- Oscillation Input at Power On

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

MB91319 Series

- Notes on Power-ON/Shut-down

Do not apply V_{DDE} (external) alone continuously (for over an indication of one minute) with V_{DDI} (internal) disconnected not to cause a reliability problem with LSI.

When V_{DDE} (external) returns from the OFF state to the ON state, the circuit may fail to hold its internal state, for example, due to power supply noise.

Turn ON/OFF the power supply in the following order:

- At power-on V_{DDI} (internal) → Analog → V_{DDE} (external) → Signal
- Turn off Signal → V_{DDE} (external) → Analog → V_{DDI} (internal)

- Undefined Output on Power-ON

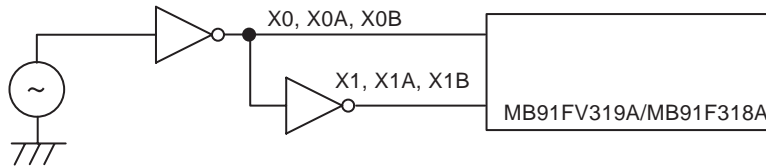
When the power is turned on, the output pin may remain unstable until the internal power supply becomes stable.

- Clock

About the attention when the external clock is used

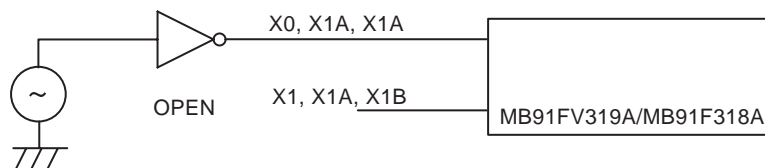
When the external clock is used, in principle, supply a clock signal to the X0 (X0A, X0B) pin and an opposite-phase clock signal to the X1 (X1A, X1B) pin at the same time. However, in this case the stop mode (oscillator stop mode) must not be used (This is because, in STOP mode, the X1 (X1A, X1B) pin stops at "H" output) . At 12.5 MHz or less, the device can be used with the clock signal supplied only to the X0 (X0A, X0B) pin.

- Using an External Clock (normal)



Note: The STOP mode (oscillation stop mode) cannot be used.

- Using an External Clock (available at 12.5 MHz or less)



Note : The X1 (X1A, X1B) pin must be designed to have a delay within 15 ns, at 10 MHz, from the signal to the X0 (X0A, X0B) pin.

- Restrictions

Common in MB91319 series

- (1) Clock control block

Take the oscillation stabilization wait time during Low level input to the $\overline{\text{INIT}}$ pin.

- (2) Bit Search Module

The 0-detection data register (BSD0) , 1-detection data register (BSD1) , and transition-detection data register (BDSC) are only word-accessible.

- (3) I/O port

Ports are accessed only in bytes.

- (4) Low-power Consumption Mode

- To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR : timebase counter control register) and be sure to use the following sequence:

(LD1 #value_of_stanby, R0)

(LD1 #_STCR, R12)

STB R0, @R12 ; Write to standby control register (STCR)

LDUB @R12, R0 ; STCR read for synchronous standby

LDUB @R12, R0 ; Dummy re-read of STCR

NOP ; NOP × 5 for adjusted timing

NOP

NOP

NOP

NOP

In addition, set the I-flag and the ILM and ICR registers to branch to an interrupt handler when the interrupt handler triggers the microcontroller to return from the standby mode.

- (5) Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

- The following operations are performed when the instruction followed by a data event, when breaks when single-stepped, or when a DIVOU/DIVOS emulator menu instruction receives a user interrupt or NMI.
 - (1)The D0 and D1 flags are updated in advance.
 - (2)An EIT handling routine (user interrupt, NMI, or emulator) is executed.
 - (3)Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1) .
- The following operations are performed when the ORCCR, STILM, MOV Ri, and PS instructions are executed to allow the interrupt at the state which a user interrupt/NMI cause occurs.
 - (1)The PS register is updated in advance.
 - (2)An EIT handling routine (user interrupt and NMI) is executed.
 - (3)Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1) .

MB91319 Series

(6) Watchdog timer

The watchdog timer built in this model monitors a program that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on operating programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.

For those conditions to which this exception applies, see the function description of watchdog timer.

A watchdog reset may not be generated in the above situation caused by the system running out of control. In that case, please reset (INIT) by external $\overline{\text{INIT}}$ pin.

(7) Notes on using A/D

The MB91319 series contains an A/D converter. Supply power to the AVCC at 3.3 V.

Evaluation chip MB91FV319A specific

(8) Simultaneous generation of software break and user interrupt/NMI (only for MB91FV319A)

If a software break and a user interrupt/NMI occur simultaneously, the emulator debugger may cause the following symptoms.

- The debugger stops pointing to a location other than the programmed breakpoints.
- The halted program is not re-executed correctly.

If these phenomena occur, use a hardware break instead of the software break. If the monitor debugger has been used, avoid setting any break at the relevant location.

(9) Step execution of RETI instruction

In an environment where interrupts frequently occur during single-step execution, only the relevant interrupt processing routines are executed repeatedly during single-step execution of the RETI instruction. This will prevent the main routine and low-interrupt-level programs from being executed. To avoid it, do not single-step RETI instructions.

When the relevant interrupt routine no longer requires being debugged, disable the relevant interrupt and perform debugging.

(10) About an operand break

Do not apply a data event break to access to the area containing the address of a stack pointer.

(11) Example of batch file for configuration

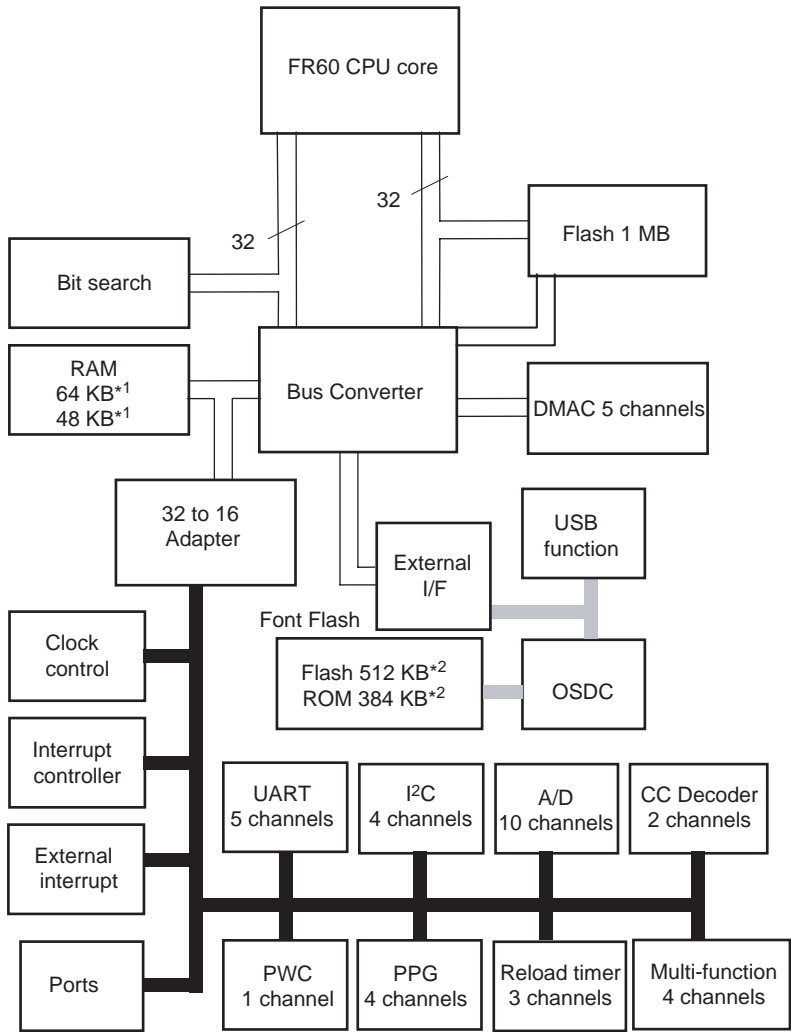
To debug a program downloaded to internal RAM, be sure to execute the following batch file after executing RESET.

```
#-----  
#Set MODR (0x7fd) = Enable In memory + 16-bit External Bus  
set mem/byte 0x7fd = 0x5  
#-----
```

(12) Address in the built-in FLASH/ROM area (1 MB product)

The address 0X0017FFF8 in the built-in FLASH/ROM area has been reserved. You must configure the FE.

■ BLOCK DIAGRAM



*1 : MB91FV319A contains the data RAM of 64KB, and MB91F318A contains that of 48KB.
 *2 : MB91FV319A contains the font ROM of 512KB flash memory, and MB91F318A contains that of 384KB mask ROM.

MB91319 Series

■ MEMORY SPACE

The FR family has 4 GB of logical address space (2^{32} addresses) available to the CPU by linear access.

● Direct Addressing Areas

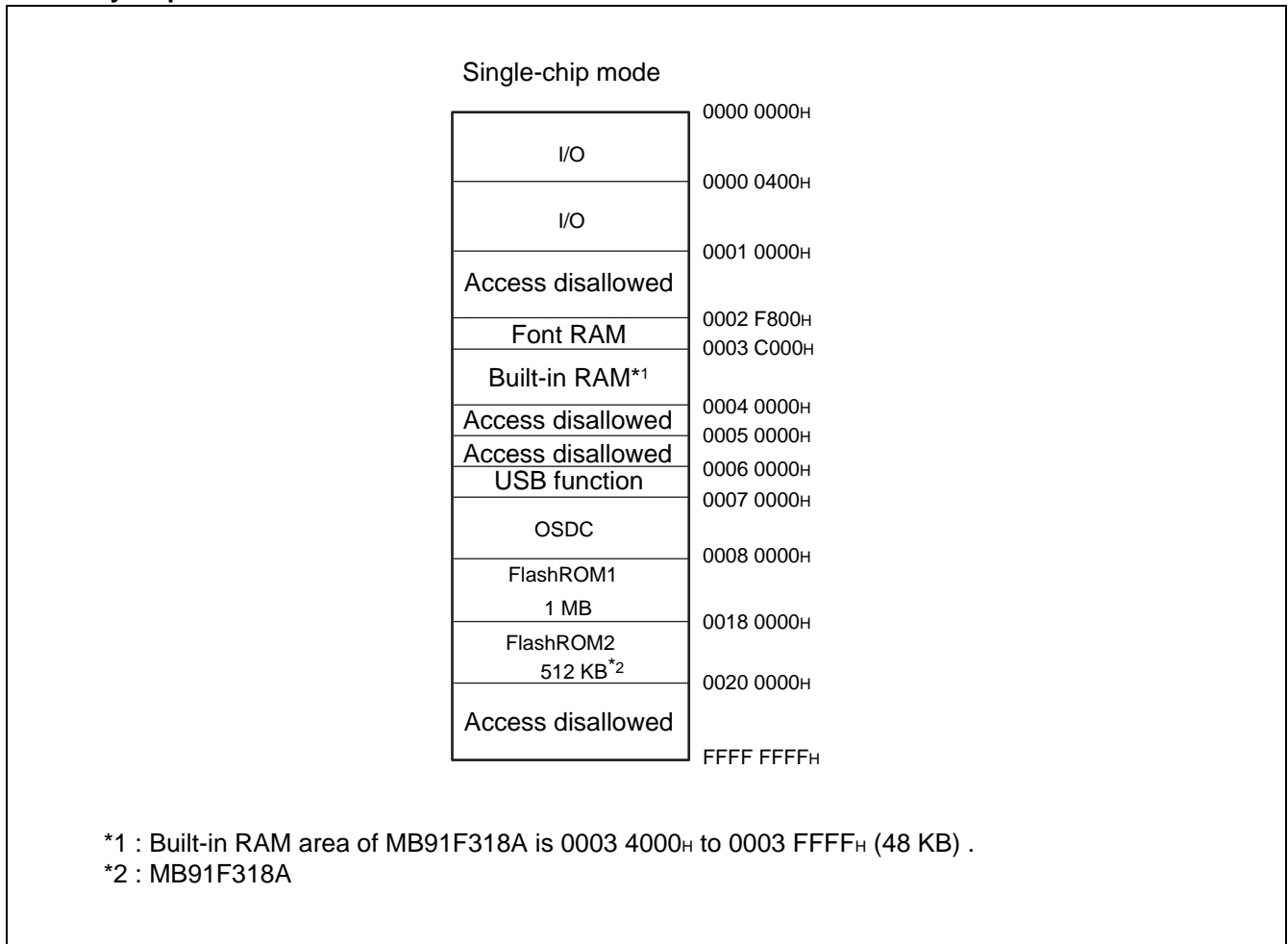
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The size of directly addressable areas depends on the length of the data being accessed as shown below.

- Byte data access : 000_H to 0FF_H
- Half word data access : 000_H to 1FF_H
- Word data access : 000_H to 3FF_H

● Memory Map



■ I/O MAP

This shows the correspondence between the memory space area and various peripheral resource registers.

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00000000H	PDR0 [R/W] XXXXXXXXX	PDR1 [R/W] XXXXXXXXX	PDR2 [R/W] XXXXXXXXX	PDR3 [R/W] XXXXXXXXX	T-unit Port Data Register

Read/Write attribute

Initial value of register after a reset

Register name (First-column register at address 4n; second-column register at address 4n + 2)

Leftmost register address (For word-length access, column 1 of the register becomes the MSB of the data.)

Note : Initial values of register bits are represented as follows :

“1” : Initial Value “1”

“0” : Initial Value “0”

“X” : Initial Value “X”

“ - ” : No physical register at this location

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H to 00000FH	—	—	—	—	Reserved
000010H	PDR0[R/W] XXXXXXXXX	PDR1[R/W] XXXXXXXXX	PDR2[R/W] XXXXXXXXX	PDR3[R/W] XXXXXXXXX	R-bus Port Data Register
000014H	PDR4[R/W] XXXXXXXXX	PDR5[R/W] XXXXXXXXX	—	PDR7[R/W] --XXXXXX	
000018H	PDR8[R/W] XXXXXXXXX	PDR9[R/W] XXXXXXXXX	PDRA[R/W] -----XXX	PDRB[R/W] XXXXXXXXX	
00001CH	PDRC[R/W] XXXXXXXXX	—	—	—	
000020H	ADCTH[R/W] XXXXXXXX00	ADCTL[R/W] 00000X00	ADCH[R/W] 00000000 00000000		10-bit A/D Converter
000024H	ADAT0[R] XXXXXXXX00 00000000		ADAT1[R] XXXXXXXX00 00000000		
000028H	ADAT2[R] XXXXXXXX00 00000000		ADAT3[R] XXXXXXXX00 00000000		
00002CH	ADAT4[R] XXXXXXXX00 00000000		ADAT5[R] XXXXXXXX00 00000000		
000030H	ADAT6[R] XXXXXXXX00 00000000		ADAT7[R] XXXXXXXX00 00000000		

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000034 _H	—	—	—	—	Reserved
000038 _H	—	—	—	—	
00003C _H	—	—	—	—	
000040 _H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000		Ext int
000044 _H	DICR [R/W] -----0	HRCL [R/W] 0--11111	—		DLYI/I-unit
000048 _H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004C _H	—		TMCSR0 [R/W] ---0000 00000000		
000050 _H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054 _H	—		TMCSR1 [R/W] ---0000 00000000		
000058 _H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005C _H	—		TMCSR2 [R/W] ---0000 00000000		
000060 _H	SSR0 [R/W] 00001-00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00--0-0-	UART0
000064 _H	UTIM0 [R] (UTIMR [W]) 00000000 00000000		DRCL0 [W] -----	UTIMC0 [R/W] 0--00001	U-TIMER 0
000068 _H	SSR1 [R/W] 00001-00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00--0-0-	UART1
00006C _H	UTIM1 [R] (UTIMR [W]) 00000000 00000000		DRCL1 [W] -----	UTIMC1 [R/W] 0--00001	U-TIMER 1
000070 _H	SSR2 [R/W] 00001-00	SIDR2 [R/W] XXXXXXXX	SCR2 [R/W] 00000100	SMR2 [R/W] 00--0-0-	UART2
000074 _H	UTIM2 [R] (UTIMR [W]) 00000000 00000000		DRCL2 [W] -----	UTIMC2 [R/W] 0--00001	U-TIMER 2
000078 _H	SSR3 [R/W] 00001-00	SIDR3 [R/W] XXXXXXXX	SCR3 [R/W] 00000100	SMR3 [R/W] 00--0-0-	UART3
00007C _H	UTIM3 [R] (UTIMR [W]) 00000000 00000000		DRCL3 [W] -----	UTIMC3 [R/W] 0--00001	U-TIMER 3
000080 _H	SSR4 [R/W] 00001-00	SIDR4 [R/W] XXXXXXXX	SCR4 [R/W] 00000100	SMR4 [R/W] 00--0-0-	UART4
000084 _H	UTIM4 [R] (UTIMR [W]) 00000000 00000000		DRCL4 [W] -----	UTIMC4 [R/W] 0--00001	U-TIMER 4

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000088 _H	—		—		Reserved
00008C _H	—		—		
000090 _H	PWCCL[R/W] 0000--00	PWCCH[R/W] 00-00000	—		PWC
000094 _H	PWCD[R] XXXXXXXX XXXXXXXX		—		
000098 _H	PWCC2[R/W] 000-----	Reserved	—		PWC
00009C _H	PWCUD[R] XXXXXXXX XXXXXXXX		—		
0000A0 _H	—		—		Reserved
0000A4 _H	—		—		
0000A8 _H	—		—		
0000AC _H	—		—		
0000B0 _H	IFN0 [R] 00000000	IFRN0 [R/W] 00000000	IFCR0 [R/W] 00-00000	IFDR0 [R/W] 00000000	I ² C Interface 0
0000B4 _H	IBCR0 [R/W] 00000000	IBSR0 [R/W] 00000000	ITBA0 [R/W] -----00 00000000		
0000B8 _H	ITMK0 [R/W] 00----11 11111111		ISMK0 [R/W] 01111111	ISBA0 [R/W] 00000000	
0000BC _H	—	IDAR0 [R/W] 00000000	ICCR0 [R/W] 0-011111	IDBL0 [R/W] -----0	
0000C0 _H	IFN1 [R] 00000000	IFRN1 [R/W] 00000000	IFCR1 [R/W] 00-00000	IFDR1 [R/W] 00000000	I ² C Interface 1
0000C4 _H	IBCR1 [R/W] 00000000	IBSR1 [R/W] 00000000	ITBA1 [R/W] -----00 00000000		
0000C8 _H	ITMK1 [R/W] 00----11 11111111		ISMK1 [R/W] 01111111	ISBA1 [R/W] 00000000	
0000CC _H	—	IDAR1 [R/W] 00000000	ICCR1 [R/W] 0-011111	IDBL1 [R/W] -----0	
0000D0 _H	IFN2 [R] 00000000	IFRN2 [R/W] 00000000	IFCR2 [R/W] 00-00000	IFDR2 [R/W] 00000000	I ² C Interface 2
0000D4 _H	IBCR2 [R/W] 00000000	IBSR2 [R/W] 00000000	ITBA2 [R/W] -----00 00000000		
0000D8 _H	ITMK2 [R/W] 00----11 11111111		ISMK2 [R/W] 01111111	ISBA2 [R/W] 00000000	
0000DC _H	—	IDAR2 [R/W] 00000000	ICCR2 [R/W] 0-011111	IDBL2 [R/W] -----0	

(Continued)

MB91319 Series

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
0000E0 _H	IFN3 [R] 00000000	IFRN3 [R/W] 00000000	IFCR3 [R/W] 00-00000	IFDR3 [R/W] 00000000	I ² C Interface 3	
0000E4 _H	IBCR3 [R/W] 00000000	IBSR3 [R/W] 00000000	ITBA3 [R/W] -----00 00000000			
0000E8 _H	ITMK3 [R/W] 00----11 11111111		ISMK3 [R/W] 01111111	ISBA3 [R/W] 00000000		
0000EC _H	—	IDAR3 [R/W] 00000000	ICCR3 [R/W] 0-011111	IDBL3 [R/W] -----0		
0000F0 _H	T0LPCR [R/W] -----000	T0CCR [R/W] 0-010000	T0TCR [R/W] 00000000	T0R [R/W] ---00000		
0000F4 _H	T0DDR [R/W] XXXXXXXX XXXXXXXX		T0CRR [R/W] XXXXXXXX XXXXXXXX		Multi-functional Timer	
0000F8 _H	T1LPCR [R/W] -----000	T1CCR [R/W] 0-000000	T1TCR [R/W] 00000000	T1R [R/W] ---00000		
0000FC _H	T1DDR [R/W] XXXXXXXX XXXXXXXX		T1CRR [R/W] XXXXXXXX XXXXXXXX			
000100 _H	T2LPCR [R/W] -----000	T2CCR [R/W] 0-000000	T2TCR [R/W] 00000000	T2R [R/W] ---00000		
000104 _H	T2DDR [R/W] XXXXXXXX XXXXXXXX		T2CRR [R/W] XXXXXXXX XXXXXXXX			
000108 _H	T3LPCR [R/W] -----000	T3CCR [R/W] 0-000000	T3TCR [R/W] 00000000	T3R [R/W] ---00000		
00010C _H	T3DDR [R/W] XXXXXXXX XXXXXXXX		T3CRR [R/W] XXXXXXXX XXXXXXXX			
000110 _H	TMODE [R/W] -----0--		—	—		
000114 _H to 00011F _H	—		—			Reserved
000120 _H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX			PPG0
000124 _H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 00000000	PCNL0 [R/W] 00000000		
000128 _H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PPG1	
00012C _H	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 00000000	PCNL1 [R/W] 00000000		
000130 _H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PPG2	
000134 _H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 00000000	PCNL2 [R/W] 00000000		

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000138 _H	PTMR3 [R] 11111111 11111111		PCSR3[W] XXXXXXXX XXXXXXXX		PPG3
00013C _H	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 00000000	PCNL3 [R/W] 00000000	
000140 _H to 00014C _H	—				Reserved
000150 _H to 00015C _H	—				Reserved
000160 _H	DSLCO0 0-----	DSLCO10 -011----	CCDC0 00-00011	VSEP0 00--0001	CCD Slicer 0 channel
000164 _H	CSYSEP0 -101-011	HMASK0 --100000	HCLR0 ---00110	FLD0 00100000	
000168 _H	HCNT0 00000000	C21H0 0-111111	CRIP0 11111111	CRIC0 000-0000	
00016C _H	CSTB0 11111111	CDTH0 11111111	CDAT00 00000000	CDAT10 00000000	
000170 _H	ID1C0 0-----00	ID20H0 0-111111	IDREF0 0-111111	IDTH0 11111111	
000174 _H	IDSTB0 11111111	IDDAT00 --000000	IDDAT10 00000000	IDDAT20 --000000	
000178 _H	DSAC10 ---000-0	DSAC20 10110011	DSAC30 00-00-00	—	
00017C _H	—	—	—	—	
000180 _H	DSLCO1 0-----	DSLCO11 -011----	CCDC1 00-00011	VSEP1 00--0001	CCD Slicer 1 channel
000184 _H	CSYTSEP1 -101-011	HMASK1 --100000	HCLR1 ---00110	FLD1 00100000	
000188 _H	HCNT1 00000000	C21H1 0-111111	CRIP1 11111111	CRIC1 000-0000	
00018C _H	CSTB1 11111111	CDTH1 11111111	CDAT01 00000000	CDAT1 00000000	
000190 _H	ID1C1 0-----00	ID20H1 0-111111	IDREF1 0-111111	IDTH1 11111111	
000194 _H	IDSTB1 11111111	IDDAT01 --000000	IDDAT11 00000000	IDDAT21 --000000	
000198 _H	DSAC11 ---000-0	DSAC21 10110011	DSAC31 00-00-00	—	
00019C _H	—	—	—	—	

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001A0 _H to 0001FC _H	—				Reserved
000200 _H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
000208 _H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
000210 _H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214 _H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
000218 _H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
000220 _H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
000228 _H	—				Reserved
00022C _H to 00023C _H	—				
000240 _H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
000244 _H to 0002FC _H	—				Reserved
000300 _H to 0003EC _H	—				
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000400 _H	DDR0 [R/W] 00000000	DDR1 [R/W] 00000000	DDR2 [R/W] 00000000	DDR3 [R/W] 00000000	R-bus Port Direction Register
000404 _H	DDR4 [R/W] 00000000	DDR5 [R/W] 00000000	—	DDR7 [R/W] --000000	
000408 _H	DDR8 [R/W] 00000000	DDR9 [R/W] 00000000	DDRA [R/W] ----000	DDRB [R/W] 00000000	
00040C _H	DDRC [R/W] 00000000	—	—	—	
000410 _H	PFR0 [R/W] 0--00000	PFR1 [R/W] 00000000	PFR2 [R/W] 00000000	PFR3 [R/W] 00000000	R-bus Port Function Register
000414 _H	PFR4 [R/W] 0000--00	PFR5 [R/W] 11111111	PFR6 [R/W] 11111111	PFR7 [R/W] 11111111	
000418 _H	PFR8 [R/W] 11111111	PFR9 [R/W] 11111111	PFRA [R/W] 11111111	PFRB [R/W] 11111111	
00041C _H	PFRC [R/W] 1111---1	PFRD [R/W] ---11111	—	—	
000420 _H to 00043C _H	—				Reserved
000440 _H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444 _H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448 _H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044C _H	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450 _H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454 _H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458 _H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045C _H	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460 _H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464 _H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468 _H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046C _H	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	

(Continued)

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000470H to 00047CH	—				Reserved
000480H	RSRR [R/W] 10000000*2	STCR [R/W] 00110011*2	TBCR [R/W] 00XXXX00*1	CTBR [W] XXXXXXXX	Clock Control Unit
000484H	CLKR [R/W] 00000000*1	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011*1	DIVR1[R/W] 00000000*1	
000488H	—	—	OSCCR [R/W] XXXXXXXX0	—	Reserved
00048CH	WPCR [R/W] B 00---000	—	—	—	Watch Timer
000490H	OSCR [R/W] B 00---000	—	—	—	Main Oscillation Stabilization Wait Timer
000494H to 0005FC _H	—				Reserved
000600H to 0007FC _H	—				Reserved
000800H to 000AFC _H	—				Reserved
000B00H	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXXX	—	DSU
000B04H	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	
000B08H	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	
000B0CH	EWP1 [R] 00000000 00000000		—		
000B10H	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		
000B14H to 000B1C _H	—				
000B20H	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24H	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000B28 _H	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU	
000B2C _H	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B30 _H	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B34 _H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B38 _H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B3C _H	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B40 _H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B44 _H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B48 _H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B4C _H	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B50 _H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B54 _H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B58 _H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B5C _H	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B60 _H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B64 _H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B68 _H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B6C _H	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000B70 _H to 000FFC _H	—					Reserved

(Continued)

MB91319 Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 006FFCH	—				Reserved
007000H	FLCR [R/W] 0110X000		—		Program FLASH I/F
007004H	FLWC [R/W] 00010011		—		
007008H to 0070FFH	—				Reserved
007100H	FNCR [R/W] 0110X000		—		Font FLASH I/F
007104H	FNWT [R/W] 00010011		—		

*1 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset.

*2 : The initial value of the register varies with the reset level. The initial value shown is the one after an INIT level reset by the $\overline{\text{INIT}}$ pin.

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
050000 _H to 050024 _H	Reserved				Reserved
050028 _H to 05FFFF _H	Reserved				Reserved
060000 _H	FIFO0o [R] XXXXXXXX XXXXXXXX		FIFO0i [W] XXXXXXXX XXXXXXXX		USB Function
060004 _H	FIFO1 [R] XXXXXXXX XXXXXXXX		FIFO2 [W] XXXXXXXX XXXXXXXX		
060008 _H	FIFO3 [R] XXXXXXXX XXXXXXXX		—		
06000C _H to 06001F _H	Reserved				
060020 _H	Reserved		CONT1 [R/W] 000XX0XX XXX00000		
060024 _H	CONT2 [R/W] XXXXXXXX XXX00000		CONT3 [R/W] XXXXXXXX XXX00000		
060028 _H	CONT4 [R/W] XXXXXXXX XXX00000		CONT5 [R/W] XXXXXXXX XXXX00XX		
06002C _H	CONT6 [R/W] XXXXXXXX XXXX00XX		CONT7 [R/W] XXXXXXXX XXX00000		
060030 _H	CONT8 [R/W] XXXXXXXX XXX00000		CONT9 [R/W] 0XX0XXXX 0XXX0000		
060034 _H	CONT10 [R/W] 00000000 X00000XX		TTSIZE [R/W] 00010001 00010001		
060038 _H	TRSIZE [R/W] 00010001 00010001		Reserved		
06003C _H	Reserved				
060040 _H	RSIZE0 [R] XXXXXXXX XXXX0000		Reserved		
060044 _H	RSIZE1 [R] XXXXXXXX X0000000		Reserved		
060048 _H to 06005F _H	Reserved				
060060 _H	Reserved		ST1 [R/W] XXXXXX00 00000000		
060064 _H	Reserved				

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
060068 _H	ST2 [R] XXXXXXXX X0000000		ST3 [R/W] 00XXXXXXXX X0000000		USB Function
06006C _H	ST4 [R/W] XXXXX000 00000000		ST5 [R/W] 0XX00XXX XX000000		
060070 _H to 06007F _H	Reserved				
060080 _H to 06FFFF _H	Reserved				Reserved
078000 _H	OSD_VADR [W] XXXXXXXX XXXXXXXX		OSD_CD1 [W] XXXXXXXX XXXXXXXX		OSDC (MAIN)
078004 _H	OSD_CD2 [W] XXXXXXXX XXXXXXXX		OSD_RCD1 [W] XXXXXXXX XXXXXXXX		
078008 _H	OSD_RCD2 [W] XXXXXXXX XXXXXXXX		OSD_SOC1 [W] XXXXXXXX 0000XXXX		
07800C _H	OSD_SOC2 [W] XXXXXXXX XXXXXXXX		OSD_VDPC [W] XXXXXXXX XXXXXXXX		
078010 _H	OSD_HDPC [W] XXXXXXXX XXXXXXXX		OSD_CVSC [W] XXXXXXXX XXXXXXXX		
078014 _H	OSD_SBFCC [W] XXXXXXXX XXXXXXXX		OSD_THCC [W] XXXXXXXX XXXXXXXX		
078018 _H	OSD_GFCC [W] XXXXXXXX XXXXXXXX		OSD_SBCC1 [W] XXXXXXXX XXXXXXXX		
07801C _H	OSD_SBCC2 [W] XXXXXXXX XXXXXXXX		OSD_SPCC1 [W] XXXXXXXX XXXXXXXX		
078020 _H	OSD_SPCC2 [W] XXXXXXXX XXXXXXXX		OSD_SPCC3 [W] XXXXXXXX XXXXXXXX		
078024 _H	OSD_SPCC4 [W] XXXXXXXX XXXXXXXX		OSD_SYNC [W] XXXXXXXX XXXXXXXX		
078028 _H	—		—		
07802C _H	—		OSD_IOC1 [W] XXXXXXXX XXXXXX00		
078030 _H	OSD_IOC2 [W] XXXXXXXX XXXXXXXX		OSD_DPC1 [W] XXXXXXXX XXXXXXXX		
078034 _H	OSD_DPC2 [W] XXXXXXXX XXXXXXXX		OSD_DPC3 [W] XXXXXXXX XXXXXXXX		
078038 _H	OSD_DPC4 [W] XXXXXXXX XXXXXXXX		OSD_IRC [W] XXXXXXXX XXXXXXXX		
07803C _H	OSD_PLT0 [W] XXXXXXXX XXXXXXXX		OSD_PLT1 [W] XXXXXXXX XXXXXXXX		

(Continued)

MB91319 Series

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
078040 _H	OSD_PLT2 [W] XXXXXXXX XXXXXXXX		OSD_PLT3 [W] XXXXXXXX XXXXXXXX		OSDC (MAIN)
078044 _H	OSD_PLT4 [W] XXXXXXXX XXXXXXXX		OSD_PLT5 [W] XXXXXXXX XXXXXXXX		
078048 _H	OSD_PLT6 [W] XXXXXXXX XXXXXXXX		OSD_PLT7 [W] XXXXXXXX XXXXXXXX		
07804C _H	OSD_PLT8 [W] XXXXXXXX XXXXXXXX		OSD_PLT9 [W] XXXXXXXX XXXXXXXX		
078050 _H	OSD_PLT10 [W] XXXXXXXX XXXXXXXX		OSD_PLT11 [W] XXXXXXXX XXXXXXXX		
078054 _H	OSD_PLT12 [W] XXXXXXXX XXXXXXXX		OSD_PLT13 [W] XXXXXXXX XXXXXXXX		
078058 _H	OSD_PLT14 [W] XXXXXXXX XXXXXXXX		OSD_PLT15 [W] XXXXXXXX XXXXXXXX		
07805C _H	OSD_ACT1 [W] XXXXXXXX XXXXXXXX		OSD_ACT2 [W] XXXXXXXX XXXXXXXX		
078060 _H	OSD_PLACC11 [W] XXXXXXXX XXXXXXXX		OSD_PLACC12 [W] XXXXXXXX XXXXXXXX		
078064 _H	OSD_PLACC2 [W] XXXXXXXX XXXXXXXX		OSD_PLACC3 [W] XXXXXXXX XXXXXXXX		
078068 _H	OSD_PLBCC11 [W] XXXXXXXX XXXXXXXX		OSD_PLBCC12 [W] XXXXXXXX XXXXXXXX		
07806C _H	OSD_PLBCC2 [W] XXXXXXXX XXXXXXXX		OSD_PLBCC3 [W] XXXXXXXX XXXXXXXX		
078070 _H	OSD_PLCC11[W] XXXXXXXX XXXXXXXX		OSD_PLCC12[W] XXXXXXXX XXXXXXXX		
078074 _H	OSD_PLCC2[W] XXXXXXXX XXXXXXXX		OSD_PLCC3[W] XXXXXXXX XXXXXXXX		
078078 _H	OSD_CSC1 [W] XXXXXXXX XXXXXXXX		OSD_CSC2 [W] XXXXXXXX XXXXXXXX		
07807C _H to 0780FF _H	—		—		
078100 _H	CCOSD_VADR [W] XXXXXXXX XXXXXXXX		CCOSD_CD1 [W] XXXXXXXX XXXXXXXX		OSDC (CC)
078104 _H	CCOSD_CD2 [W] XXXXXXXX XXXXXXXX		CCOSD_RCD1 [W] XXXXXXXX XXXXXXXX		
078108 _H	CCOSD_RCD2 [W] XXXXXXXX XXXXXXXX		CCOSD_SOC1 [W] XXXXXXXX 0000XXXX		
07810C _H	CCOSD_SOC2 [W] XXXXXXXX XXXXXXXX		CCOSD_VDPC [W] XXXXXXXX XXXXXXXX		

(Continued)

MB91319 Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
078110 _H	CCOSD_HDPC [W] XXXXXXXX XXXXXXXX		CCOSD_CVSC [W] XXXXXXXX XXXXXXXX		OSDC (CC)
078114 _H	—		CCOSD_THCC [W] XXXXXXXX XXXXXXXX		
078118 _H	—		—		
07811C _H	—		—		
078120 _H	—		—		
078124 _H	—		—		
078128 _H	—		—		
07812C _H	—		—		
078130 _H	—		CCOSD_DPC1 [W] XXXXXXXX XXXXXXXX		
078134 _H	CCOSD_DPC2 [W] XXXXXXXX XXXXXXXX		CCOSD_DPC3 [W] XXXXXXXX XXXXXXXX		
078138 _H	CCOSD_DPC4 [W] XXXXXXXX XXXXXXXX		CCOSD_IRC [W] XXXXXXXX XXXXXXXX		
07813C _H	CCOSD_PLT0 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT1 [W] XXXXXXXX XXXXXXXX		
078140 _H	CCOSD_PLT2 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT3 [W] XXXXXXXX XXXXXXXX		
078144 _H	CCOSD_PLT4 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT5 [W] XXXXXXXX XXXXXXXX		
078148 _H	CCOSD_PLT6 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT7 [W] XXXXXXXX XXXXXXXX		
07814C _H	CCOSD_PLT8 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT9 [W] XXXXXXXX XXXXXXXX		
078150 _H	CCOSD_PLT10 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT11 [W] XXXXXXXX XXXXXXXX		
078154 _H	CCOSD_PLT12 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT13 [W] XXXXXXXX XXXXXXXX		
078158 _H	CCOSD_PLT14 [W] XXXXXXXX XXXXXXXX		CCOSD_PLT15 [W] XXXXXXXX XXXXXXXX		
07815C _H	—		—		
078160 _H to 07FFFF _H	Reserved				Reserved

■ INTERRUPT FACTORS, INTERRUPT VECTORS, AND INTERRUPT REGISTER

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
Reset	0	00	—	3FC _H	000FFFFC _H	—
Mode vector	1	01	—	3F8 _H	000FFF8 _H	—
System reserved	2	02	—	3F4 _H	000FFF4 _H	—
System reserved	3	03	—	3F0 _H	000FFF0 _H	—
System reserved	4	04	—	3EC _H	000FFFE _C	—
System reserved	5	05	—	3E8 _H	000FFFE8 _H	—
System reserved	6	06	—	3E4 _H	000FFFE4 _H	—
Coprocessor absent trap	7	07	—	3E0 _H	000FFFE0 _H	—
Coprocessor error trap	8	08	—	3DC _H	000FFFD _C	—
INTE instruction	9	09	—	3D8 _H	000FFFD8 _H	—
Instruction break exception	10	0A	—	3D4 _H	000FFFD4 _H	—
Operand break trap	11	0B	—	3D0 _H	000FFFD0 _H	—
Step trace trap	12	0C	—	3CC _H	000FFFC _C	—
NMI request (tool)	13	0D	—	3C8 _H	000FFFC8 _H	—
Undefined instruction exception	14	0E	—	3C4 _H	000FFFC4 _H	—
NMI request	15	0F	15 (F _H) fixed	3C0 _H	000FFFC0 _H	—
External interrupt 0	16	10	ICR00	3BC _H	000FFFB _C	—
External interrupt 1	17	11	ICR01	3B8 _H	000FFFB8 _H	—
External interrupt 2	18	12	ICR02	3B4 _H	000FFFB4 _H	—
External interrupt 3	19	13	ICR03	3B0 _H	000FFFB0 _H	—
External interrupt 4 (USB function)	20	14	ICR04	3AC _H	000FFFA _C	—
External interrupt 5 (OSDC-MAIN)	21	15	ICR05	3A8 _H	000FFFA8 _H	—
External interrupt 6 (OSDC-CC)	22	16	ICR06	3A4 _H	000FFFA4 _H	—
System reserved	23	17	ICR07	3A0 _H	000FFFA0 _H	—
Reload timer 0	24	18	ICR08	39C _H	000FFF9 _C	8
Reload timer 1	25	19	ICR09	398 _H	000FFF98 _H	9
Reload timer 2	26	1A	ICR10	394 _H	000FFF94 _H	10
UART0 (Reception completed)	27	1B	ICR11	390 _H	000FFF90 _H	0
UART1 (Reception completed)	28	1C	ICR12	38C _H	000FFF8 _C	1
UART2 (Reception completed)	29	1D	ICR13	388 _H	000FFF88 _H	2
UART0 (Transmission completed)	30	1E	ICR14	384 _H	000FFF84 _H	3
UART1 (Transmission completed)	31	1F	ICR15	380 _H	000FFF80 _H	4

(Continued)

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Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
UART2 (Transmission completed)	32	20	ICR16	37C _H	000FFF7C _H	5
DMAC0 (end, error)	33	21	ICR17	378 _H	000FFF78 _H	—
DMAC1 (end, error)	34	22	ICR18	374 _H	000FFF74 _H	—
DMAC2 (end, error)	35	23	ICR19	370 _H	000FFF70 _H	—
DMAC3 (end, error)	36	24	ICR20	36C _H	000FFF6C _H	—
DMAC4 (end, error)	37	25	ICR21	368 _H	000FFF68 _H	—
A/D	38	26	ICR22	364 _H	000FFF64 _H	—
PPG0	39	27	ICR23	360 _H	000FFF60 _H	—
PPG1	40	28	ICR24	35C _H	000FFF5C _H	—
PPG2	41	29	ICR25	358 _H	000FFF58 _H	—
PPG3	42	2A	ICR26	354 _H	000FFF54 _H	—
PWC	43	2B	ICR27	350 _H	000FFF50 _H	—
CCD0	44	2C	ICR28	34C _H	000FFF4C _H	—
CCD1	45	2D	ICR29	348 _H	000FFF48 _H	—
Main oscillation wait	46	2E	ICR30	344 _H	000FFF44 _H	—
Timebase timer overflow	47	2F	ICR31	340 _H	000FFF40 _H	—
System reserved	48	30	ICR32	33C _H	000FFF3C _H	—
Watch timer	49	31	ICR33	338 _H	000FFF38 _H	—
I ² C ch0	50	32	ICR34	334 _H	000FFF34 _H	—
I ² C ch1	51	33	ICR35	330 _H	000FFF30 _H	—
I ² C ch2	52	34	ICR36	32C _H	000FFF2C _H	—
I ² C ch3	53	35	ICR37	328 _H	000FFF28 _H	—
UART3 (Reception completed)	54	36	ICR38	324 _H	000FFF24 _H	—
UART4 (Reception completed)	55	37	ICR39	320 _H	000FFF20 _H	—
UART3 (Transmission completed)	56	38	ICR40	31C _H	000FFF1C _H	—
UART4 (Reception completed)	57	39	ICR41	318 _H	000FFF18 _H	—
Multi-functional timer 0	58	3A	ICR42	314 _H	000FFF14 _H	—
Multi-functional timer 1	59	3B	ICR43	310 _H	000FFF10 _H	—
Multi-functional timer 2	60	3C	ICR44	30C _H	000FFF0C _H	—
Multi-functional timer 3	61	3D	ICR45	308 _H	000FFF08 _H	—
System reserved	62	3E	ICR46	304 _H	000FFF04 _H	—
Delay interrupt factor bit	63	3F	ICR47	300 _H	000FFF00 _H	—
System reserved (Used by REALOS)	64	40	—	2FC _H	000FFEFC _H	—
System reserved (Used by REALOS)	65	41	—	2F8 _H	000FEF8 _H	—

(Continued)

(Continued)

Interrupt factor	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
System reserved	66	42	—	2F4 _H	000FFE _{F4H}	—
System reserved	67	43	—	2F0 _H	000FFE _{F0H}	—
System reserved	68	44	—	2E _C _H	000FFE _{EC} _H	—
System reserved	69	45	—	2E8 _H	000FFE _{E8} _H	—
System reserved	70	46	—	2E4 _H	000FFE _{E4} _H	—
System reserved	71	47	—	2E0 _H	000FFE _{E0} _H	—
System reserved	72	48	—	2D _C _H	000FFE _{DC} _H	—
System reserved	73	49	—	2D8 _H	000FFE _{D8} _H	—
System reserved	74	4A	—	2D4 _H	000FFE _{D4} _H	—
System reserved	75	4B	—	2D0 _H	000FFE _{D0} _H	—
System reserved	76	4C	—	2C _C _H	000FFE _{CC} _H	—
System reserved	77	4D	—	2C8 _H	000FFE _{C8} _H	—
System reserved	78	4E	—	2C4 _H	000FFE _{C4} _H	—
System reserved	79	4F	—	2C0 _H	000FFE _{C0} _H	—
Used by INT instruction	80 to 255	50 to FF	—	2B _C _H to 000 _H	000FFE _{BC} _H to 000FF _{C00} _H	—

MB91319 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *	V _{DDE} (3.3 V)	V _{SS} - 0.5	V _{SS} + 4.0	V	
	V _{DDI} (2.5 V)	V _{SS} - 0.5	V _{SS} + 3.0	V	
Analog power supply voltage *	AV _{CC}	V _{SS} - 0.5	V _{SS} + 4.0	V	
Input voltage *	V _I	V _{SS} - 0.5	V _{DDE} + 0.5	V	
Analog pin input voltage *	V _{IA}	V _{SS} - 0.5	AV _{CC} + 0.5	V	
Output voltage *	V _O	V _{SS} - 0.5	V _{DDE} + 0.5	V	
Storage temperature	T _{stg}	- 40	+ 125	°C	

* : The parameter is based on V_{SS} = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Operating temperature	T _a	- 40	+ 70	°C	
Power supply voltage	V _{DDE} (3.3 V)	3.00	3.6	V	
	V _{DDI} (2.5 V)	2.30	2.70		
Analog power supply voltage	AV _{CC}	3.00	V _{DDE}	V	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(1) CPU

(Ta = -10 °C to +70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I _{CC1}	Watch mode Ta = +25 °C, fclk = 32 kHz	—	800	1300	μA	Dot clock PLL stop USB clock stop
	I _{CC}	ROM product normal operation Ta = +25 °C, fcp = 40 MHz, fcpp = 20 MHz	—	240	280	mA	Font Mask ROM Dot clock at 90 MHz
	I _{CCS}	Main sleep mode Ta = +25 °C, fcp = 40 MHz, fcpp = 20 MHz	—	160	200	mA	Dot clock PLL stop
	I _{CC1}	Sub RUN mode Ta = +25 °C, fclk = 32 kHz	—	1000	1700	μA	Dot clock PLL stop USB clock stop
	I _{CC1}	Main stop mode Ta = +25 °C, fclk = 0 kHz	—	150	400	μA	Font Mask ROM
		Main stop mode Ta = +70 °C, fclk = 0 kHz	—	1200	4000	μA	Font Mask ROM
“H” level input voltage	V _{IH}	—	V _{CC} × 0.8	—	V _{CC}	V	
“L” level input voltage	V _{IL}	V _{CC} = 3.3 V	V _{SS}	—	V _{CC} × 0.2	V	P00 to P74, PA0 to PA2, PB0 to PB7, PC0 to PC7, DCKI, HSYNC1 to HSYNC3, VSYNC
		V _{CC} = 2.5 V			V _{CC} × 0.15	V	B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
“H” level output voltage	V _{OH}	V _{CC} = 3.3 V, I _{OH} = -4 mA	V _{CC} - 0.5	—	V _{CC}	V	P0 to PC
		V _{CC} = 2.5 V, I _{OH} = -4 mA				V	B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
“L” level output voltage	V _{OL}	V _{CC} = 3.3 V, I _{OL} = 4 mA	V _{SS}	—	0.4	V	P0 to PC
		V _{CC} = 2.5 V, I _{OL} = 4 mA				V	B0 to B2, G0 to G2, R0 to R2, VOB1, VOB2, DCKO, FH
Input leak current	I _{IL}	—	-5	—	5	μA	
I ² C bus switch connection resistance	R _{BS}	—	—	—	130	Ω	Between SCL2 and SCL3 Between SDA2 and SDA3 Between SCL3 and SCL4 Between SDA3 and SDA4

(Continued)

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(Continued)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Analog RGB reference voltage	V _{REF}	—	1.05	1.10	1.15	V	VREF
Analog RGB reference resistance	R _{REF}	—	2.4	2.7	—	kΩ	Between VR0 and GND
Analog RGB output impedance	R _L	—	—	150	160	Ω	ROUT, GOUT, BOUT

(2) USB

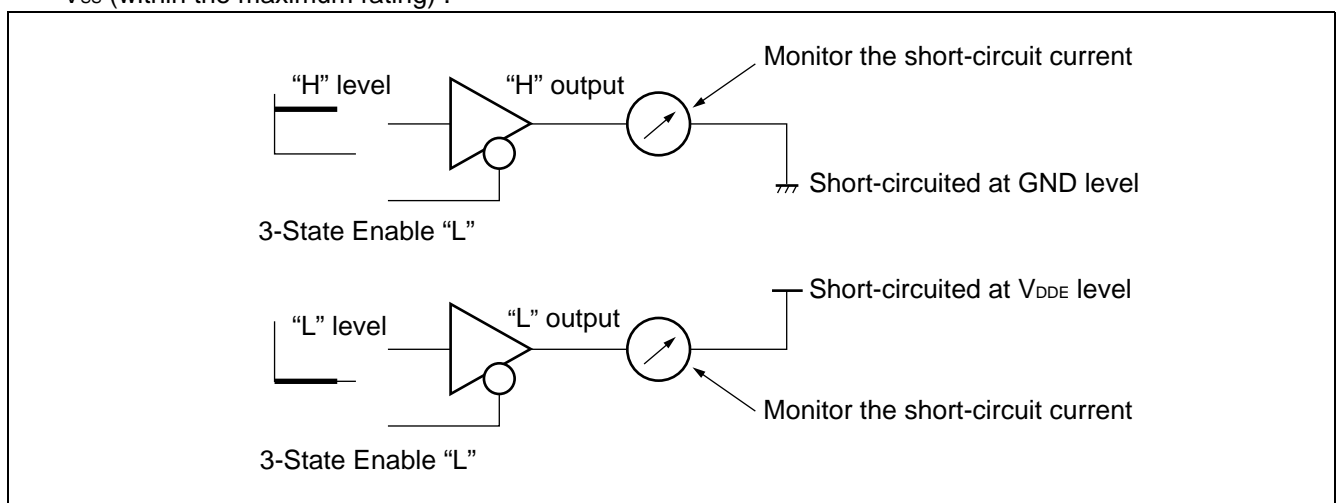
• DC Characteristics (1)

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	—	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{DDE} - 0.2$	—	V_{DDE}	V	
"L" level output voltage	V_{OL}	—	$I_{OL} = 100\text{ }\mu\text{A}$	0	—	0.2	V	
"H" level output current	I_{OH}	—	At Full Speed Mode $V_{OH} = V_{DDE} - 0.4\text{ V}$	-20	—	—	mA	
			At Low Speed Mode $V_{OH} = V_{DDE} - 0.4\text{ V}$	-6	—	—	mA	
"L" level output current	I_{OL}	—	At Full Speed Mode $V_{OL} = 0.4\text{ V}$	20	—	—	mA	
			At Low Speed Mode $V_{OL} = 0.4\text{ V}$	6	—	—	mA	
Output short-circuit current	I_{OS}	—	—	—	—	300	mA	*1
Input leak current	I_{LZ}	—	—	—	—	± 5	μA	*2

*1 : About the output short-circuit current I_{OS}

Output short-circuit current I_{OS} is the maximum current that flows when the output pin is connected to V_{DDE} or V_{SS} (within the maximum rating).

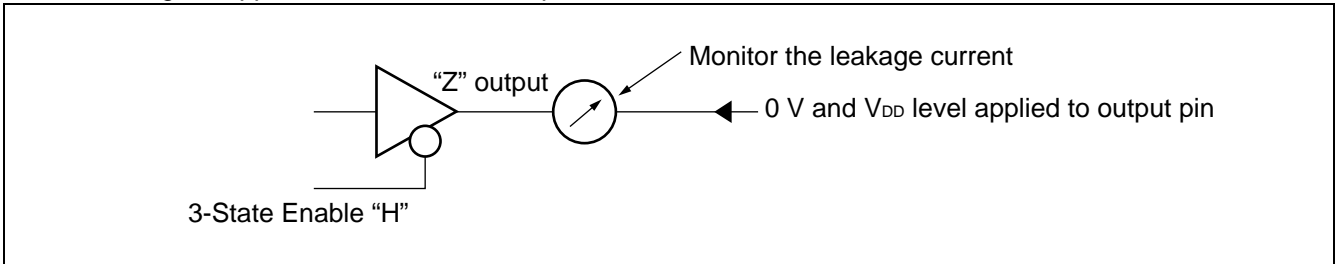


About the output short-circuit current : The current is "the short-circuit current per differential output pin". As the USB I/O buffer is a differential output, the short-circuit current should be considered for both of the output pins.

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*2 : About measurement of "Z" leakage current I_{LZ}

Input leakage current I_{LZ} is measured with the USB I/O buffer in the high-impedance state when the V_{DDE} or V_{SS} voltage is applied to the bidirectional pin.



- DC Characteristics (2)

Conform to the USB Specification Revision 1.1.

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Input Voltage :					
High (driven)	V_{IH}	2.0	—	V	*1
Low	V_{IL}	—	0.8	V	*1
Differential Input Sensitivity	V_{DI}	0.2	—	V	*2
Common Mode Input Voltage	V_{CM}	0.8	2.5	V	*2
Output Voltage :					
Low	V_{OL}	0.0	0.3	V	*3
High (driven)	V_{OH}	2.8	3.6	V	*3
Output Signal Crossover Voltage	V_{CRS}	1.3	2.0	V	*4
Terminations :					
Pull-Up Resistor on Upstream Port	R_{PU}	1.425	1.575	k Ω	1.5 k Ω \pm 5%
Pull-Down Resistor on Downstream Port	R_{PD}	1.425	1.575	k Ω	1.5 k Ω \pm 5%
Termination voltage for upstream port pull-up	V_{TERM}	3.0	3.6	V	*5

*1 : About input voltage V_{IH} , V_{IL}

The switching threshold voltage of the USB I/O buffer's single-end receiver is set within the range from $V_{IL}(\text{Max}) = 0.8\text{ V}$ to $V_{IH}(\text{Min}) = 2.0\text{ V}$ (TTL input standard) .

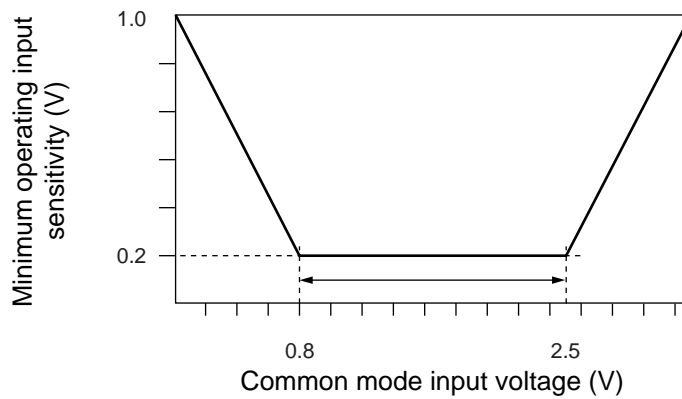
For V_{IH} and V_{IL} , the LSI has some hysteresis to reduce noise susceptibility.

*2 : About input voltage V_{DI} , V_{CM}

A differential receiver is used to receive USB differential data signals.

The differential receiver has a differential input sensitivity of 200 mV when the differential data input falls within the range from 0.8 V to 2.5 V with respect to the local ground reference level.

The above voltage range is referred to as common-mode input voltage range.



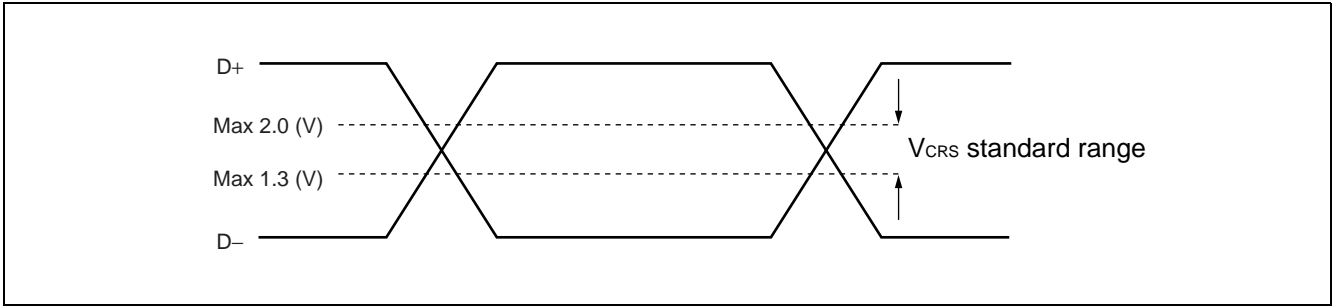
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*3 : About output voltage V_{OL} , V_{OH}

The output driving performance levels of the driver are 0.3 V or less (to 3.6 V, 1.5 k Ω load) in the low state (V_{OL}) and 2.8 V or more (to ground, 1.5 k Ω load) in the high state (V_{OH}) .

*4 : About output voltage V_{CRS}

The cross voltage of the external differential output signals (D+ and D-) for the USB I/O buffer falls within the range from 1.3 V to 2.0 V.



*5 : About terminations V_{TERM}

V_{TERM} indicates the pull-up voltage at the upstream port.

4. AC Characteristics

(1) Clock Timing

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Clock frequency	f_c	X0, X1	—	6.25	10	MHz	PLL system (operation at a maximum internal speed of 40 MHz by quadrupling a self-oscillation frequency of 10 MHz via PLL)
Internal operating clock frequency	f_{CP}	—	—	1.56*	40	MHz	CPU system ($t_{CP} = 1/f_{CP}$)
	f_{CPP}			1.56*	20	MHz	Peripheral system ($t_{CPP} = 1/f_{CPP}$)
	f_{CPT}			1.56*	20	MHz	External bus system ($t_{CPT} = 1/f_{CPT}$)

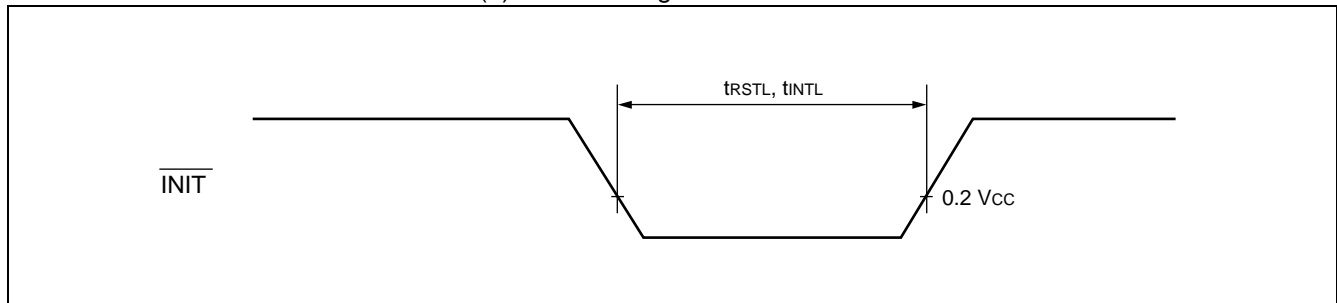
* : The numeric value when inputting the 6.25 MHz (the minimum clock frequency) to X0 and using the PLL system and the gear ratio 1/16 of the oscillator circuit.

(2) Reset Input

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
INIT input time (at power-on)	t_{INTL}	$\overline{\text{INIT}}$	—	Oscillation stabilization wait time of oscillator $+ t_{CP} \times 10$	—	μs	
INIT input time (other than at power-on)				$t_{CP} \times 10$	—	ns	
INIT input time (at recovering stop)				Oscillation stabilization wait time of oscillator $+ t_{CP} \times 10$	—	μs	

Note: t_{CP} is the internal clock time. See “(1) Clock Timing”.



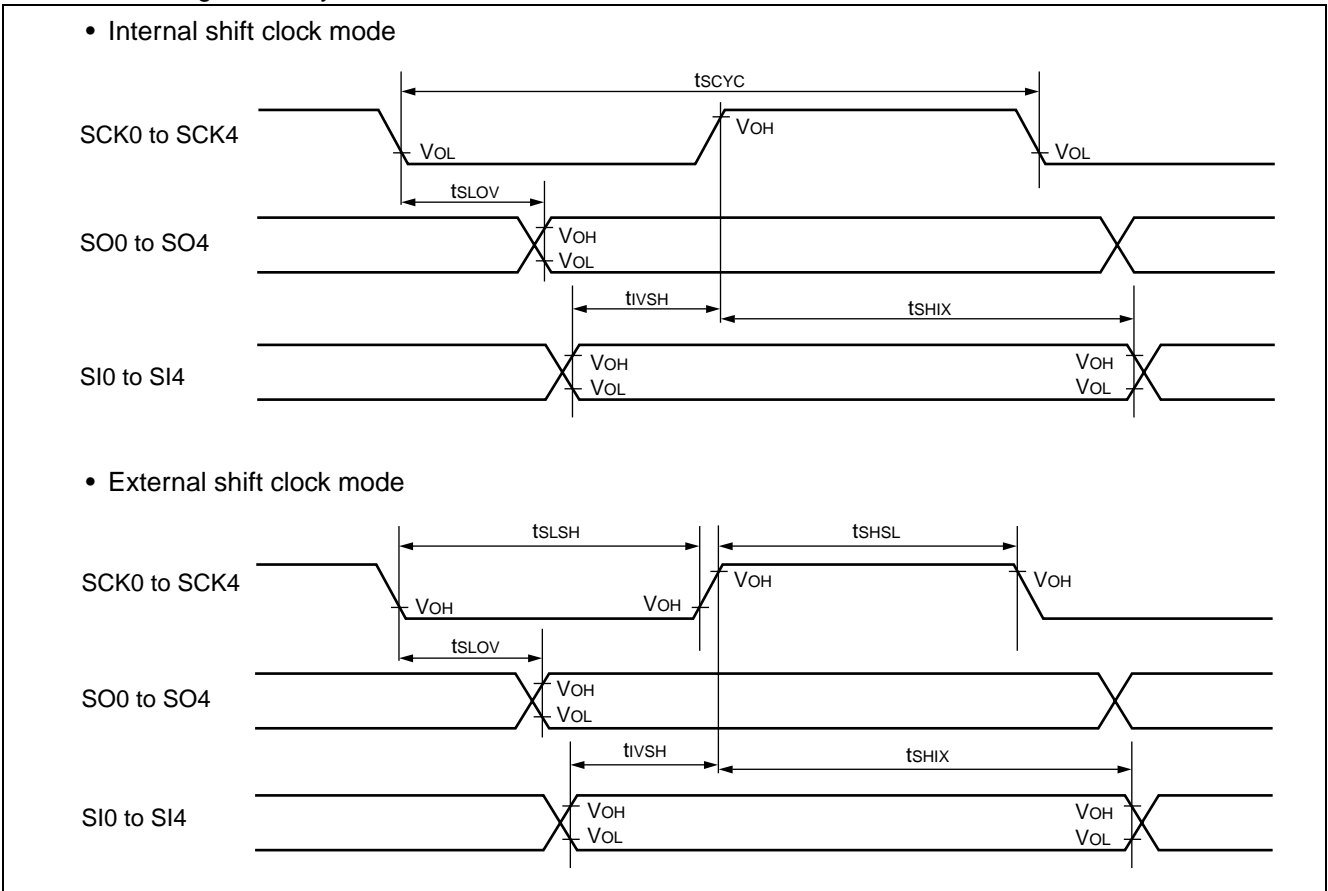
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(3) UART Timing

($T_a = -10\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Internal shift lock mode	$8 t_{CPP}$	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK4, SO0 to SO4		- 80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK4, SI0 to SI4		100	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK4, SI0 to SI4		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	External shift lock mode	$4 t_{CPP}$	—	ns	
Serial clock "L" pulse width	t_{LSLH}	SCK0 to SCK4		$4 t_{CPP}$	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK4, SO0 to SO4		—	150	ns	
Valid SI → SCK ↑	t_{IVSH}	SCK0 to SCK4, SI0 to SI4		60	—	ns	
Valid SCK ↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK4, SI0 to SI4		60	—	ns	

Note : • t_{CPP} indicates the peripheral clock cycle time. See "(1) Clock Timing".
 • AC rating in CLK synchronous mode.

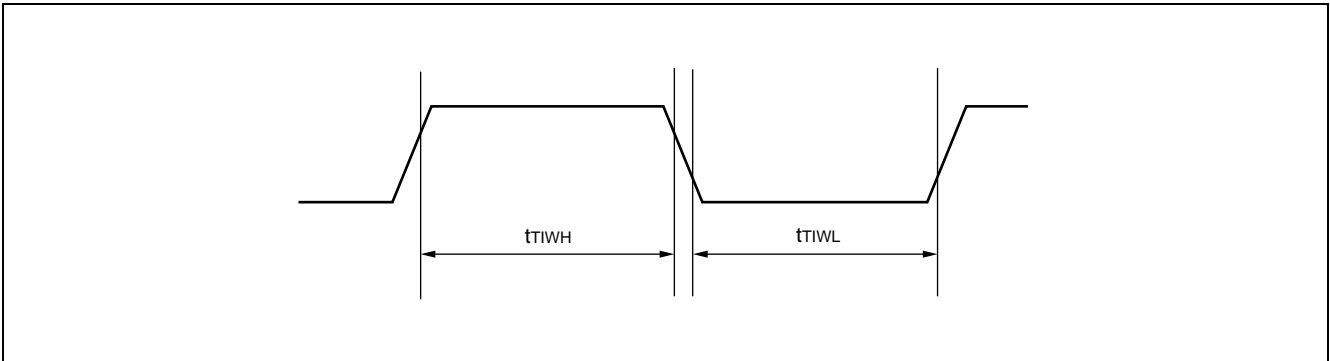


(4) Reload timer clock , PPG timer input, multi-functional timer input timing

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN2, PPG0 to PPG3, TRG0 to TRG3, TMI0 to TMI3	—	$2 t_{CPP}$	—	ns	

Note : t_{CPP} indicates the peripheral clock cycle time. See “(1) Clock Timing”.

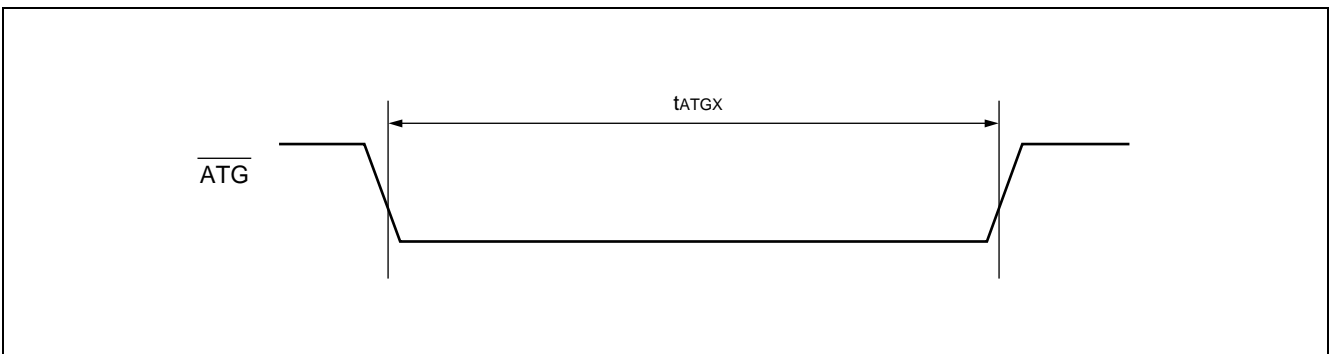


(5) Trigger Input Timing

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
A/D activation trigger input time	t_{ATGX}	\overline{ATG}	—	$5 t_{CPP}$	—	ns	

Note : t_{CPP} indicates the peripheral clock cycle time. See “(1) Clock Timing”.

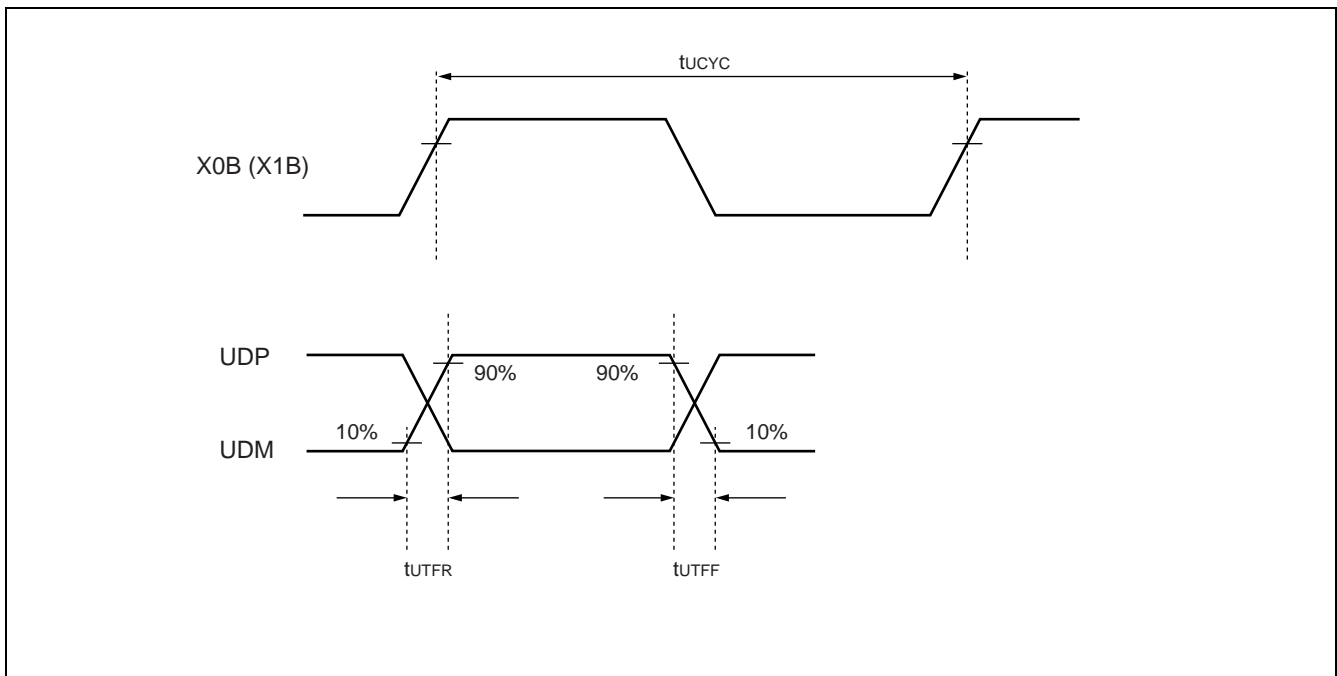


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(6) USB interface

($T_a = -10\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input clock	t_{UCYC}	X0B, X1B	—	—	48*1	—	MHz	Self-oscillation 500 ppm accuracy *1
		X0B	—	—	—	—		External input 500 ppm accuracy *1
Rise Time	t_{UTFR}	UDP/ UDM	At Full Speed Mode	4	—	20	ns	*2
Fall Time	t_{UTFF}	UDP/ UDM	At Full Speed Mode	4	—	20	ns	*2
Differential Rise and Fall Timing Matching	t_{UTFRFM}	UDP/ UDM	At Full Speed Mode	90	—	111.11	%	*2
Driver Output Resistance	t_{ZDRV}	UDP, UDM	—	28	—	44	Ω	*3



*1 : The AC characteristics of the USB interface conform to USB Specification Revision 1.1.

*2 : About driver characteristics t_{UTFR} , t_{UTFF} , t_{UTFRFM}

These items specify the differential data signal rise (Rise Time) and fall (Fall time) times.

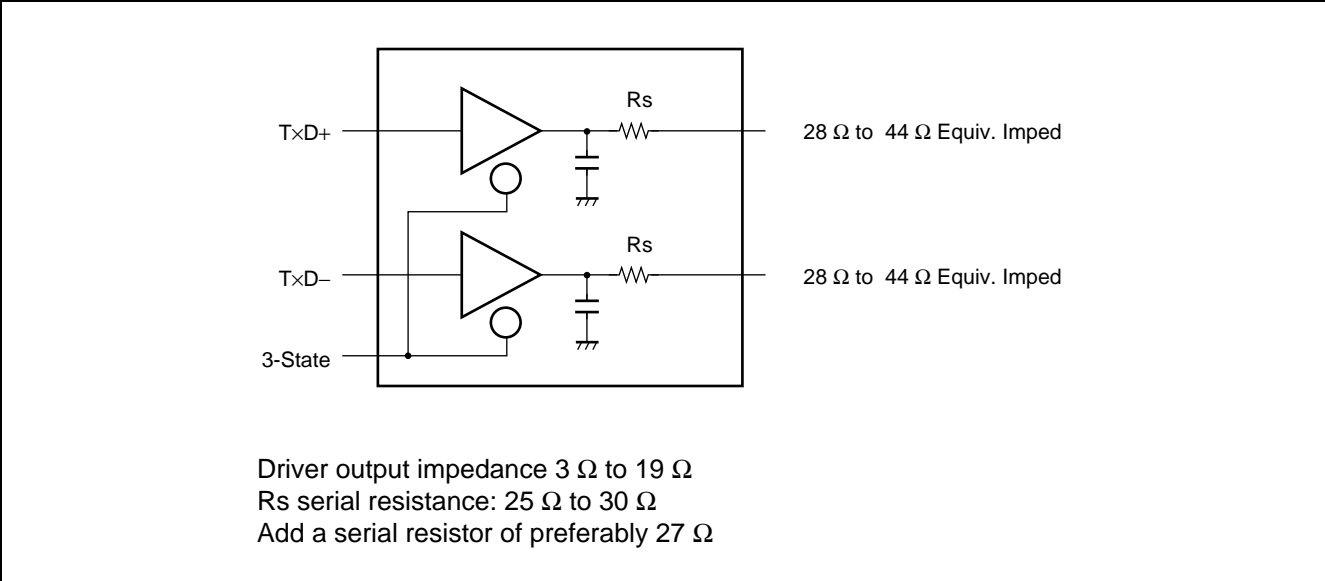
These are defined as the times between 10% to 90% of the output signal voltage.

For the full-speed buffer, t_{UTFR} and t_{UTFF} are specified such that the t_{UTFR}/t_{UTFF} ratio falls within $\pm 10\%$ to minimize RFI radiation.

*3 : About driver characteristics ZDRV

USB full-speed connection is performed via a shielded twisted-pair cable at a characteristic impedance of $90 \Omega \pm 15\%$. The USB Standard stipulates that the USB driver's output impedance must be within the range of 28Ω to 44Ω . The USB Standard also stipulates that a discrete serial resistor (R_s) must be added to have balance while satisfying the above standard.

The output impedance of the USB I/O buffer on this LSI is about 3Ω to 19Ω . Therefore, serial resistor R_s to be added must be 25Ω to 30Ω (27Ω recommended) .



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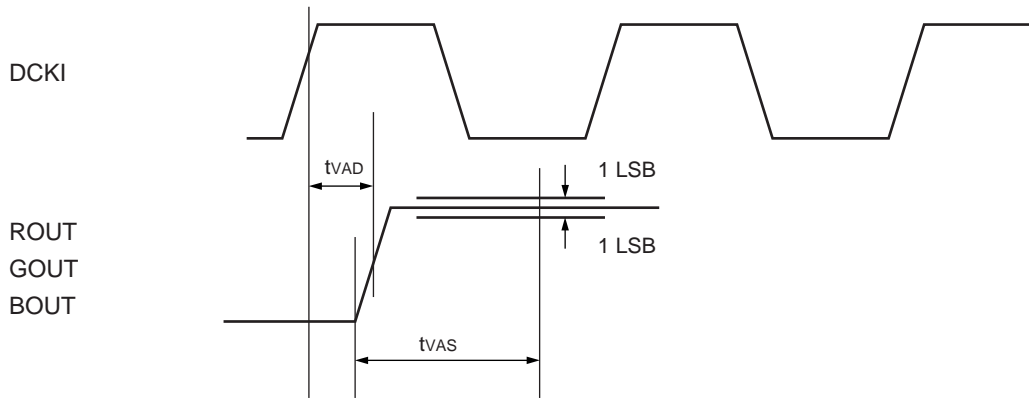
(7) Analog RGB

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Analog RGB output delay	t_{VAD}	ROUT, GOUT, BOUT	$V_{REF} = 1.1\text{ V}$, $V_{DDR} = V_{DDG} =$	—	12	—	ns	50 MHz (Max)
Analog RGB output settling time	t_{VAS}	ROUT, GOUT, BOUT	$V_{DDB} = 2.5\text{ V}$, $V_{RO}^* = 2.7\text{ k}\Omega$	—	—	20	ns	

* : V_{RO} is an external resistor for DAC.

- Display signal output timing



(8) Digital RGB

Vertical synchronous, horizontal synchronous, and display output control signal input timing

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Horizontal sync signal cycle time	t_{HCYC}	HSYNC1 to HSYNC3	$100 + t_{WH}$	—	Dot clock	
Horizontal sync signal pulse width	t_{WH}	HSYNC1 to HSYNC3	20	—	Dot clock	*1
			—	6	μs	
Horizontal sync signal setup time	t_{DHST}	HSYNC1 to HSYNC3	4	—	ns	
Horizontal sync signal hold time	t_{DHHD}		0	—	ns	
Vertical sync signal setup time	t_{HVST}	VSYNC	5	$1H^{*2} - 5$	Dot clock	
Vertical sync signal hold time	t_{HVHD}		3	—	H^{*2}	
Input sync signal rise/fall time	t_{DR} t_{DF}	HSYNC1 to HSYNC3, VSYNC	—	2	ns	

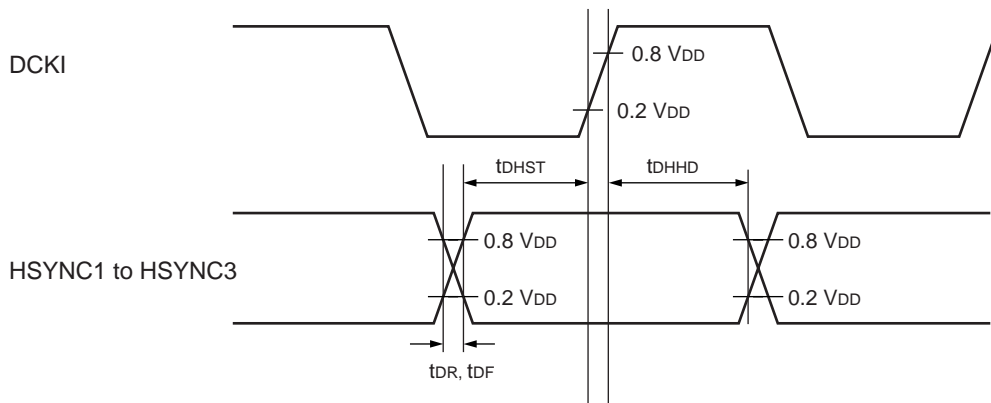
*1 : During the horizontal sync signal pulse period, the device stops its internal OSDC operation, disabling writing to the internal VRAM. Therefore, set the horizontal sync signal pulse width and VRAM write cycle to ensure that : horizontal sync signal pulse width < VRAM write cycle.

Precisely, adjust the command issuance interval not to issue command 2 or command 4 (VRAM write command) more than twice in the horizontal sync signal pulse width period.

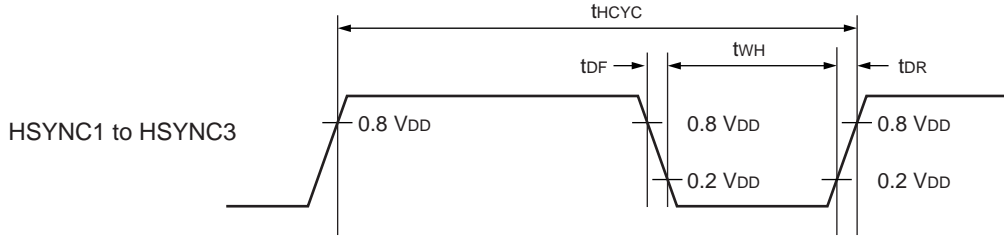
If the above condition is not satisfied, the device may fail writing to VRAM.

2 : 1H is assumed to be one horizontal sync signal period.

- Horizontal sync signal, display output control signal input timing

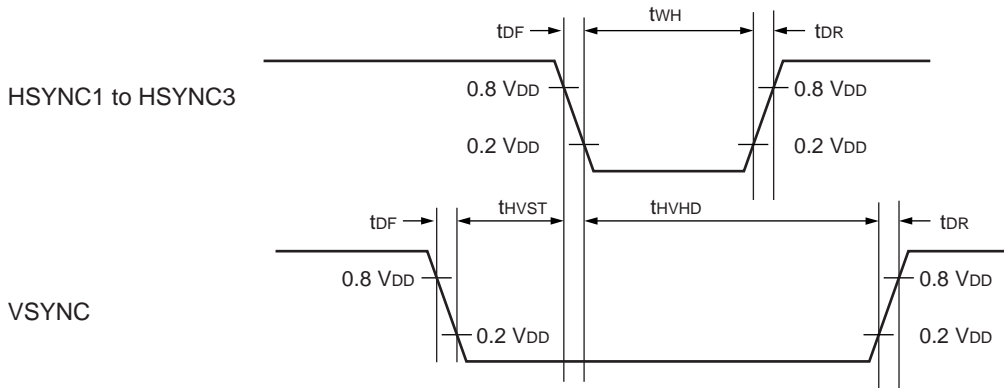


- Horizontal sync signal input

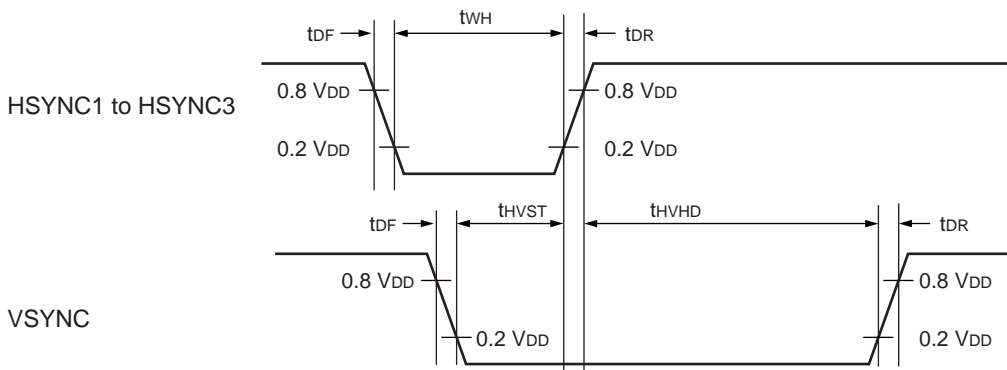


- Vertical sync signal input timing

- VSYNC detection at the leading edge of HSYNC



- VSYNC detection at the trailing edge of HSYNC



(9) Display signal timing

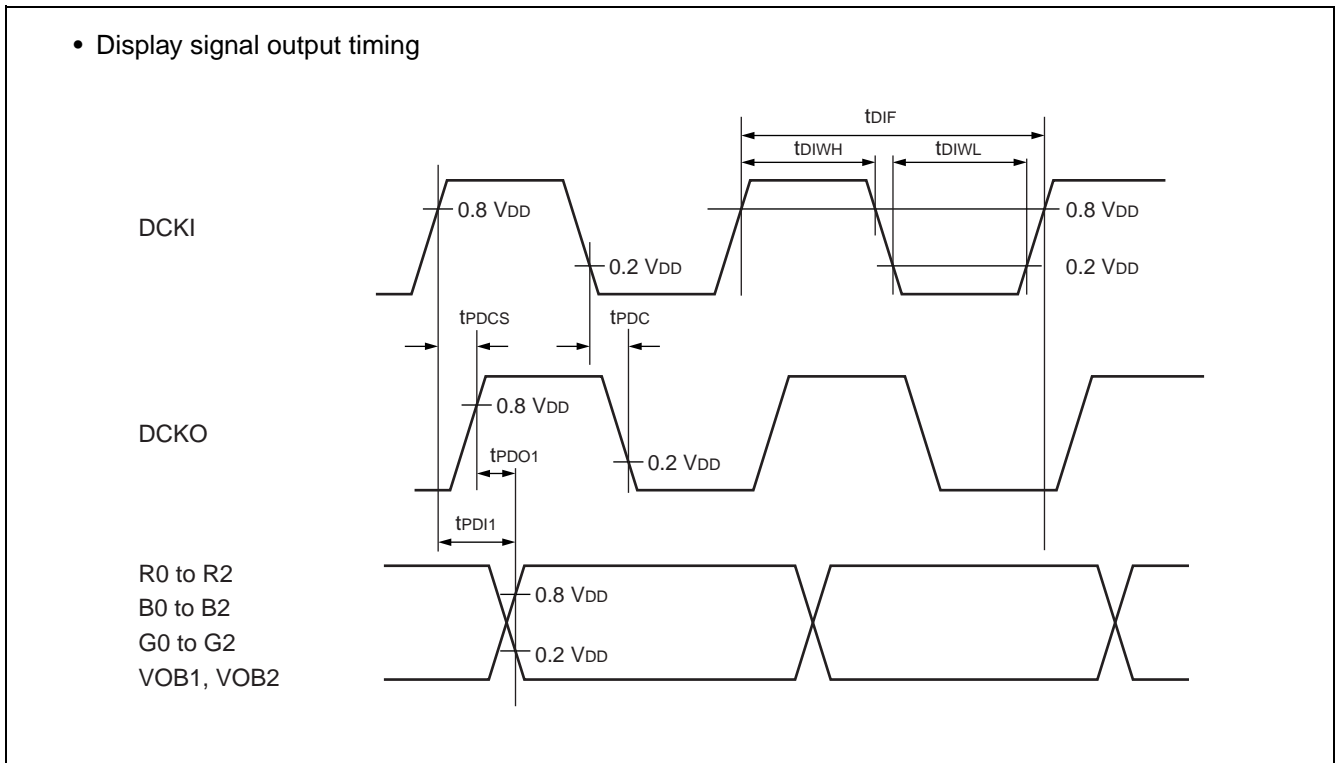
($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Dot clock cycle time	t_{DIF}	DCKI	11	90	MHz	*1
Dot clock pulse time	t_{DIWH}	DCKI	5	—	ns	*1
	t_{DIWL}		5	—	ns	
Dot clock output delay time 1	t_{PDC}	DCKO	3	8	ns	*2
Display signal output delay time I1	t_{PDI1}	R0 to R2, B0 to B2, G0 to G2, VOB1, VOB2	2	8	ns	*2
Display signal output delay time O1	t_{PDO1}	R0 to R2, B0 to B2, G0 to G2, VOB1, VOB2	-4	5	ns	*2

*1 : Input a continuous dot clock signal without a break.

*2 : Output load 16 pF

Note : The actual display output varies depending on how the display output/position is controlled for each display layer.



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(10-a) External circuit for data slicer

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

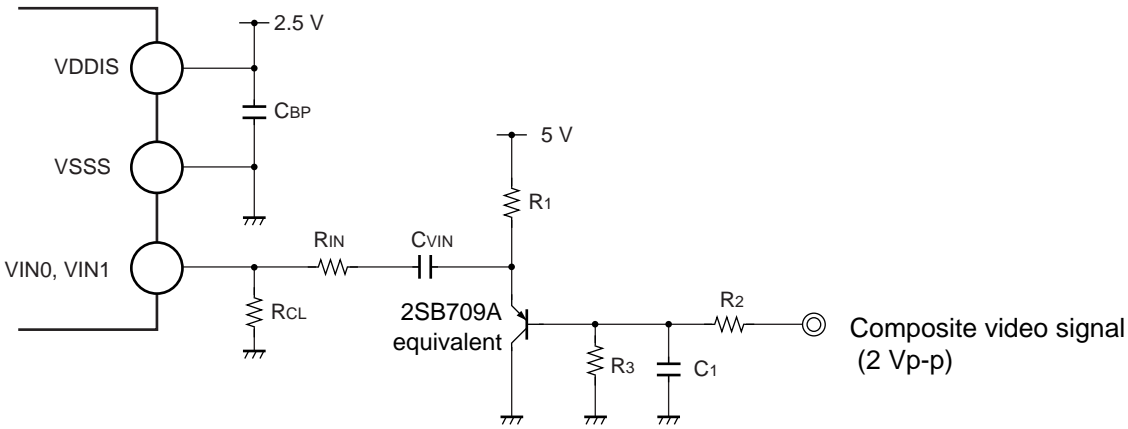
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Video signal input level	V_{VIN}	VIN0, VIN1	1.0	—	1.5	Vp-p	

(10-b) External circuit for data slicer

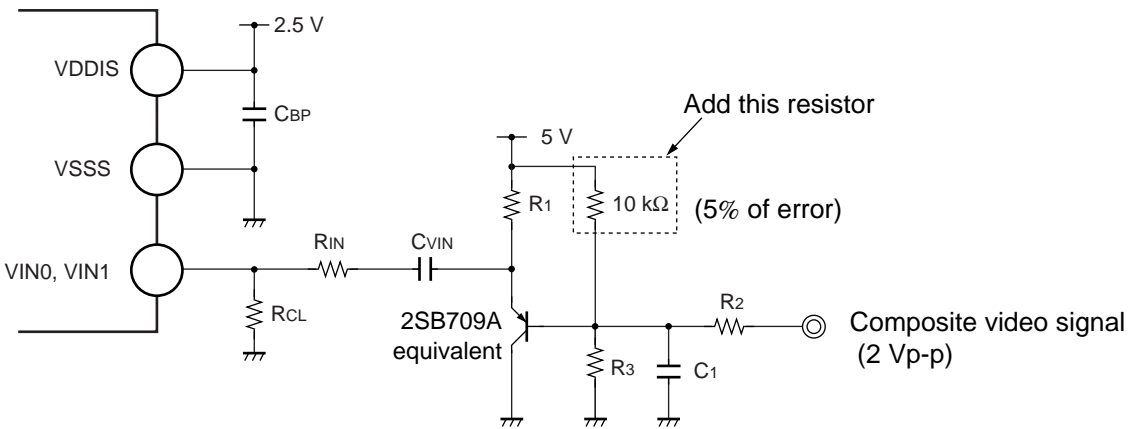
($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Coupling condenser for VIN pin	C_{VIN}	VIN0, VIN1	—	—	0.1	μF	More than B features 10% of error Ceramic condenser
Resistor for clamp	R_{CL}	VIN0, VIN1	—	—	1	$\text{M}\Omega$	5% of error
Input resistance for VIN pin	R_{IN}	VIN0, VIN1	—	—	0	Ω	5% of error
Condenser of low pass filter for VIN	C_1	—	—	—	82	pF	More than B features 10% of error Ceramic condenser
Power supply bypass condenser	C_{BP}	VDDIS, VSSS	—	—	0.1	μF	Ceramic condenser
Resistance for video signal input buffer	R_1	—	—	—	2.2	$\text{k}\Omega$	5% of error
Video signal input level correcting resistor	R_2	—	—	—	4.7	$\text{k}\Omega$	5% of error
Video signal input level correcting resistor	R_3	—	—	10	12	$\text{k}\Omega$	5% of error

(1) When the input composite video signals have been DC clamped



(2) When the input composite video signals have not been DC clamped



External recommended circuit for data slicer

MB91319 Series

(11) I²C timing

- At master mode operating

(Ta = -10 °C to +70 °C, V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 2.5 V ± 0.2 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Typical mode		High-speed mode* ³		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	R = 1 kΩ C = 50 pF* ⁴	0	100	0	400	kHz	
“L” period of SCL clock	t _{LOW}		4.7	—	1.3	—	μs	
“H” period of SCL clock	t _{HIGH}		4.0	—	0.6	—	μs	
Bus free time between [STOP condition] and [START condition]	t _{BUS}		4.7	—	1.3	—	μs	
SCL↓ → SDA output delay time	t _{DLDAT}		—	5 × M* ¹	—	5 × M* ¹	ns	
Setup time of [repeat START condition] SCL↑ → SDA↓	t _{SUSTA}		4.7	—	0.6	—	μs	
Hold time of [repeat START condition] SDA↓ → SCL↓	t _{HDSTA}		4.0	—	0.6	—	μs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL↑ → SDA↑	t _{SUSTO}		4.0	—	0.6	—	μs	
SDA data input hold time (vs. SCL↓)	t _{HDDAT}		2 × M* ¹	—	2 × M* ¹	—	μs	
SDA data input setup time (vs. SCL↑)	t _{SUDAT}		250	—	100* ²	—	ns	

*1 : M = Resource clock cycle (ns)

*2 : A Fast-mode I²C bus device can be used for a standard mode I²C bus system as long as the device satisfies a requirement of “t_{SUDAT} ≥ 250 ns”.

When the device does not extend the “L” period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

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- At slave mode operating

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*3		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	R = 1 k Ω C = 50 pF*4	0	100	0	400	kHz	
“L” period of SCL clock	t_{LOW}		4.7	—	1.3	—	μs	
“H” period of SCL clock	t_{HIGH}		4.0	—	0.6	—	μs	
SCL $\downarrow \rightarrow$ SDA output delay time	t_{DLDAT}		—	$5 \times M^{*1}$	—	$5 \times M^{*1}$	ns	
Bus free time between [STOP condition and START condition]	t_{BUS}		4.7	—	1.3	—	μs	
SDA data input hold time (vs. SCL \downarrow)	t_{HDDAT}		$2 \times M^{*1}$	—	$2 \times M^{*1}$	—	μs	
SDA data input setup time (vs. SCL \uparrow)	t_{SUDAT}		250	—	100^{*2}	—	ns	
Setup time of [repeat START condition] SCL $\uparrow \rightarrow$ SDA \downarrow	t_{SUSTA}		4.7	—	0.6	—	μs	
Hold time of [repeat START condition] SDA $\downarrow \rightarrow$ SCL \downarrow	t_{HDSTA}		4.0	—	0.6	—	μs	After that, the first clock pulse is generated.
Setup time of [STOP condition] SCL $\uparrow \rightarrow$ SDA \uparrow	t_{SUSTO}		4.0	—	0.6	—	μs	

*1 : M = Resource clock cycle (ns)

*2 : A Fast-mode I²C bus device can be used for a standard mode I²C bus system as long as the device satisfies a requirement of “ $t_{SUDAT} \geq 250\text{ ns}$ ”.

When the device does not extend the “L” period of the SCL signal, the next data must be outputted to the SDA line within 1250 ns (maximum SDA/SCL rise time + t_{SUDAT}) in which the SCL line is released.

*3 : For use at over 100 kHz, set the resource clock to at least 6 MHz.

*4 : R and C represent the pull-up resistor and load capacitor of the SCL and SDA output lines.

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5. 0.25 μm Technology About the Power-on Sequence for Dual-power-supply Models

- The power supplies must be turned on in the VDDI \rightarrow AVCC, AVRH, VDDE order and off in the VDDE \rightarrow AVCC, AVRH, VDDI order.

6. Electrical Characteristics for the A/D Converter

($T_a = -10\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$, $V_{DDE} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{DDI} = 2.5\text{ V} \pm 0.2\text{ V}$, $V_{SS} = 0\text{ V}$,
 $V_{SSE} = V_{SSI} = AV_{SS} = 0\text{ V}$, $AVRH = 3.0\text{ V}$ to 3.6 V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Resolution	—	—	10	bit	
Total error*1	- 5.5	—	+ 5.5	LSB	AV _{CC} = 3.3 V, AVRH = 3.3 V (at CPU sleep)
Nonlinear error*1	- 3.5	—	+ 3.5	LSB	
Differential linear error*1	- 2.0	—	+ 2.0	LSB	
Zero transition voltage*1	- 4.0	—	+ 6.0	LSB	
Full transition voltage*1	AVRH - 5.5	—	AVRH + 3.0	LSB	
Conversion time	10*2	—	—	μs	
Power supply voltage (analog + digital)	—	3.6	—	mA	
	—	—	5	μA	At stop converting
Reference power supply current (between AVRH and AVRL)	—	470	—	μA	AVRH = 3.0 V, AVRL = 0.0 V
	—	—	10	μA	At stop converting
Analog input capacitance	—	40	—	pF	
Interchannel disparity	—	—	4	LSB	

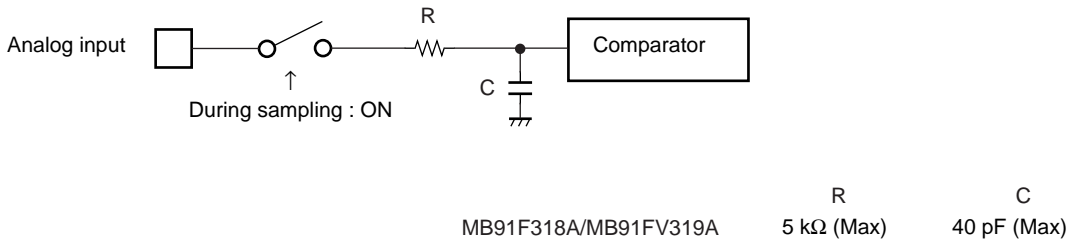
*1 : Measured in the CPU sleep state

*2 : Depends on the clock cycle of the clock signal supplied to peripheral resources.

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

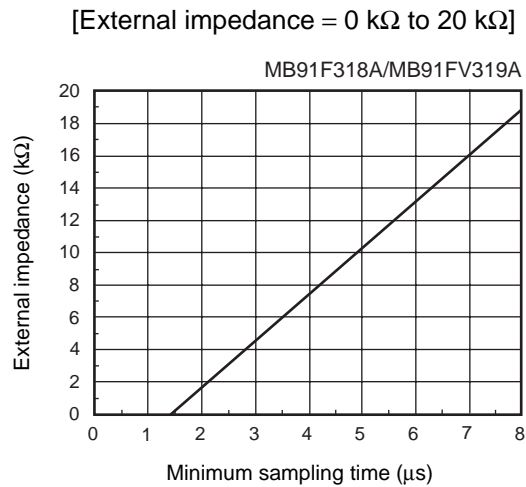
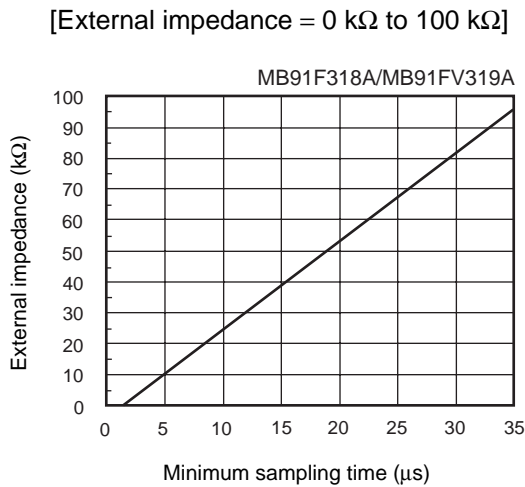
• Analog input circuit model



Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

• The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• About errors

- As $|AVRH - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

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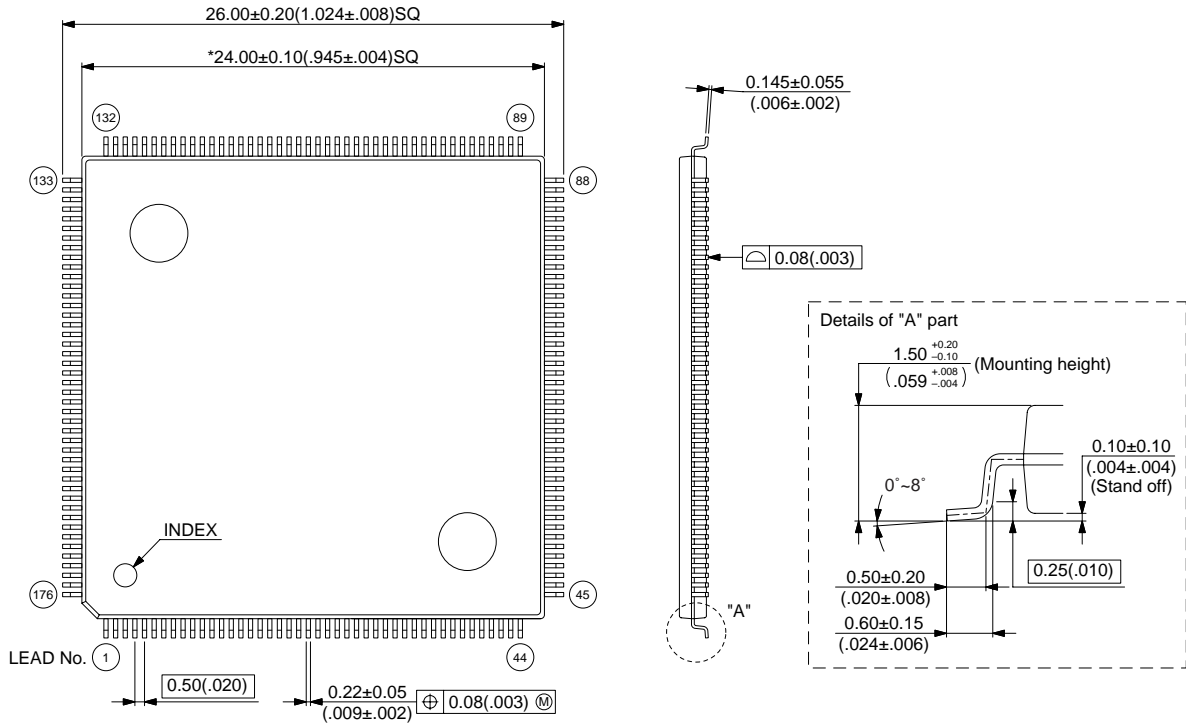
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91FV319APMT-ES	176-pin plastic LQFP (FPT-176P-M07)	For developing tool

■ PACKAGE DIMENSION

176-pin plastic LQFP
(FPT-176P-M07)

- Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25 (.010) Max (each side) .
- Note 2) Pins width and pins thickness include plating thickness
- Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

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