Ordering number : ENA0207

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA1652C — Time Code Reception IC

Overview

The LA1652C time code reception IC receives long-wave time standard broadcasts (such as the Japanese JJY and German DCF77 standards) and detects and outputs the time code superposed on the long-wave signal. Applications can automatically correct their clock's time setting by using the time code received by the LA1652C. Note that the LA1652C is a bare chip product that is not packaged.

Functions

- RF amplifier, rectifier, detector, time code output, and standby circuit.

Features

- Low-voltage operation (operating V_{CC} as low as 1.8V).
- Standby mode current drain less than or equal to 0.1μA.
  Japan : JJY 40/60kHz
  Germany : DCF77 77.5kHz

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.0	V
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage	V_{CC}			3.0		V
Operating supply voltage range	V_{CC} op		1.8		3.6	V

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Characteristics at Ta = 25°C, V_{CC} = 3.0V

* : Packaged in an SSOP16 package and measured using the IC51-0162-911 socket (Yamaichi Electronics Co., Ltd.)

Overall Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	No input		55	70	μA
Standby mode current drain	I_{STB}	PAD15 = 3.0V		0.01	0.1	μA

Amplifier Input Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input impedance	Z_I	PAD1		2.0		MΩ
Input frequency range	F_{IN}		37.5		80.0	kHz
Minimum input voltage	V_{MIN}	PAD1 input level		1	2	μVrms
Maximum input voltage	V_{MAX}	PAD1 input level	50	100		mVrms

TCO Output Characteristics - Input pad = PAD1, fin = 40kHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level output voltage	V_{OH}		2.90	2.95		V
Low-level output voltage	V_{OL}			0.05	0.10	V
Output pulse width (500 ms input)	T500	V_{IN} = 0 to 100dBμV, AM modulation (1Hz square wave, duty = 50%, 10:1 modulation)	350	450	550	ms
Output pulse width (800 ms input)	T800	V_{IN} = 0 to 100dBμV, AM modulation (1Hz square wave, duty = 80%, 10:1 modulation)	650	750	850	ms
Output pulse width (200 ms input)	T200	V_{IN} = 0 to 100dBμV, AM modulation (1Hz square wave, duty = 20%, 10:1 modulation)	100	200	300	ms

Chip Specifications

Parameter	Conditions	Ratings	Unit
Chip size		1.73×2.60	mm^2
Chip thickness		330(±20)	μm
Pad size		140×140	μm^2
Pad opening		115×115	μm^2

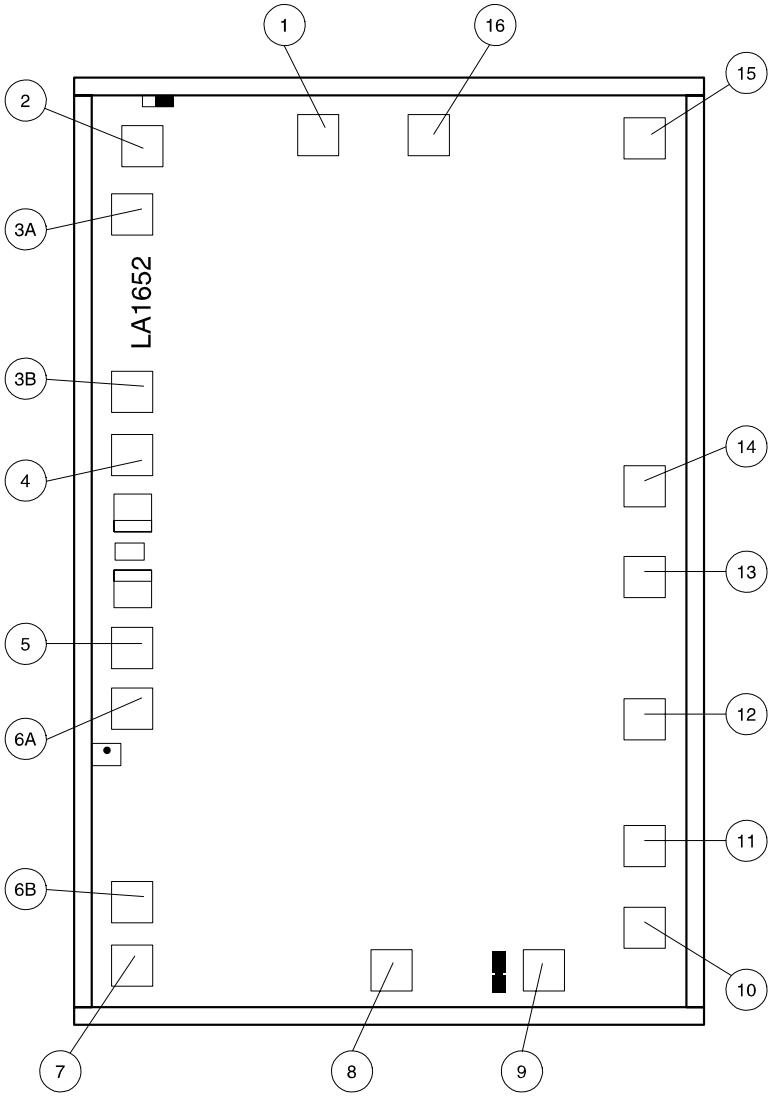
PAD Coordinates

PAD	X-Axis	Y-Axis	PAD	X-Axis	Y-Axis
P1	664	150	P9	1293	2450
P2	180	180	P10	1580	2330
P3A	150	864	P11	1580	2103
P3B	150	372	P12	1580	1754
P4	150	1034	P13	1580	1360
P5	150	1563	P14	1580	1108
P6A	150	2269	P15	1570	160
P6B	150	1733	P16	974	150
P7	160	2440			
P8	876	2450			

Notes

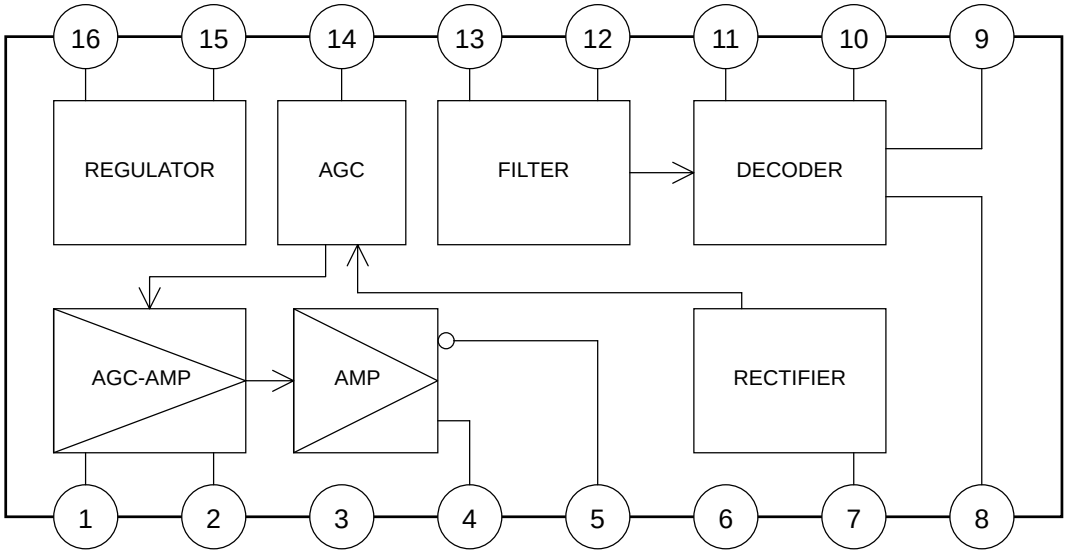
1. The left upper corner of the Pad Layout Diagram on the following page is the origin, the X axis increases to the right and the Y axis increases in the downward direction.
2. Units : μm
3. The pad coordinates give the coordinate values of the center of the pads.
4. Both of each of the pairs P3A/P3B (V_{CC}) and P6A/P6B (ground) must be bonded.

Pad Layout Diagram



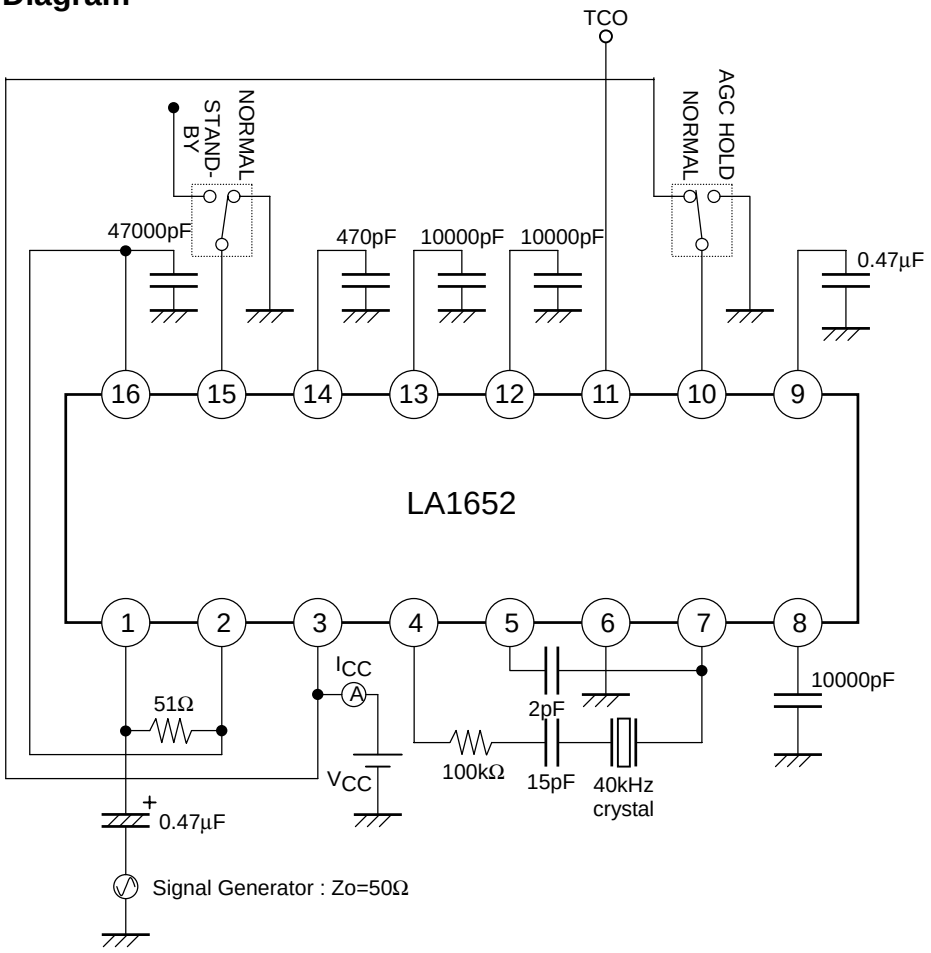
PCA00615

Block Diagram



PCA00616

Test Circuit Diagram



PCA00617