

## CMOS Switched-Capacitor Voltage Converter

### Features

- Simple conversion of  $V_{DD}$  to  $-V_{DD}$
- Cascade connection (two devices are connected,  $V_{OUT} = -2 V_{DD}$ )
- Boost pin for higher switching frequency
- Easy to use
  - Requires only two external capacitors
- No external diode required
- Typically with no load voltage conversion, 99.9% efficiency
- Typical power efficiency is 98%
- Wide operating voltage range: 3V to 12V
- 8-pin DIP/SOP package

### Applications

- RS-232 power supply
- On board negative supply for dynamic RAMS
- Supply voltage splitter,  $V_O = \pm V_{DD}/2$
- Operation amplifier supply
- Data acquisition systems
- Positive voltage doubler

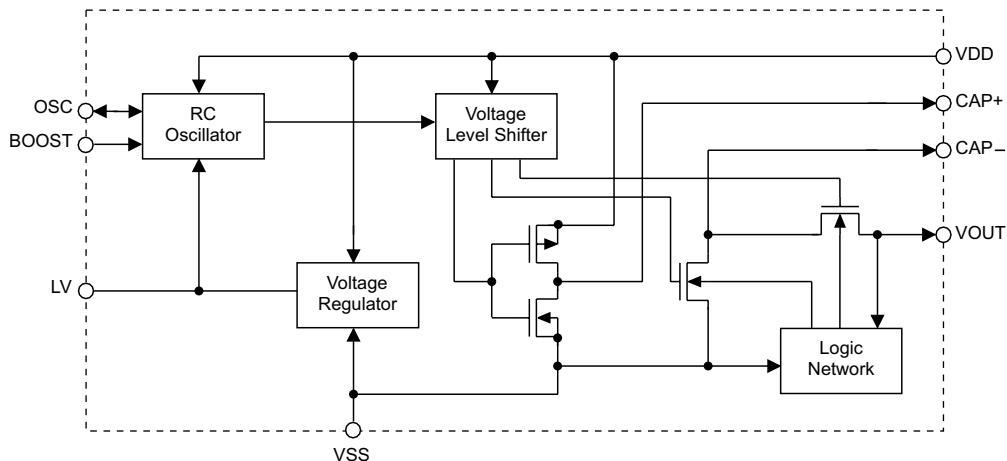
### General Description

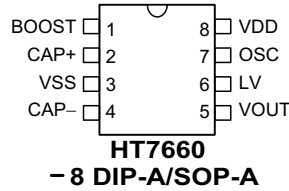
HT7660 is a monolithic CMOS switched-capacitor voltage converter. HT7660 is designed to complete a voltage conversion from positive to negative. The only required external components are two low cost electrolytic capacitors.

HT7660 includes a voltage regulator, an RC oscillator and four output power MOS switches. The frequency of

an RC oscillator can be lowered by adding an external capacitor between  $V_{DD}$  and the OSC pin, or an external clock can be connected to the OSC pin to replace the original oscillator. The LV terminal may be tied to VSS to disable the voltage regulator. By doing this, low voltage operation can be improved.

### Block Diagram



**Pin Assignment**

**Pin Description**

Pin No.	Pin Name	I/O	Internal Connection	Description
1	BOOST	I	CMOS Pull-low	Higher switching frequency selection input
2	CAP+	O	CMOS	This pin is connected to the positive terminal of Capacitor C1 for a charge pump
3	VSS	—	—	Negative power supply, ground
4	CAP-	O	NMOS	This pin is connected to the negative terminal of Capacitor C1 for a charge pump
5	VOUT	O	NMOS	This pin is connected to the negative terminal of Capacitor C2 for charge reservoir. Output voltage pass through this pin
6	LV	I	—	Floating this pin enables the voltage regulator. Connect this pin to VSS (Ground) to bypass voltage regulator and improve low voltage operation
7	OSC	I/O	Transmission Gate	External clock input pin. This pin can be connected with an external capacitor to reduce switching frequency
8	VDD	—	—	Positive power supply

**Absolute Maximum Ratings**

Supply Voltage ..... $V_{SS}-0.3V$  to  $V_{SS}+13V$       Operating Temperature ..... $-40^{\circ}C$  to  $85^{\circ}C$   
 Storage Temperature ..... $-50^{\circ}C$  to  $125^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**Electrical Characteristics**
 $T_a=25^{\circ}C$ 

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		$V_{DD}$	Conditions				
$V_{DD}$	Operating Voltage	—	—	3	—	12	V
$I_{STB}$	Standby Current	3V	No load	—	26	100	$\mu A$
		5V		—	80	160	
$f_{OSC}$	System Frequency	3V	—	2.5	4	—	kHz
		5V		5	10	—	
$R_{OUT}$	Output Source Resistance	3V	$I_{OUT}=10mA$	—	97	150	$\Omega$
		5V	$I_{OUT}=20mA$	—	60	100	
$V_{CON-EFF}$	Voltage Conversion Efficiency	3V	No load	99	—	—	%
		5V		99	99.9	—	
$P_{EFF}$	Power Efficiency	3V	$R_L=5k\Omega$	96	—	—	%
		5V		96	98	—	

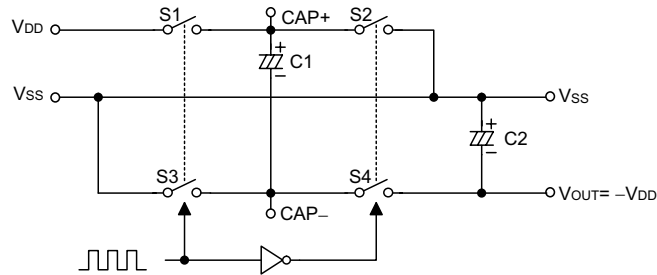
**Functional Description**

HT7660 needs only two external polarized electrolytic capacitors to complete a negative voltage converter.

HT7660 has four MOS power switches: S1, S2, S3 and S4. For the first half cycle, when S2 and S4 are open, Capacitor C1 is charged to a voltage  $V_{DD}$  through S1 and S3. During the second half cycle, when S1 and S3 are open, the charge on Capacitor C1 is shifted to Capacitor C2 through S2 and S4. Thereby, the voltage across Capacitor C2 is  $V_{DD}$ . Because the positive terminal of C2 is connected to  $V_{SS}$ , we get a  $-V_{DD}$  voltage at  $V_{OUT}$  pin.

For high voltage operation, the LV pin is left floating to enable the voltage regulator. This can reduce the current consumption of the RC oscillator, and thus get a fixed switching frequency  $f_{OSC}$  with high voltage range. For low voltage operation, the LV pin is connected to  $V_{SS}$  to bypass the voltage regulator of which inherent voltage drop can degrade the operation at low voltages.

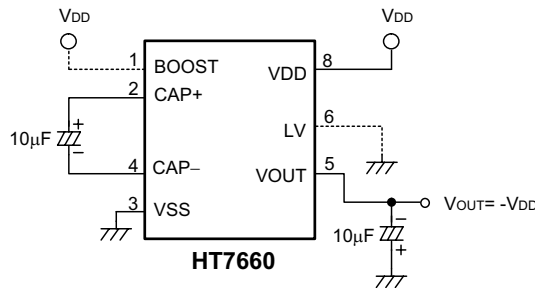
A capacitor may be connected between  $V_{DD}$  and pin OSC to lower the switching  $f_{OSC}$ , and an external clock may be added to replace the built-in RC oscillator.



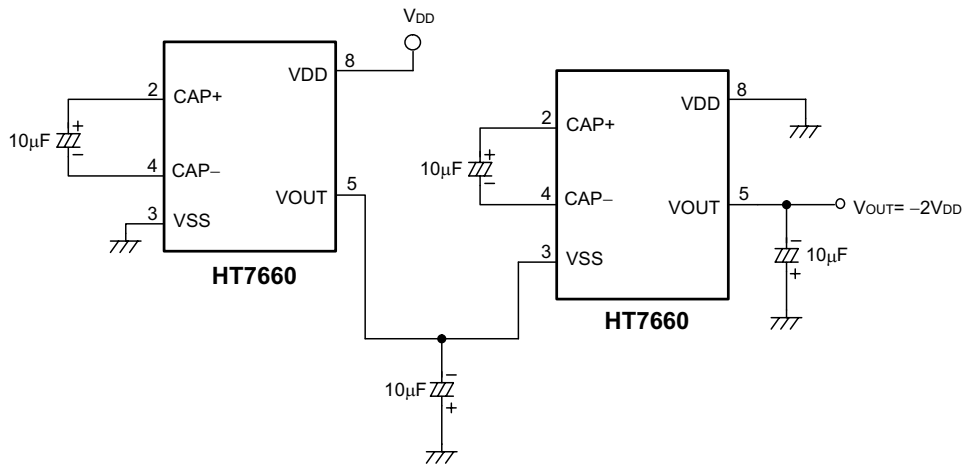
The operating mode of HT7660

**Application Circuits**

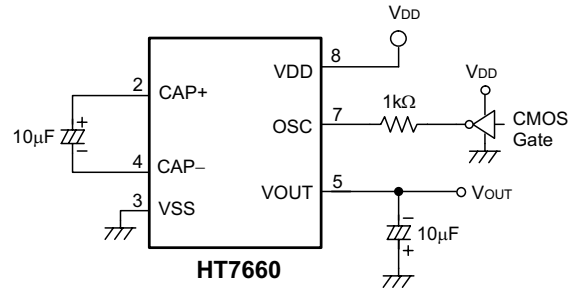
**Simple Negative Voltage Converter**



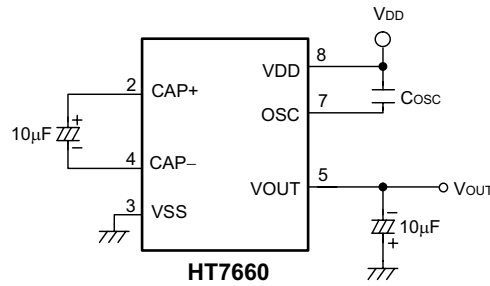
**Simple Voltage Multiplier**



**External Switching Frequency**

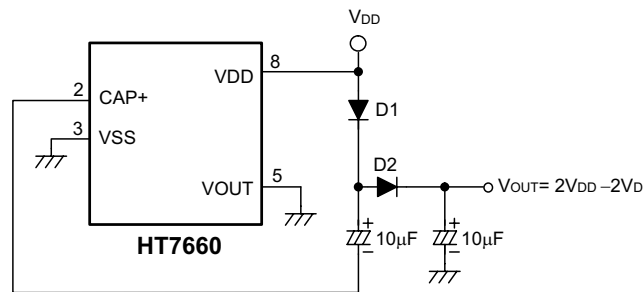


**Lower Switching Frequency**



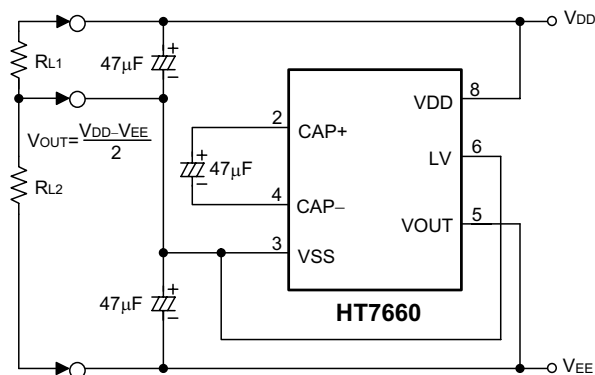
Note:  $C_{osc}$  is tens of pico farad

**Positive Voltage Doubler**

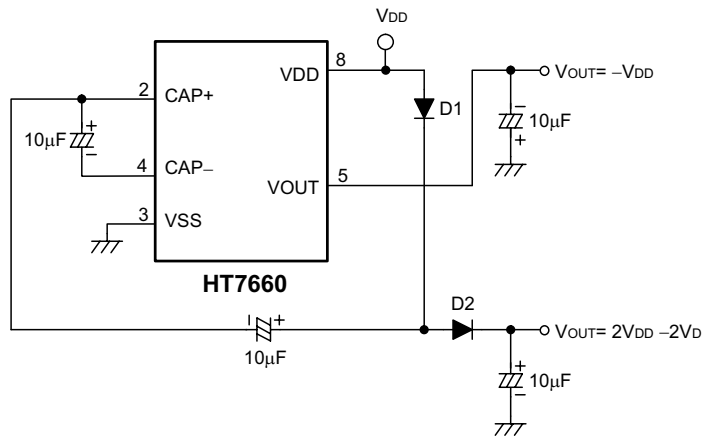


Note:  $V_d$  is forward voltage drop of diode D1 and D2

**Voltage Splitter**



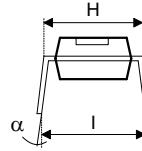
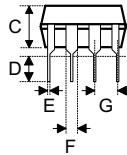
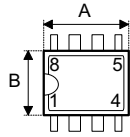
Combined Negative Voltage Converter and Positive Voltage Doubler



Note:  $V_d$  is forward voltage drop of diode D1 and D2

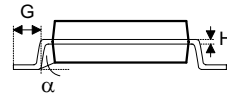
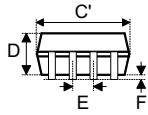
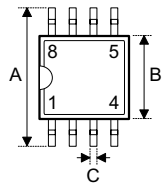
**Package Information**

**8-pin DIP (300mil) Outline Dimensions**



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
$\alpha$	0°	—	15°

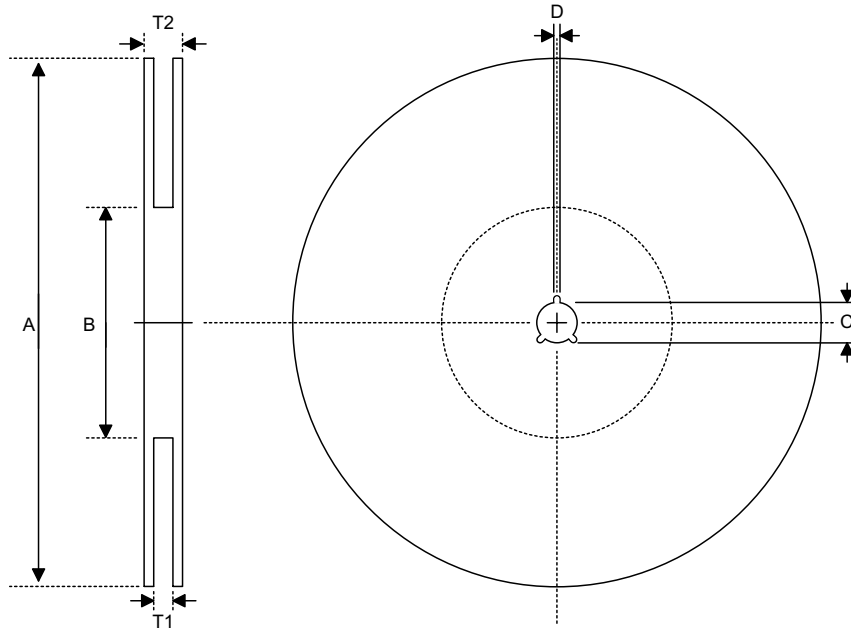
**8-pin SOP (150mil) Outline Dimensions**



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C'	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
$\alpha$	0°	—	10°

**Product Tape and Reel Specifications**

**Reel Dimensions**

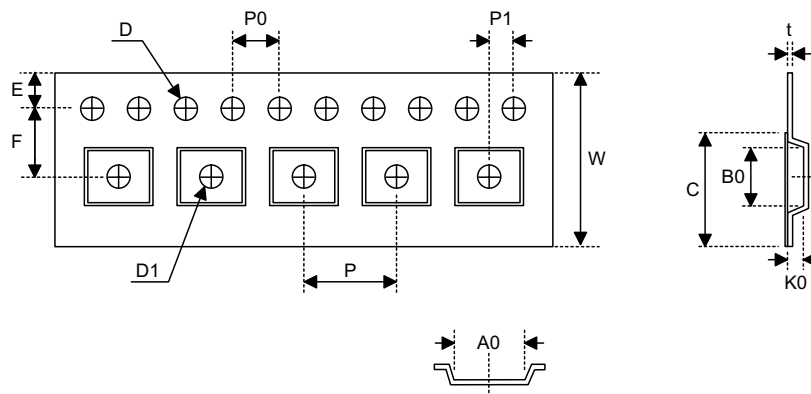


SOP 8N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 -0.2
D	Key Slit Width	2.0±0.15
T1	Space Between Flange	12.8+0.3 -0.2
T2	Reel Thickness	18.2±0.2



**Carrier Tape Dimensions**



**SOP 8N**

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 -0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

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