

## Features

July 2003

- Extremely fast turn-on
- Very small size and very low leakage
- 5, 6 and 7 terminals available
- Standard delivery form: solder bumped die
- Facilitates compliance with EN-45502 and EN-50061

### Ordering Information

ZL70002/UDJ Bumped Die, Waffle Tray  
 ZL70008/UDJ Bumped Die, Waffle Tray  
 ZL70009/UDJ Bumped Die, Waffle Tray  
 ZL70010/UDJ Bumped Die, Waffle Tray  
**0 to +55°C**

## Superior Quality

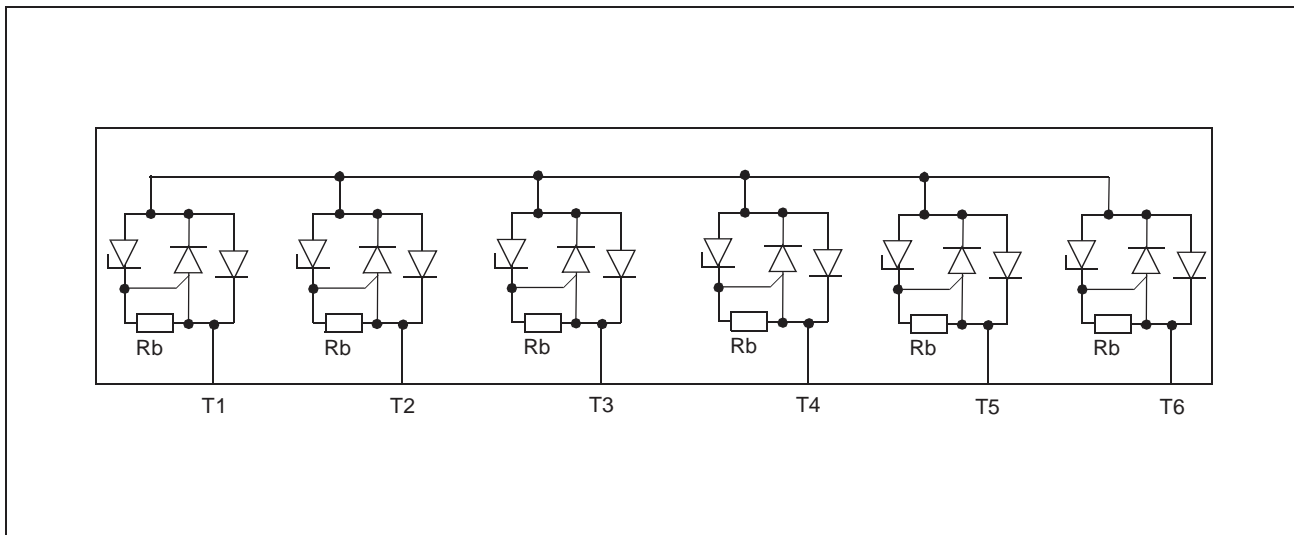
- QA procedures based on MIL-PRF-38535
- Traceability for every chip to lot and wafer number
- 100% burn-in capability

## Description

The ZL70002/08/09/10 family are high performance surge protection devices targeted for medical applications.

## Applications

- Pacemakers, Implantable Cardioverter Defibrillators (ICDs), Neurostimulators, Bladder Control Devices
- Medical devices with electronics requiring protection against a high voltage surge



**Figure 1 - ZL70010 Block Diagram**

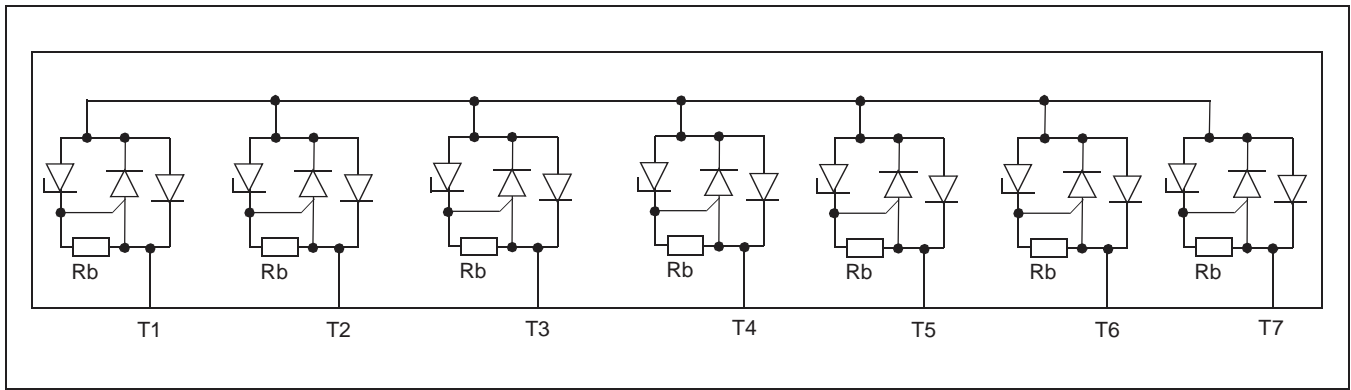


Figure 2 - ZL70002 Block Diagram

Pin Description Table - ZL70010 and ZL70002

Pin #	In/Output	Name	Description
1	I	T1	Transient Surge Protection Terminal 1
2	I	T2	Transient Surge Protection Terminal 2
3	I	T3	Transient Surge Protection Terminal 3
4	I	T4	Transient Surge Protection Terminal 4
5	I	T5	Transient Surge Protection Terminal 5
6	I	T6	Transient Surge Protection Terminal 6
7	I	T7	Transient Surge Protection Terminal 7 (ZL70002 only)

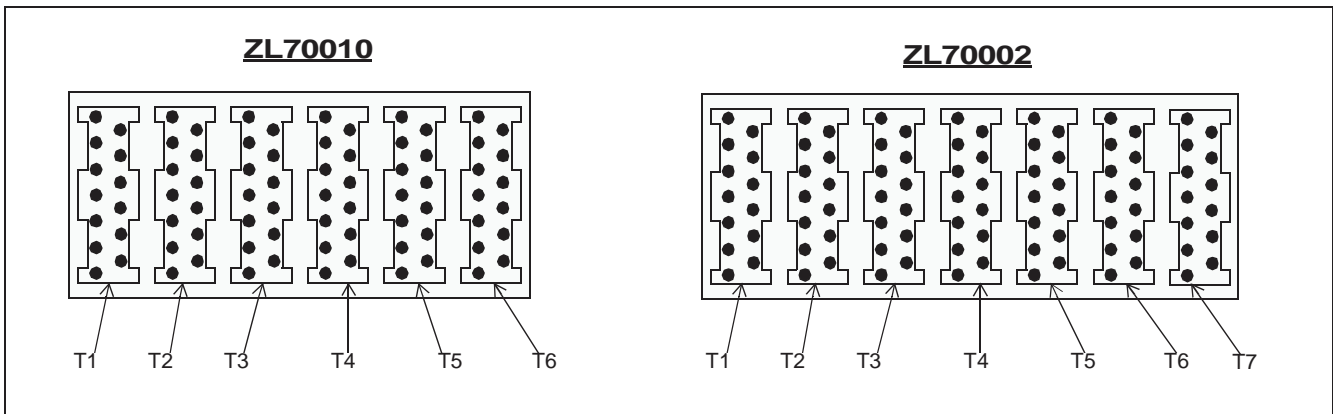


Figure 3 - ZL70010 and ZL70002 Bumped Chip Appearance

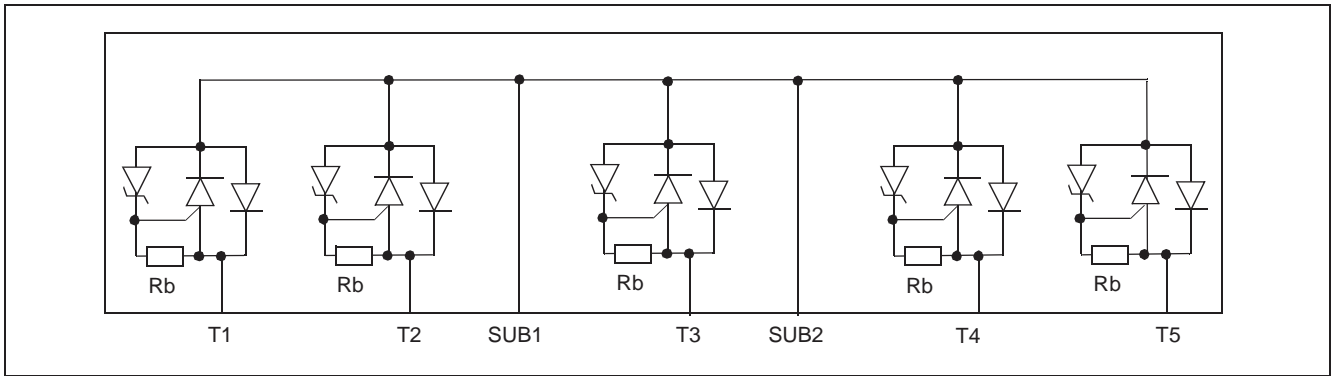


Figure 4 - ZL0008/ZL0009 Block Diagram

Pin Description Table - ZL0008 and ZL0009

Pin #	In/Output	Name	Description
1	I	T1	Transient Surge Protection Terminal 1
2	I	T2	Transient Surge Protection Terminal 2
3	I/O	SUB1	Transient Surge Protection Substrate Connection 1
4	I	T3	Transient Surge Protection Terminal 3 Doubled Area
5	I/O	SUB2	Transient Surge Protection Substrate Connection 2
6	I	T4	Transient Surge Protection Terminal 4
7	I	T5	Transient Surge Protection Terminal 5

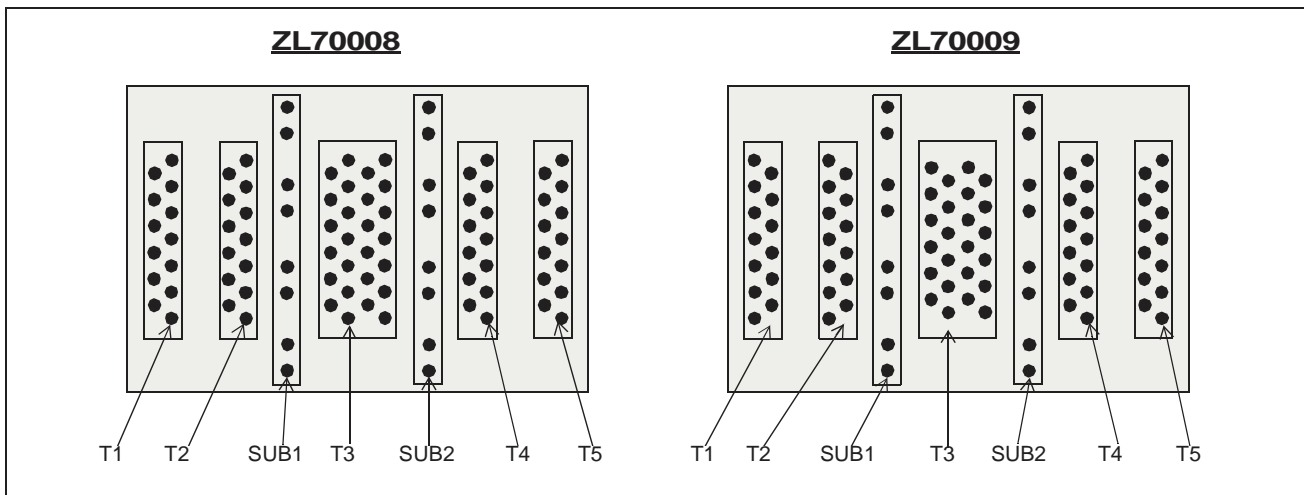


Figure 5 - ZL70008 and ZL70009 Bumped Chip Appearance

**1.0 Functional Description**

The ZL70002/08/09/10 is a family of transient surge suppressing devices designed specifically for implanted medical devices. The device terminals have an extremely low leakage during normal voltages and can therefore be connected in parallel with the pins of the device it protects. When the voltage rises to dangerous level it then rapidly turns on and limits the voltage by shunting the current through its thyristors. This makes the ZL70002/08/09/10 family an effective means of compliance with international regulations EN-45502, "Active implantable" and the EN-50061 "Safety of Implantable Cardiac Pacemakers".

**1.1 ZL70010**

ZL70010 is a six-branch device. The suppression is achieved by a self-triggering thyristor-diode device in parallel with a diode between each branch-input and a common node which also is the substrate of the device. The six branches of the device are reached through terminals T1, T2, T3, T4, T5 and T6. The electrical characteristic observed between any two of the terminals (T1, T2, T3, T4, T5 and T6) very much resembles that of a DIAC, see Figure 12.

When a transient current is forced between two branch-input terminals, the positive terminal will be clamped to the common node by the diode of one branch and the negative terminal to the forward voltage of the thyristor-diode of the other branch. Due to the low on-state voltage of the thyristor that voltage will stay at a safe value during the transient.

**1.2 ZL70002**

ZL70002 is a seven-branch device with exactly the same electrical characteristics as ZL70010.

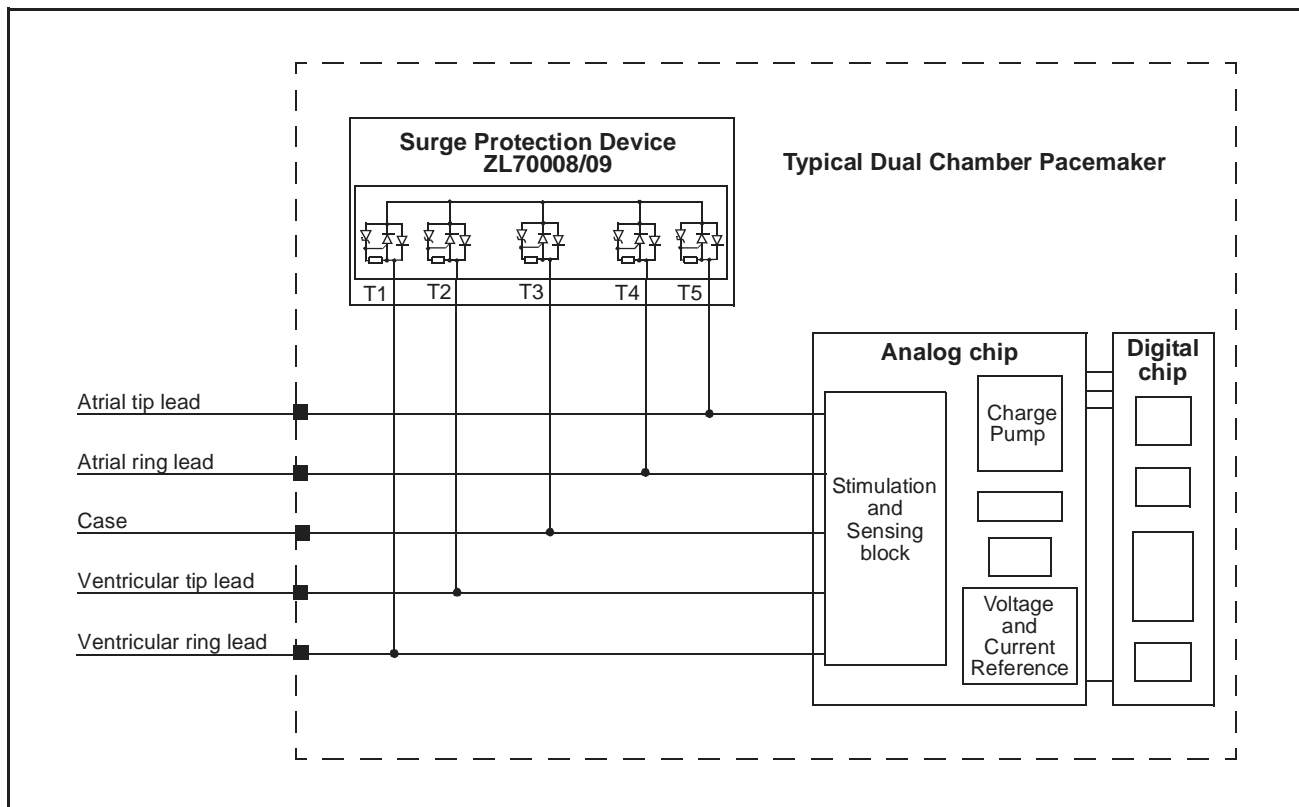
**1.3 ZL70008 and ZL70009**

ZL70008 and ZL70009 are five-branch transient surge suppressing with the same functionality as ZL70010. The only functional difference is that the substrate of the device is accessible through the two terminals SUB1 and SUB2.

## 2.0 Application

According to the EN-45502 standard, all active medical devices intended for implantation in a human torso should not be permanently affected by an external defibrillation of the patient. Compliance is confirmed if the implanted device continues to meet device specification after being subjected to a sequence of 140 Volt pulses in series with a 300 Ohm resistor between each conductive part of the device including the device case (see EN-45502 for details). Using the ZL70002/08/09/10 protects the implantable device and is an effective means of compliance with the EN-45502 standard where the electronics, in almost all cases, would be destroyed if not protected. The same compliance tests are also described in EN-50061.

In the application example shown in Figure 6, each of the dual chamber pacemaker's terminals and case are connected to a terminal on the protection device. If a defibrillation pulse causes the ventricular tip to begin to go positive, relative to the case, the ZL70008/9 thyristor structure rapidly becomes active and forms a low impedance path between T2 and T3 to absorb the current and limit the voltage. This provides an effective means of protection to the pacemaker chip. In actuality, the voltages and currents the implanted device is subjected to in an actual defibrillation can be higher than described in EN-45502/EN-50061 and has been taken into account when designing the ZL70002/08/09/10 family.



**Figure 6 - Pacemaker Application Example**

Terminals placed most remotely to others should get special attention since they effectively form a large pick-up coil and could therefore be exposed to a large amount of current. When implanted, the pacemaker case is placed beneath the collarbone and all other terminals are placed together inside the heart. For this reason, the largest current will pass through the surge protection terminal connected to the case of the pacemaker. For ZL70008/9, we recommend that the case be connected to T3 of the protection device which is designed to be able to withstand the largest amount of current. If device ZL700010 is used in a 5 terminal application, we recommend that 2 pins of the protection device be connected to the implantable device terminal with the largest current flow (typically the terminal for the device case).

2.1 Mechanical Data - ZL70010

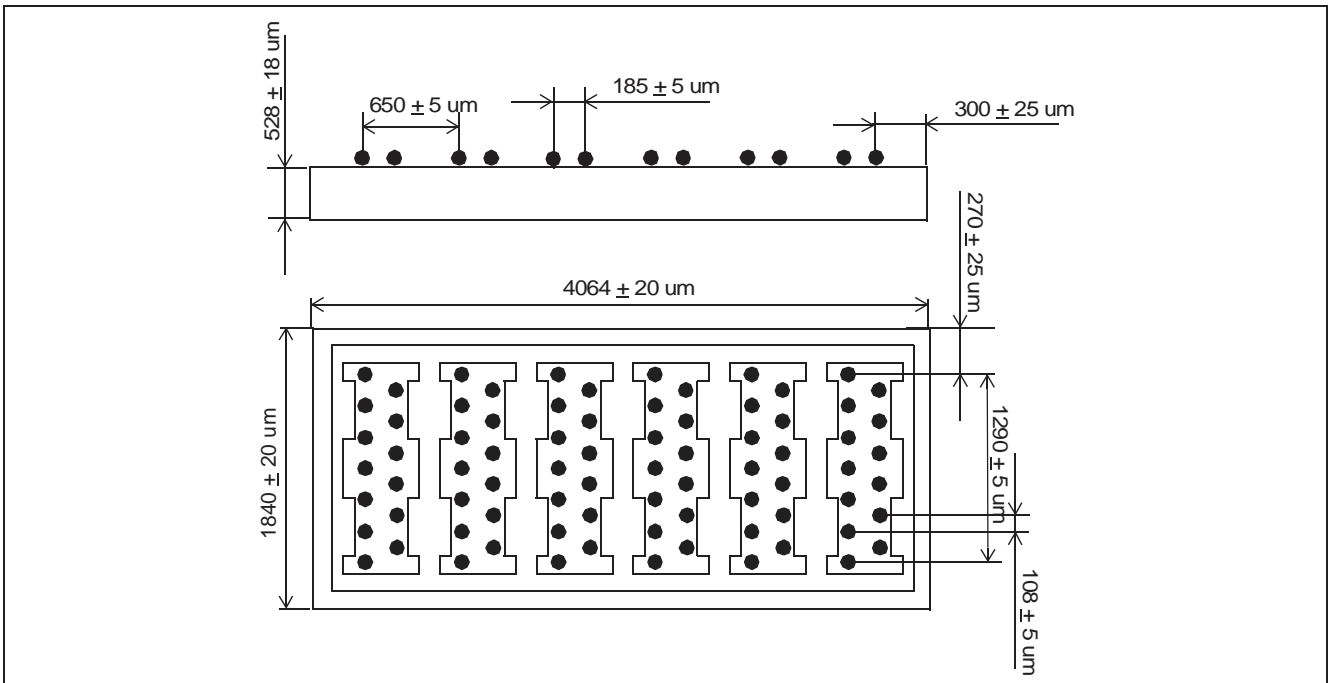


Figure 7 - Size and Bump Placement of ZL70010

2.2 Mechanical Data - ZL70002

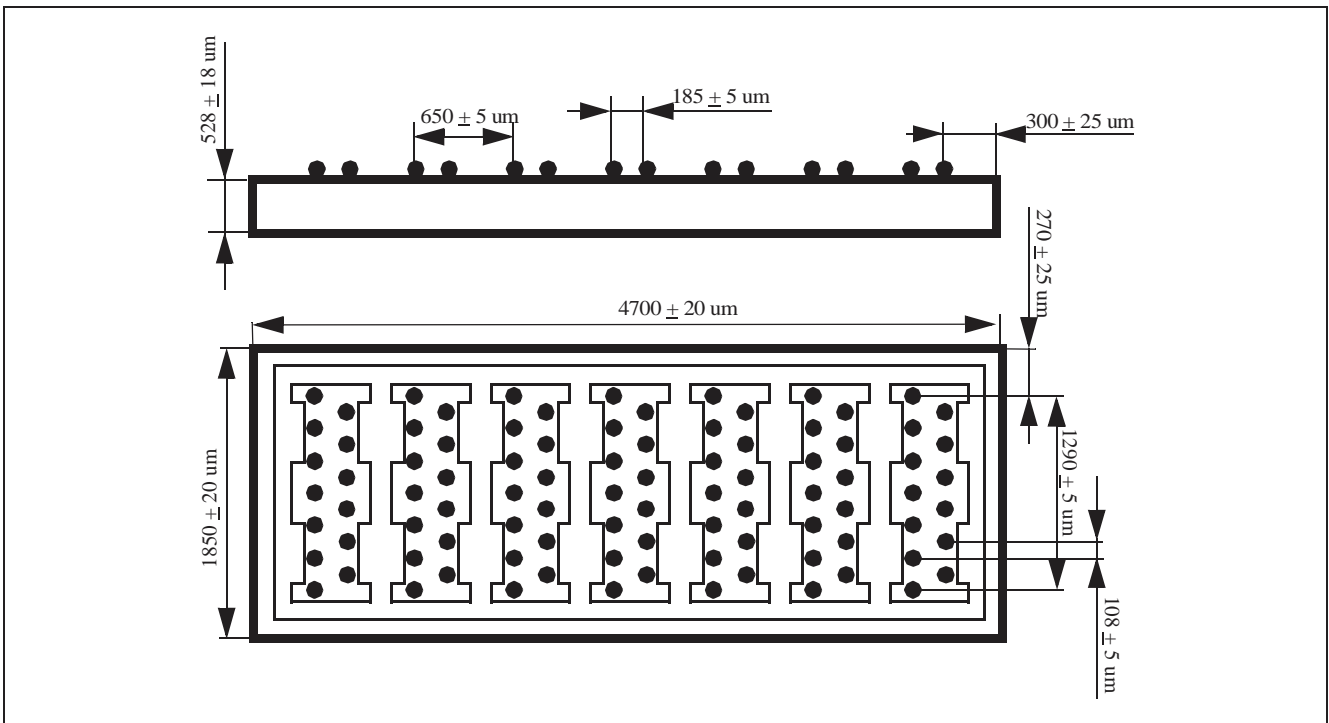


Figure 8 - Size and Bump Placement of ZL70002

2.3 Mechanical Data - ZL70008 and ZL70009

Note that the bump pattern for ZL70008 and ZL70009 differ slightly as shown in Figure 5. Figure 9 depicts ZL70008.

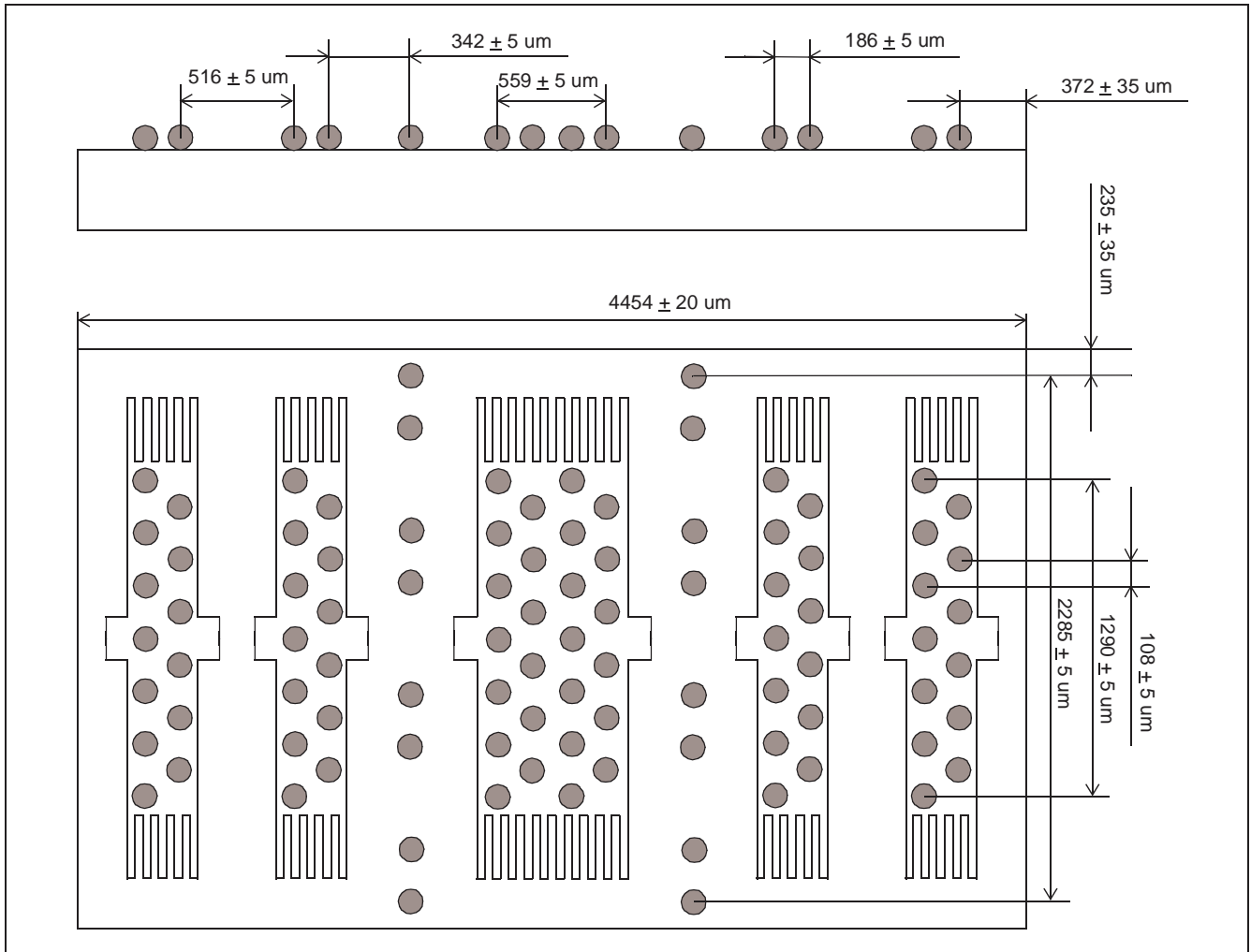


Figure 9 - Size and Bump Placement of ZL70008 and ZL70009

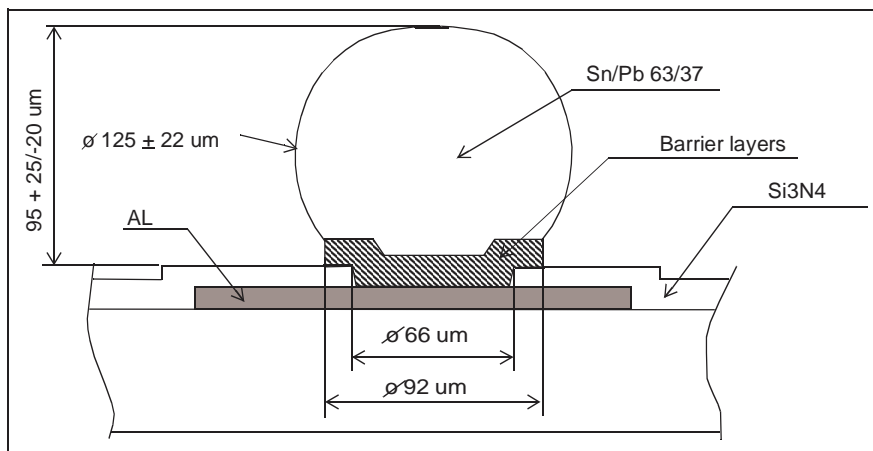


Figure 10 - Bump Appearance of ZL70002/08/09/10

**Absolute Maximum Ratings\***

	Parameter	Sym	Min	Max	Units	Test Conditions
1	Storage Temperature range	T <sub>S</sub>	-40	125	°C	
2	Maximum junction temperature	T <sub>j</sub>		125	°C	
3	Maximum surge current	ITSM		8	A	Test according to Figure 11. tp for flip mounted chips with underfill: 10 ms
4	Continuous power dissipation	Pmax		300	mW	t>1 s

\*Exceeding these values may cause permanent damage. Functional operations under these conditions is not implemented

**Recommended Operating Conditions**

	Parameter	Sym	Min	Typ <sup>1</sup>	Max	Units	Test Conditions
5	Operating temperature range	T <sub>OP</sub>	0	37	55	°C	

1) Typical figures are at 37 degrees C and are for design only.

**DC Electrical Characteristics<sup>1</sup>**

	Parameter	Sym	Min	Typ <sup>2</sup>	Max	Units	Test Conditions
6	Forward breakdown voltage, Zener diode, terminal to terminal						
	ZL70002/10	Vfz	9.0	10.1	11.0	V	Iz=10µA
	ZL70008	Vfz	9.5	10.5	13.5	V	Iz=10µA
	ZL70009	Vfz	9.0	9.5	12.2	V	Iz=10µA
7	Forward breakdown voltage, Zener diode, terminal to substrate						
	ZL70008	Vfz	9.0	10.2	12.8	V	Iz=10µA
	ZL70009	Vfz	8.5	9.2	11.5	V	Iz=10µA
8	Breakover voltage, terminal to terminal						
	ZL70002/10	Vbo	9.0	11.2	12.2	V	Figure 12
	ZL70008	Vbo	9.5	11.6	13.5	V	Figure 12
	ZL70009	Vbo	9.0	10.5	12.2	V	Figure 12
9	Breakover voltage, terminal to substrate						
	ZL70008	Vbo	9.0	11.0	12.8	V	Figure 12
	ZL70009	Vbo	8.5	9.8	11.5	V	Figure 12



	Parameter	Sym	Min	Typ <sup>2</sup>	Max	Units	Test Conditions
10	Forward diode voltage drop, substrate to terminal ZL70008/09	Vfwd			2	V	Measured @2A
11	Breakover current ZL70002/10 ZL70008 ZL70009	lbo lbo lbo		15 28 15	60 60 40	mA mA mA	Figure 12 Figure 12 Figure 12
12	Holding current ZL70002/08/09/10	lh	1			mA	Measured after a current pulse of Ip=0.2A for tp=1ms, RG<200 Ω Figure 13.
13	On-state voltage terminal to terminal ZL70002/08/09/10	Von		2.2	3.0	V	Measured with a 300 μs pulse, IT=1 A
14	On-state dynamic resistance ZL70002/08/09/10	Ron		0.4	1	Ω	Measured with a 300 μs pulse, dIT=1-2 A
15	On-state voltage terminal to substrate ZL70008/09	Von		1.0	3.0	V	Measured with a 300 μs pulse, IT=1 A
16	Off-state current terminal to terminal ZL70002/08/09/10	Id		10	100	nA	Measured at 8.5 V (ZL70002/09/10) and at 9.0 V (ZL70008)
17	Off-state current terminal to substrate ZL70008/09	Id		10	100	nA	Measured at 8.5 V (ZL70008) and at 8.0 V (ZL70009)
18	Parasitic capacitance ZL70002/10	Cp			50	pF	
19	Parasitic capacitance ZL70008/09	Cp			200	pF	

1) Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

2) Typical figures are at 37 degrees C and are for design only

AC Electrical Characteristics<sup>1</sup>

	Parameter	Sym	Min	Typ <sup>2</sup>	Max	Units	Test Conditions
20	Turn-on delay ZL70002/10	t <sub>ond</sub>		500	700	ns	Measured at 8.0 V (ZL70002/09/10) and at 8.5 V (ZL70008) and defined according to Figure 14.
	ZL70008	t <sub>ond</sub>		140	200	ns	
	ZL70009	t <sub>ond</sub>		60	100	ns	
21	Maximum voltage during surge ZL70002/08/10	V <sub>peak</sub>		13	15	V	Measured at peak and defined according to Figure 14.
	ZL70009	V <sub>peak</sub>		11	13	V	Measured at peak and defined according to Figure 14.

1) Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.  
 2) Typical figures are at 37 degrees C and are for design only.

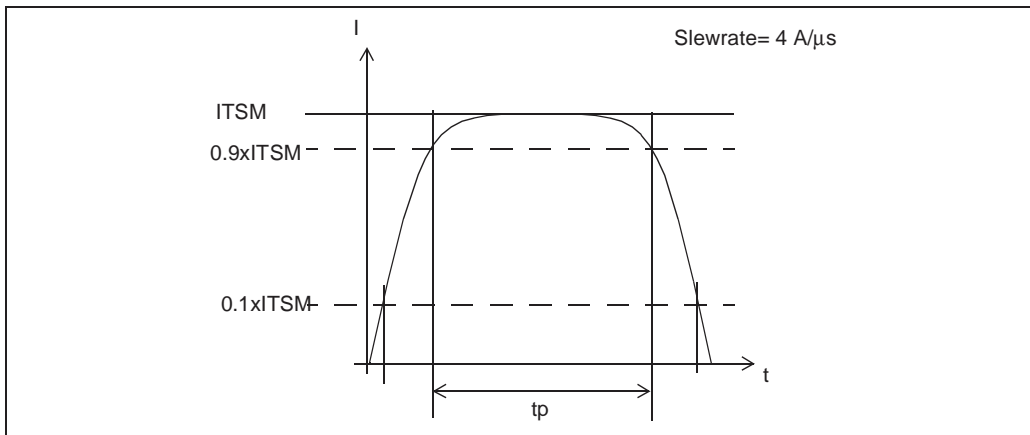


Figure 11 - 10 ms Surge Current Waveform

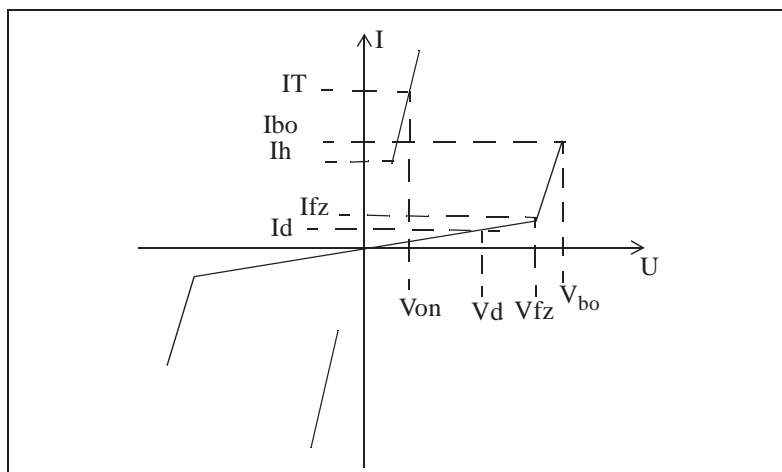


Figure 12 - Terminal to Terminal Characteristic

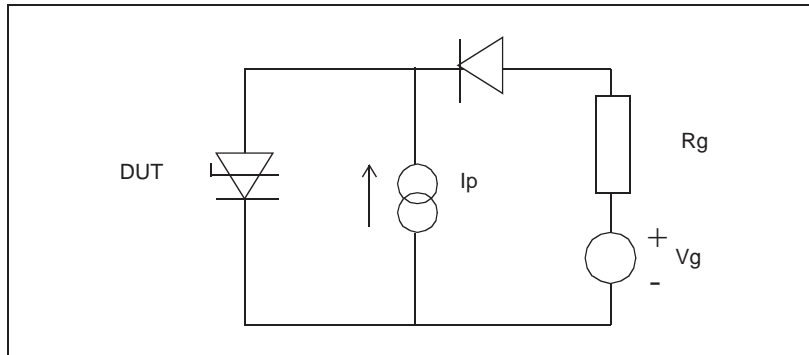


Figure 13 - Holding Current Circuit

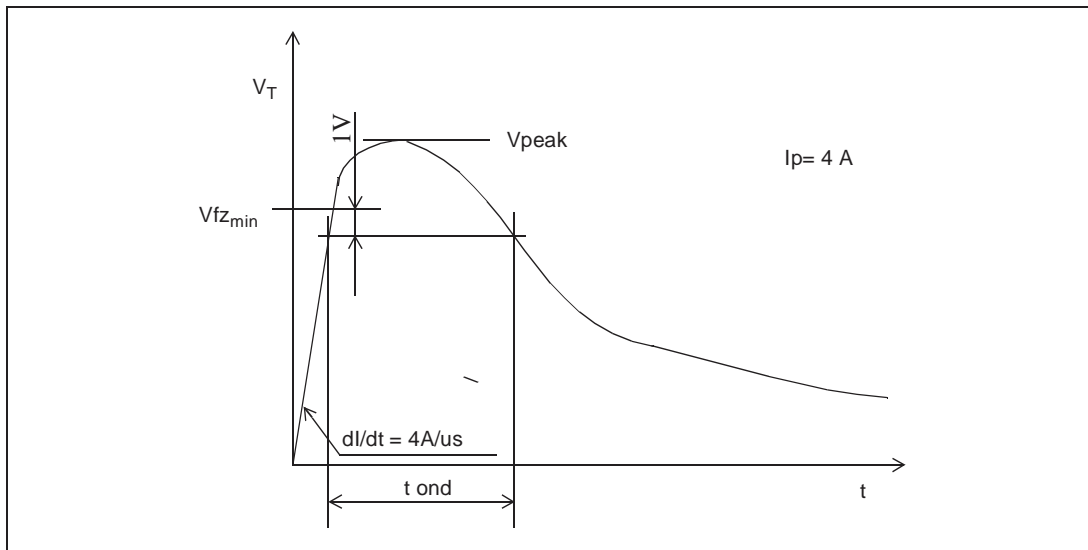


Figure 14 - Turn-on Delay Definition



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