ZL40518

3 Channel Laser Diode Driver

Data Sheet

February 2005

Features

- Current-controlled Output Current source
- Output Current per Channel to 250 mA
- Total Output Current to 300 mA
- Rise Time 1.0 ns, Fall Time 1.1 ns
- On-chip RF Oscillator
- External Resistor Control of Oscillator Swing and Frequency
- 200 to 500 MHz Oscillator Range
- 100 mA Maximum Oscillator Swing
- Single +5 V Power Supply (±10%)
- Low-power Consumption
- Common Enable, Disable Input
- TTL/CMOS control signals
- Small SS016 Package

Ordering Information

ZL40518DGE1 16 Pin QSOP* Tubes

*Pb Free Matte Tin

0°C to +70°C

Applications

- DVD R/RW
- CD R/RW

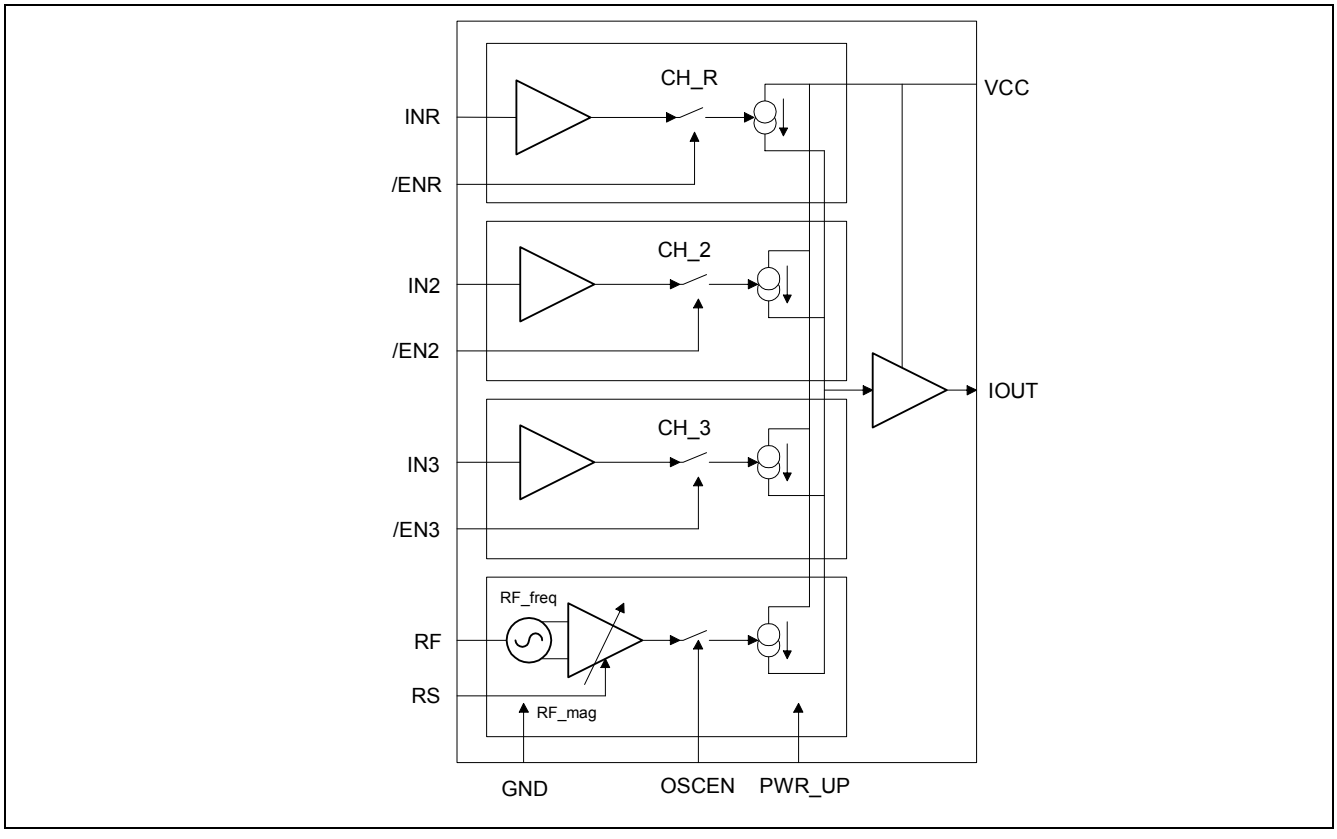


Figure 1 - Functional Block Diagram

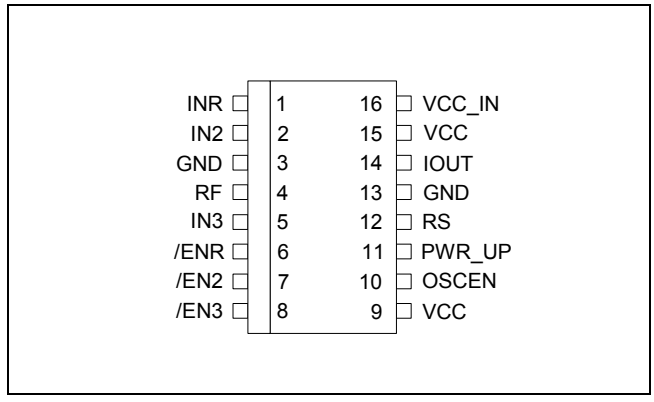


Figure 2 - Pinout of 16 Pin SSO16 Package (Top View)

Description

The ZL40518 is a laser diode driver for high speed operation of a grounded laser diode. The driver consists of 3 controllable channels: a switchable, low noise, read channel and two switchable write channels. Write current pulses are enabled with the application of a low signal on the /EN pins. A summed output of all channels is available at the IOUT pin. Each channel can contribute up to 250 mA to the total output current of up to 300 mA. A total read channel gain of 100 and write channels 2 and 3 with a gain of 250 and 150 respectively are provided between each reference current input and output.

Laser mode hopping noise during read mode can be reduced by the use of an on-chip RF oscillator. The oscillator frequency and swing can be set by two external resistors. The oscillator is enabled by a high signal on the OSCEN pin and the entire device can be switched off by the application of a low signal on the PWR_UP pin.

Application Notes

Read and Write Channel Operation

The read channel is activated by applying a 'High' signal to the PWR_UP pin and applying a 'low' signal to /ENR. In this mode, the fast write channels can be enabled by applying a 'Low signal to the respective pair of write enable pins (/EN2) or (/EN3). The output currents of the three channels are summed together and output as a composite signal at IOUT.

Voltage control of the channel reference inputs (INR, IN2 and IN3) can be achieved quite easily using an external resistor R_{ref} in series with the reference channel input to convert a given reference potential V_{ref} to an input current, I_{in}:

$$I_{in} = \frac{V_{ref}}{R_{ref} + R_{in}} ,$$

where R_{in} is the input impedance of the respective reference channel.

On-Chip RF Oscillator

An on-chip RF oscillator is enabled if OSCEN = 'High', and its output signal is added to the current output.The oscillator amplitude is set by an external resistor from RS to GND. Its frequency is set by an external resistor RF to GND. The oscillator signal is summed with the programmed Write and Read levels before amplification to the output. The oscillator signal has zero DC level and +I_pk to -I_pk signal swing. Consequently, if the programmed DC level from the Write and Read Channels is less than the PK level programmed for the Oscillator, the combined

signal will be clipped on the negative cycle of the signal. This will increase the harmonic content of the output signal and reduce the pk to pk amplitude output.

Thermal Considerations

Package thermal resistance is 40° C/W under the EIA/JESD51-3 compliant PCB test board condition. Users should ensure that the junction temperature does not exceed 150°C. Thermal resistance from junction to case and to ambient is very much dependent on how the IC is mounted onto the board, on the PCB layout and on any heat extraction arrangements. Power consumption and system ambient operating temperature limits should be noted and careful thermal gradient calculations undertaken to ensure that the junction temperature never exceeds 150°C.

Electrical and Optical Pulse Response

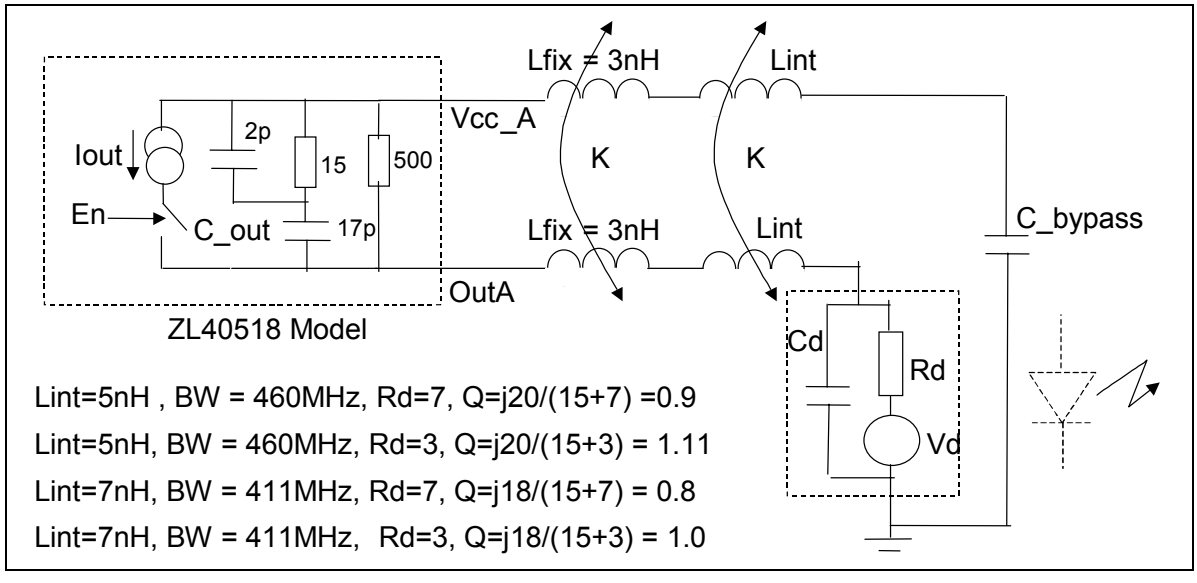


Figure 3 - Pulse Response Model

Figure 3 illustrates a simplified model of the typical ZL40518 and the application. The ZL40518 consist of an ideal switched current source and an equivalent model of the ZL40518 output stage. The Electrical Model for the Laser Diode is a Voltage source Vd (V_on) in series with the On Resistance Rd all in parallel with the Junction Capacitance Cd. This simplified model approximately represents the Laser Diode Electrical load when operated beyond the Laser Threshold. To a first approximation, the Optical output is proportional to the current flow in the Resistor Rd.

The Laser Diode and the ZL40518 are connected together by interconnect tracks with the return current passing through the supply decoupling bypass capacitor between ground and output Vcc. The ZL40518 will typically switch the programmed output current in 400 ps and can be approximated to an ideal switch with a propagation delay of Iout_on (1.2 nS). The electrical pulse response parameters, Trise, Tfall, Overshoot and Undershoot are determined by the combined electrical network as illustrated in Figure 3.

For example, the Rise Time and Fall time for large current steps can be slew rate limited by the combined interconnect and fixed interconnect inductance. The Fixed Inductance represents that associated with packaging and minimum interconnect distance . The Interconnect Inductance is that associated with the additional tracking between Laser Diode and the ZL40518 to accommodate application physical limitations.

For example, if a pulse of 260 mA amplitude (40 mA to 300 mA) is to be switched in a time of 1 ns with the Vd = 1.6 V, then the maximum volt drop across the interconnect inductance is approximately 3.5 V (maximum Vpin for 300 mA output) - 1.6 V (Vdiode) = 1.9 V. Consequently, L*di/dt < 1.9 V. Hence , L < 1.9/ (0.26A/1ns)

= 7.3 nH.

Small current step size Rise and Fall time will be determined by the Bandwidth of the combined network. This is dominated by the Interconnect Inductance and the output Capacitance. Similarly, the overshoot and undershoot will be determined by the Q of the network. This is a function of the Source Impedance from the ZL40518, the Interconnect inductance and the Load impedance of the Laser Diode. Figure 3 includes example simplified estimates of the Q and BW of the combined Laser Diode, ZL40518 and interconnect network for two different interconnect inductance values (5 nH & 7 nH) and two different Diode On resistance (3 Ohm & 7 Ohm) . This simple analysis illustrates the change in BW and Q of the network depending on these parameters. This in Turn effects the Rise Time and Fall time and the Overshoot and Undershoot performance achieved in the application.

Specified Electrical Performance with 15 mm Interconnect and Zarlink ZLE40518 Evaluation Board

The specified performance in the table are results based on the electrical measurements and simulations across full process corners using the Zarlink Evaluation Board using a 6.8 Ohm resistive load to ground. The track interconnect between ZL40518 and the 6.8 Ohm Resistor is 15 mm long and uses a 2 mm wide track on single sided FR4 board. The return path is via two 2 mm wide tracks spaced 0.25 mm either side of the track between output and the 6.8 ohm resistor. The combined forward and return path forms a co planar transmission line with a characteristic impedance of approximately 120 ohms. The tight coupled return paths carrying the return current reduce the effective series inductance (Leff) which can be approximated to:-

$$L_{eff} = 2 * Lint * (1 - K) + 2 * Lfix * (1 - K).$$

The ZLE40518 board has two positions for the Laser Diode at two different distances. (15 and 30 mm).

The measured value of L_{eff} is 7 nH.

The estimated value of $L_{eff} = 2 * 8 (1 - 0.5) = 8$ nH.

The actual pulse response achieved in an application is thus dependent on the application.

Application Layer Guide Lines

Minimize Interconnect Inductance by:-

a. Using Short Interconnect Distance

b. Use wide interconnect tracks

c. Keep the return path tightly coupled to the forward path

ZLE40518 Interconnect

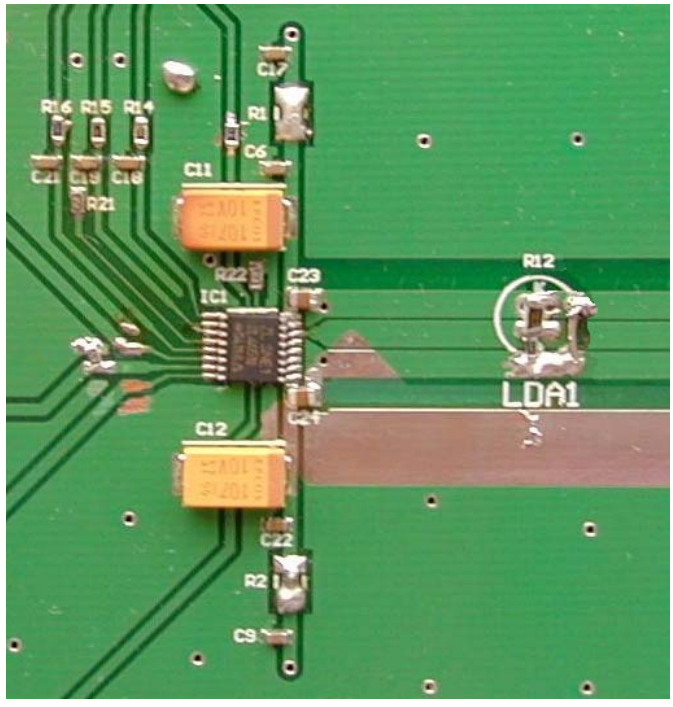


Figure 4 - ZLE40518 Application Board Electrical Interconnect

Application Diagram

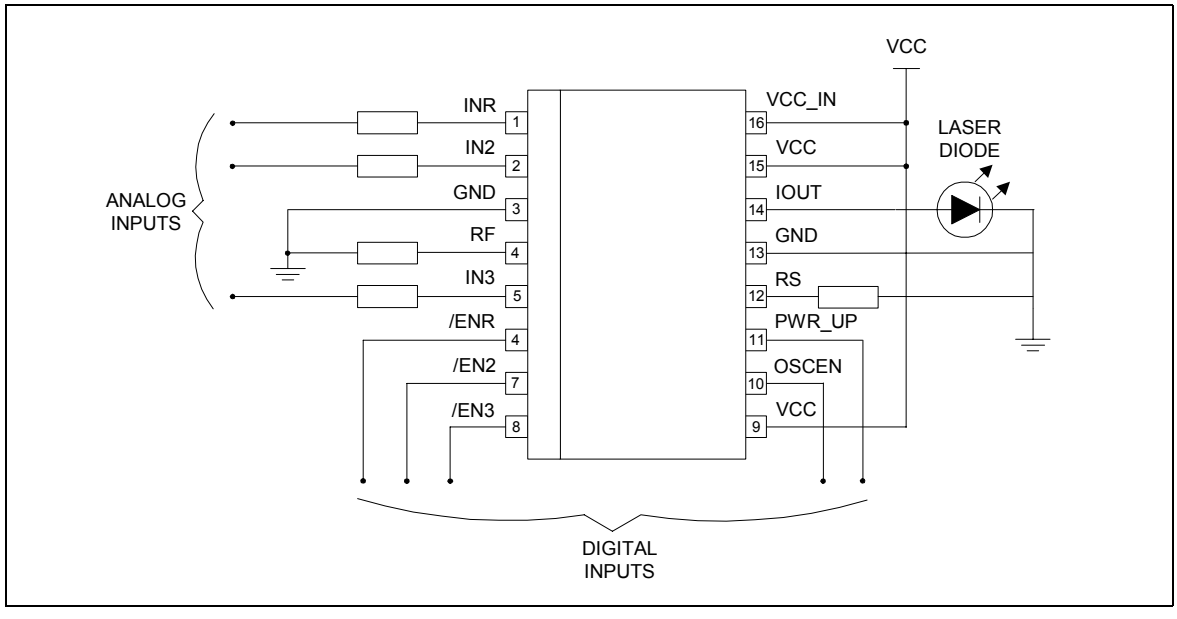


Figure 5 - Evaluation Board Circuit

Pin List

Pin No.	Pin name	Type	Function
1	INR	Analog	Read Channel Input Current
2	IN2	Analog	Channel 2 Input Current
3	GND	Supply	Ground
4	RF	Analog	External Resistor to ground to set Oscillator Frequency
5	IN3	Analog	Channel 3 Input Current
6	/ENR	Digital	Digital control of Read Channel (active low)
7	/EN2	Digital	Digital control of Channel 2 (active low)
8	/EN3	Digital	Digital control of Channel 3 (active low)
9	VCC	Supply	+5 V supply
10	OSCEN	Digital	Enables RF oscillator (active high)
11	PWR_UP	Digital	Device Power Up (active high)
12	RS	Analog	External Resistor to ground to set Oscillator Amplitude
13	GND	Supply	Ground
14	IOUT	Analog	Output current for laser diode
15	VCC	Supply	+5 V supply
16	VCC_IN	Supply	+5 V supply

Absolute Maximum Ratings

Permanent damage may occur to any device stressed beyond the “Absolute Maximum Ratings”. Operation at or beyond this stress rating is not implied for this or following sections of this specification. Device reliability can be affected by prolonged exposure to absolute maximum ratings.

Parameters	Symbol	Value	Unit
Supply voltage	V_{cc}	-0.5 to +6.0	V
Input voltage at INR, IN2, IN3	V_{IN1}	-0.5 to +2.0	V
Input voltage at PWR_UP, /ENR, /EN2, /EN3, OSCEN	V_{IN2}	-0.5 to V_{cc} + 0.5	V
Output voltage	V_{OUT}	-0.5 to V_{cc} - 1	V
Power dissipation	P_{Max}	0.7[1] to 1[2]	W
Junction temperature	T_J	150	C
Storage temperature range	T_{Stg}	-65 to +125	C

Note 1: $R_{thJA} \leq 115°C/W$, T_{amb} = 70 C

Note 2: $R_{thJA} \leq 115°C/W$, T_{amb} = 25°C

Operating Range

Characteristic	Symbol	Units	Unit
Supply voltage range	V_{cc}	4.5 to 5.5	V
Input current	I_{INR} I_{IN2} I_{IN3}	<2.5 <1.0 <1.7	mA
External resistor to GND to set oscillator frequency	RF	>3	kΩ
External resistor to GND to set oscillator swing	RS	>2	kΩ
Operating temperature range	T_{amb}	0 to +70	C

Package Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	115[1]	K/W

Note 1: Measured with a multilayer test board (JEDEC standard).

Electrical Characteristics - Vcc = 5 V, T_{amb} = 25°C, PWR_UP = High, Ch2 and Ch3 disabled (/EN2 = /EN3 = high), Read enabled (/ENR = low), OSCEN = Low, unless otherwise specified.

Parameters	Test Conditions	Pin.	Symbol	Min.	Typ.	Max.	Unit	Type*
Power Supply								
Supply current, power down	PWR_UP = Low, /EN2 = /EN3 = Low	9, 15, 16	ICC_{PD2}		0.4		mA	A
Supply current, read mode, oscillator disabled	I_{INR} =500 μA, I_{IN2} = 200 μA, I_{IN3} = 333 μA	9, 15, 16	ICC_{R1}		86		mA	A
Supply current, read mode, oscillator enabled	I_{INR} =500 μA, I_{IN2} = 200 μA, I_{IN3} = 333 μA, OSCEN = High, RS = 7.5 kΩ, RF = 7.5 kΩ	9, 15, 16	ICC_{R2}		90		mA	A
Supply current, write mode	I_{INR} =500 μA, I_{IN2} = 200 μA, I_{IN3} = 333 μA, /EN2 = /EN3 = Low	9, 15, 16	ICC_{W}		180		mA	A
Supply current, input off	I_{INR} = I_{IN2} = I_{IN3} = 0 μA	9, 15, 16	ICC_{off}		15		mA	A
Digital Inputs								
/ENR, /EN2, /EN3 low voltage		6, 7, 8	VNE_{LO}			1.2	V	A
/ENR, /EN2, /EN3 high voltage		6, 7, 8	VNE_{HI}	1.9			V	A
PWR_UP Low Voltage		11	VEN_{LO}			0.5	V	A
PWR_UP High Voltage		11	VEN_{HI}	2.7			V	A
OSCEN low voltage		10	VEO_{LO}			0.5	V	A
OSCEN high voltage		10	VEO_{HI}	3.0			V	A
Current at Digital Inputs								
/ENR, /EN2, /EN3 low current	/EN = 0 V	6, 7, 8	INE_{LO}	-300			μA	C
/ENR, /EN2, /EN3 high current	/EN = 5 V	6, 7, 8	INE_{HI}			800	μA	C
PWR_UP Low Current	PWR_UP = 0 V	11	IEN_{LO}	-150			μA	C
PWR_UP High Current	PWR_UP = 5 V	11	IEN_{HI}			100	μA	C
OSCEN low current	OSCEN = 0 V	10	IEO_{LO}	-100			μA	C
OSCEN high current	OSCEN = 5 V	10	IEO_{HI}			800	μA	C

* A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics - Vcc = 5 V, Tamb = 25°C, PWR_UP = High, unless otherwise specified.

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Output IOUT								
Total output current	Output is sourcing	14	I_{OUT}		350		mA	A
Output current per channel	Output is sourcing	14	I_{OUTR}	250			mA	A
I_{OUT} series resistance	Total R_{OUT} to V_{CC} rail	14	R_{OUT}		2		Ω	C
Best fit current gain INR	Channel R[1]	14	GAINR	90	100	130	mA/ mA	A
Best fit current gain IN2	Channel 2[1]	14	GAIN2	225	250	325	mA/ mA	A
Best fit current gain IN3	Channel 3[1]	14	GAIN3	135	150	195	mA/ mA	A
Best fit current offset	Any channel [1]	14	IOS		2.6		mA	A
Output current linearity	Any channel [1]	14	ILIN	-3		+3	%	A
I_{IN} input impedance	$R_{IN,INR}$ is to GND	1	$R_{IN,INR}$		500		Ω	C
I_{IN} input impedance	$R_{IN,IN2}$ is to GND	2	$R_{IN,IN2}$		1250		Ω	C
I_{IN} input impedance	$R_{IN,IN3}$ is to GND	5	$R_{IN,IN3}$		750		Ω	C
EN threshold	Temperature stabilised	6, 7, 8	VTH		1.6		V	C
Output off current 1	PWR_UP = Low	14	$IOFF_1$			1	mA	C
Output off current 2	/EN2 = /EN3 = High, I_{INR} = 0, I_{IN2} = 200 μA, I_{IN3} = 333 μA	14	$IOFF_2$			1	mA	C
Output off current 3	/EN2 = /EN3 = Low, I_{INR} = I_{IN2} = I_{IN3} = 0 μA	14	$IOFF_3$			5	mA	C
I_{OUT} supply sensitivity, write mode	IOUT = 80 mA, 40 mA read + 40 mA write, VCC = 5 V +/- 10%	14	VSE_W		6		%/V	C
I_{OUT} current output noise	IOUT = 40 mA, OSCEN = Low	14	INO_O		3		nA/rt-Hz	C

*A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note 1: Linearity of the amplifier is calculated using a best fit method at three operating points of I_{OUT} at 20 mA, 40 mA, and 60 mA. $I_{OUT} = (I_{IN} \times GAIN) + I_{OS}$

Electrical Characteristics: AC Performance - Vcc = 5 V, Iout = 40 mA DC with 40 mA pulse, Tamb = 25°C, unless otherwise specified.

Parameters	Test Conditions	Pin.	Symbol	Min.	Typ.	Max.	Unit	Type*
Output AC Performance								
Write rise time	I_{OUT} = 40 mA (read) + 40 mA (10 to 90%)[1]	14	t_{RISE}		1.0		ns	C
Write fall time	I_{OUT} = 40 mA (read) + 40 mA (10 to 90%)[1]	14	t_{FALL}		1.1		ns	C
Output current overshoot	I_{OUT} = 40 mA (read) + 40 mA[1]	14	OS		5		%	C
I_{OUT} ON propagation delay	/EN 50% High-Low to I_{OUT} at 50% of final value	14	t_{ON}		2.2		ns	C
I_{OUT} OFF propagation delay	/EN 50% Low-High to I_{OUT} at 50% of final value	14	t_{OFF}		2.0		ns	C
Disable time	PWR_UP 50% High-Low to Iout at 50% of final value	14	t_{DIS}		20		ns	C
Enable time	PWR_UP 50% Low-High to Iout at 50% of final value	14	t_{EN}		23		ns	C
Amplifier bandwidth	I_{OUT} = 50 mA, all channels, -3 dB value	14	BW_{LCA}		28		MHz	C
Oscillator								
Oscillator frequency	RF = 7.5 kΩ	14	F_{OSC}	288	322	352	MHz	A
Osc. Temperature coefficient	RF = 7.5 kΩ	14	TC_{OSC}		+150		ppm/C	C
Disable time oscillator	OSCEN 50% High-Low to I_{OUT} at 50% of final value	14	T_{DISO}		4		ns	C
Enable time oscillator	OSCEN 50% Low-High to I_{OUT} at 50% of final value	14	T_{ENO}		2		ns	C

* A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note 1: Load resistor at I_{OUT} 6.8 ohms, measurement with 50 ohm oscilloscope and 39 ohm series resistor.

Characteristic Curves

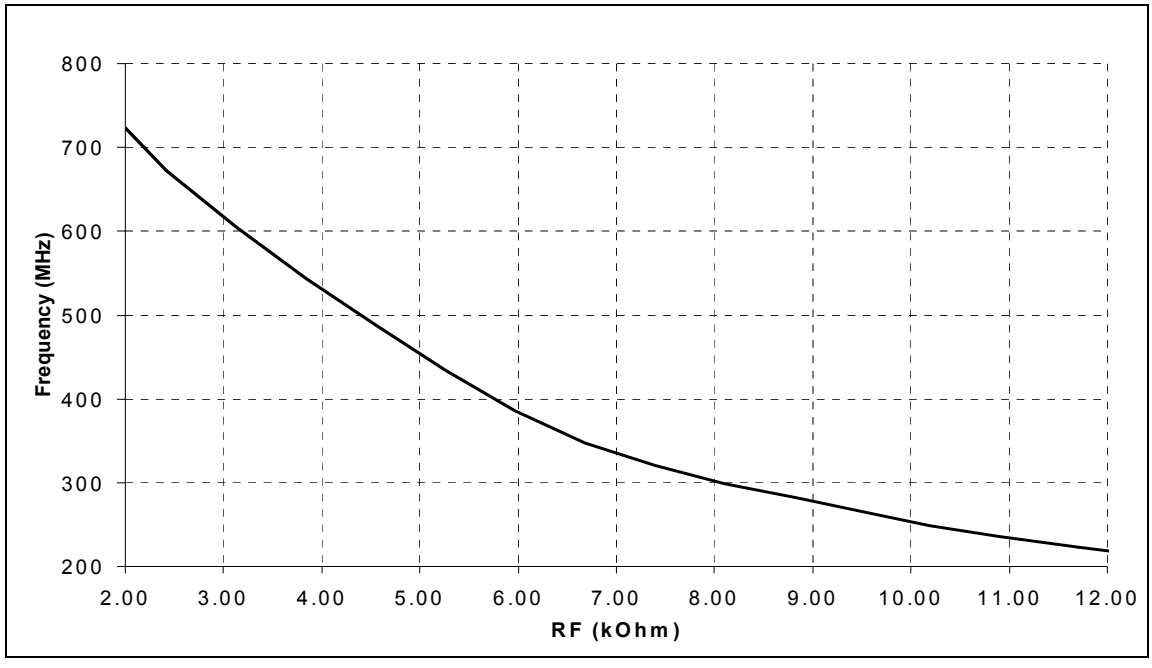


Figure 6 - Oscillator Frequency vs RF (RS=7.5 kΩ)

Vcc = 5 V, Temp = 25°C

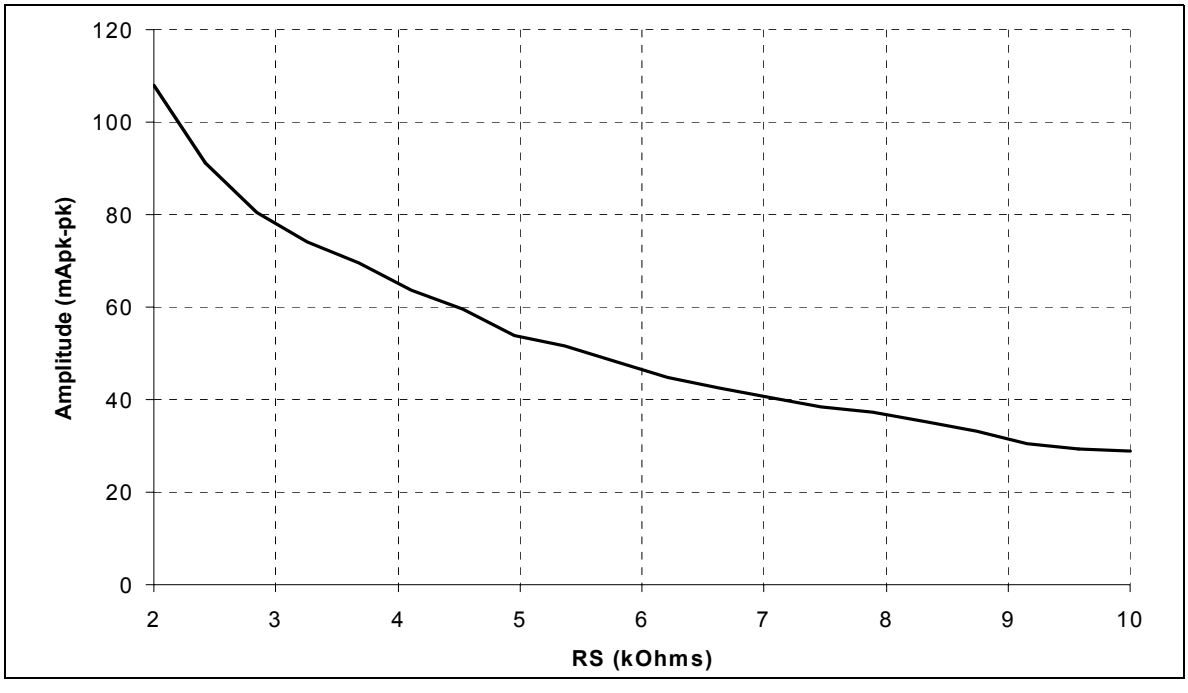


Figure 7 - Oscillator Swing vs RS (RF=7.5 Ω)

Vcc = 5 V, Temp = 25°C

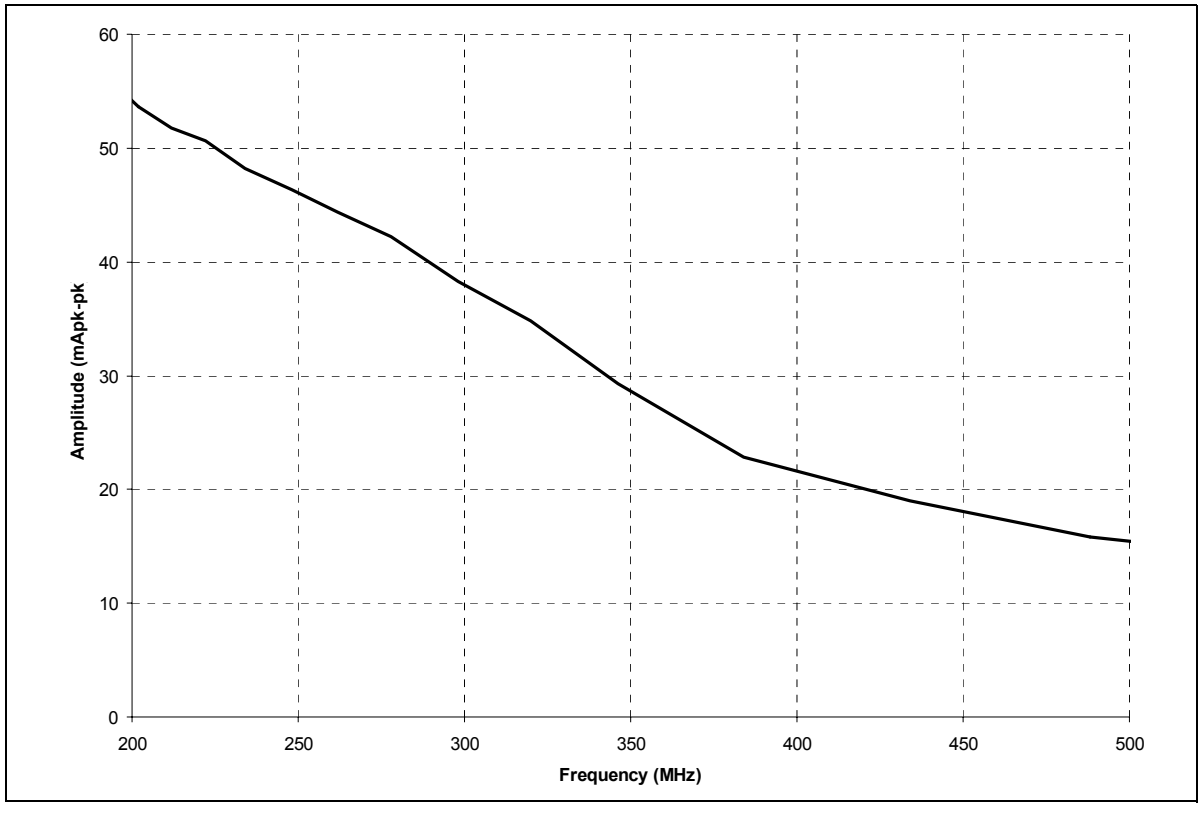


Figure 8 - Oscillator Frequency Dependency of Swing

Vcc = 5 V, Temp = 25°C

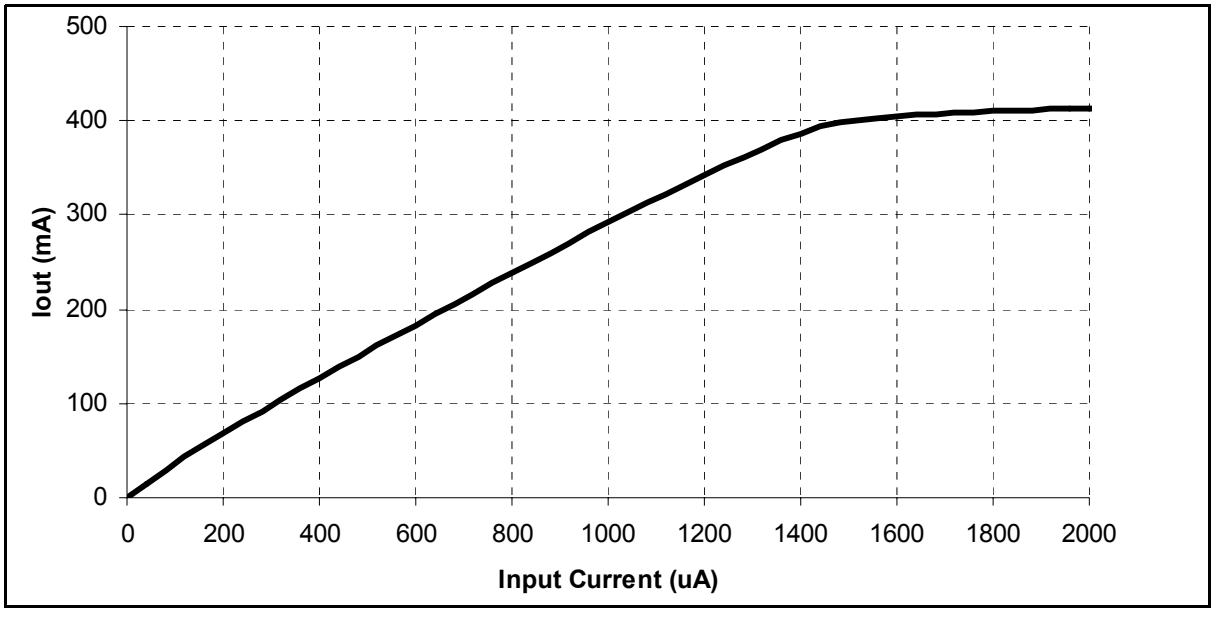


Figure 9 - Transfer Characteristic of Channel 2

(Gain = 278, Load Resistor at IOUT = 6.8 Ω)

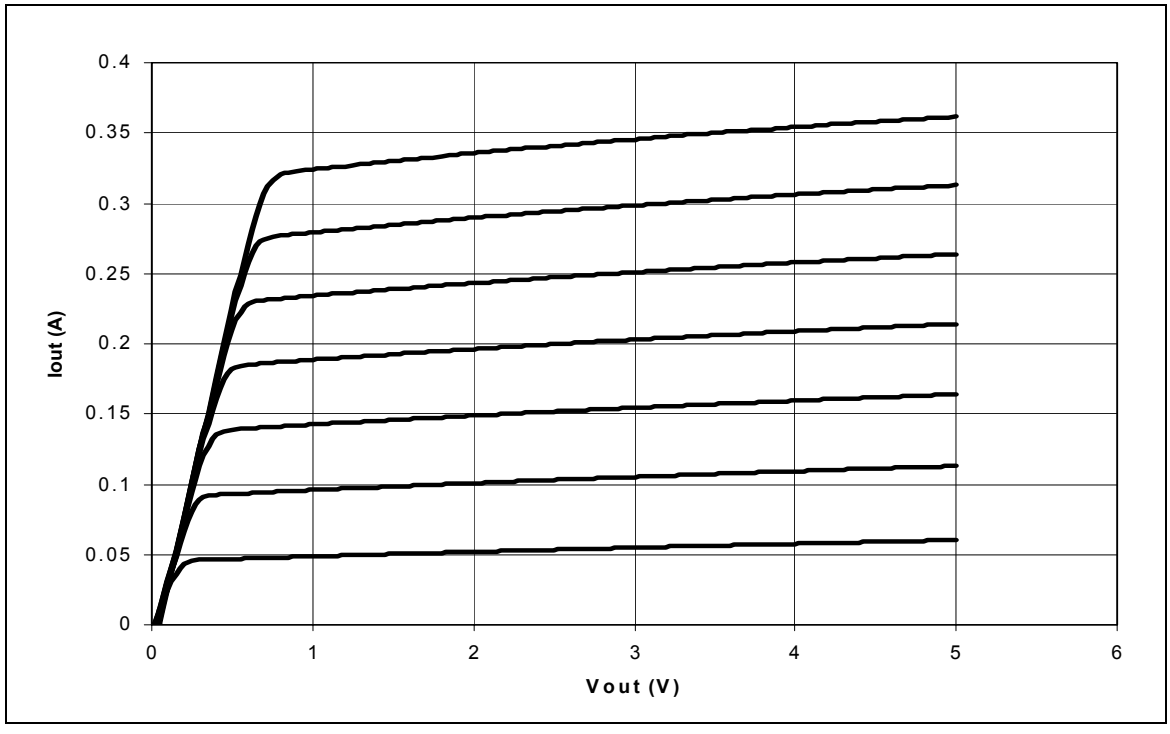


Figure 10 - Voltage Compliance R (IOUT to VCC) = 2.0 Ω

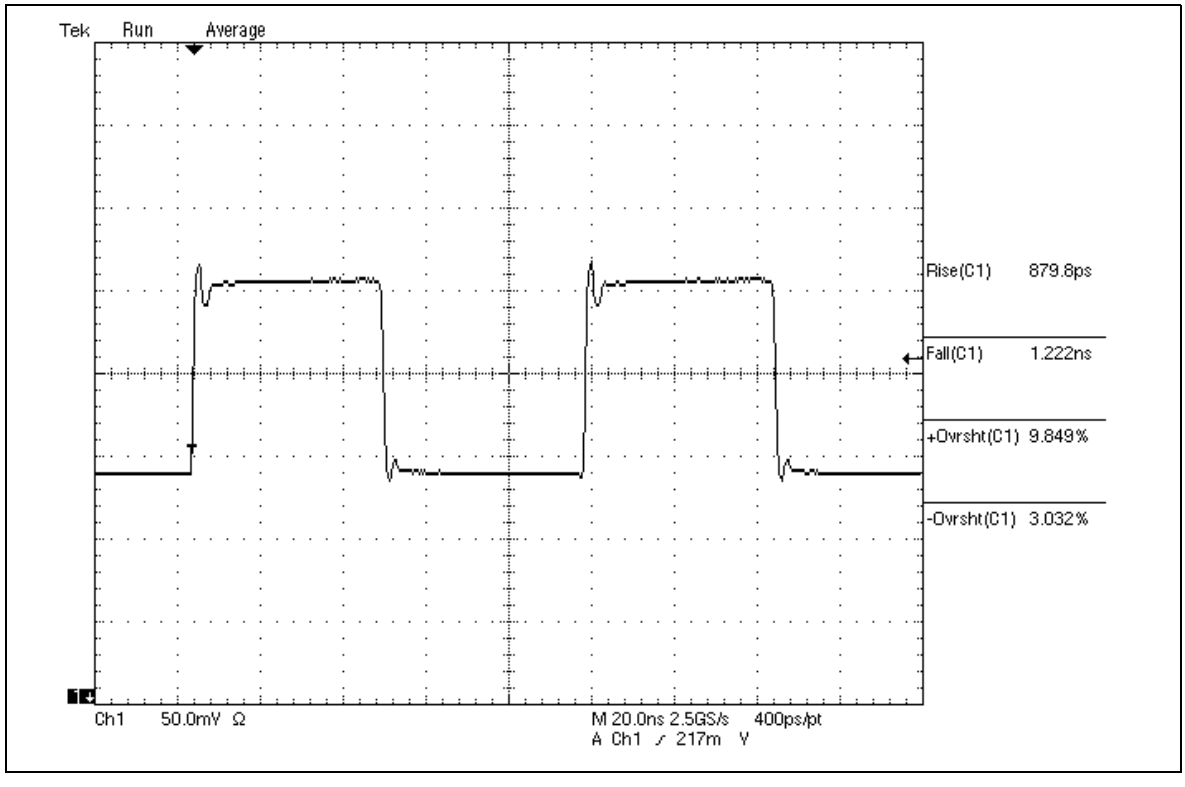


Figure 11 - Step Response, Read Channel: 50 mA, Channel 2: 50mApp

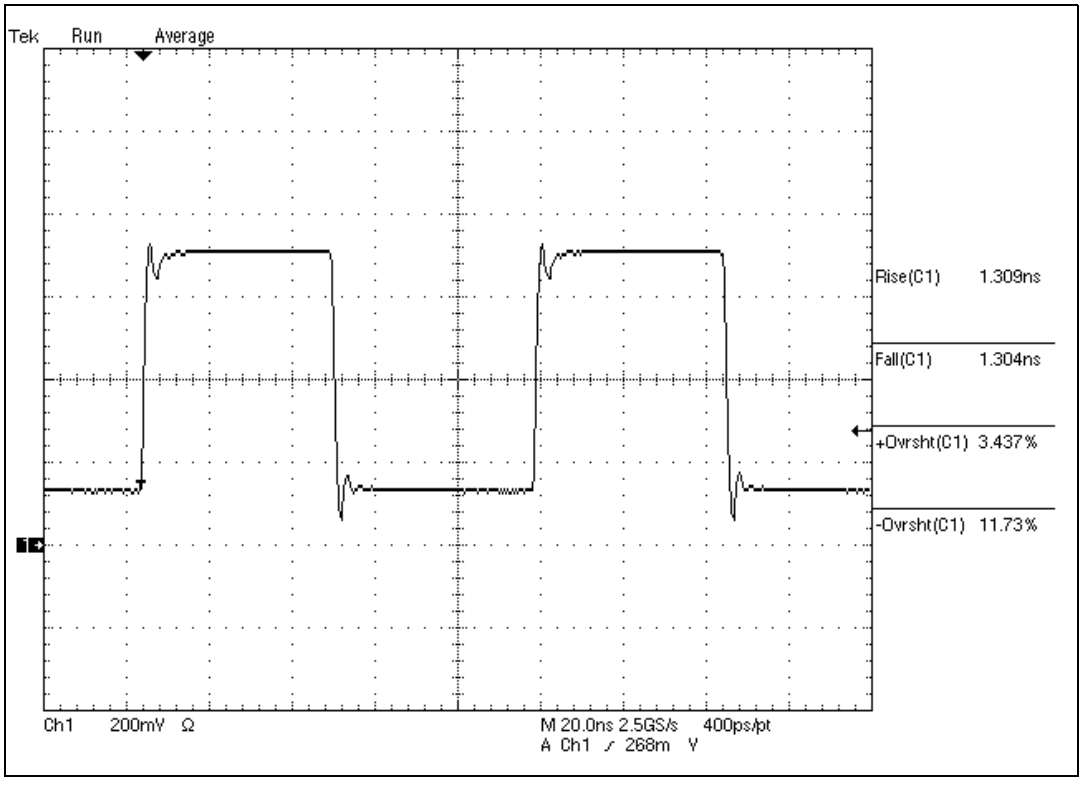


Figure 12 - Step Response, Read Channel: 50 mA, Channel 2: 250mApp

Timing Waveforms

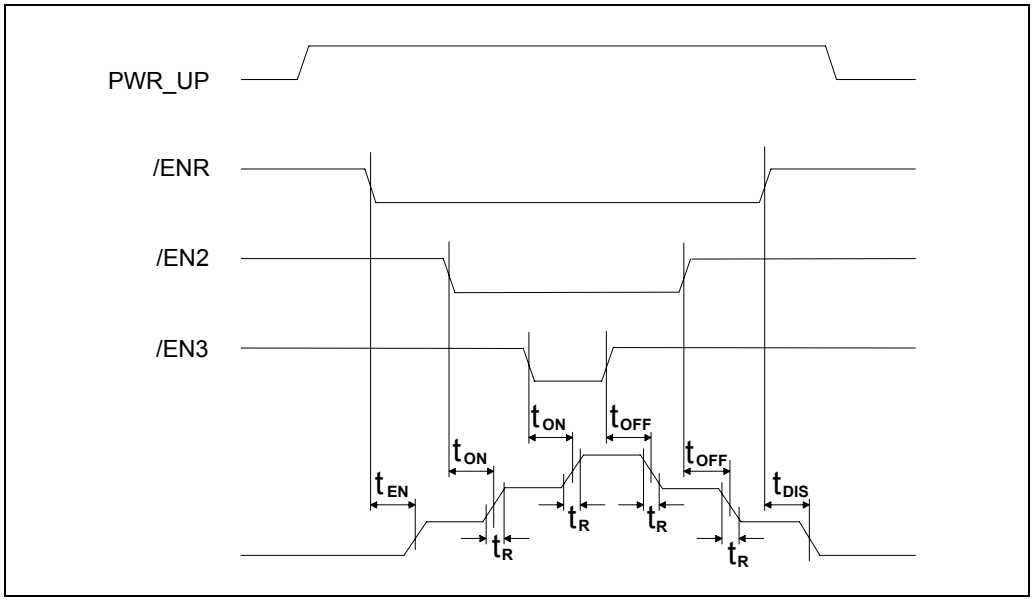
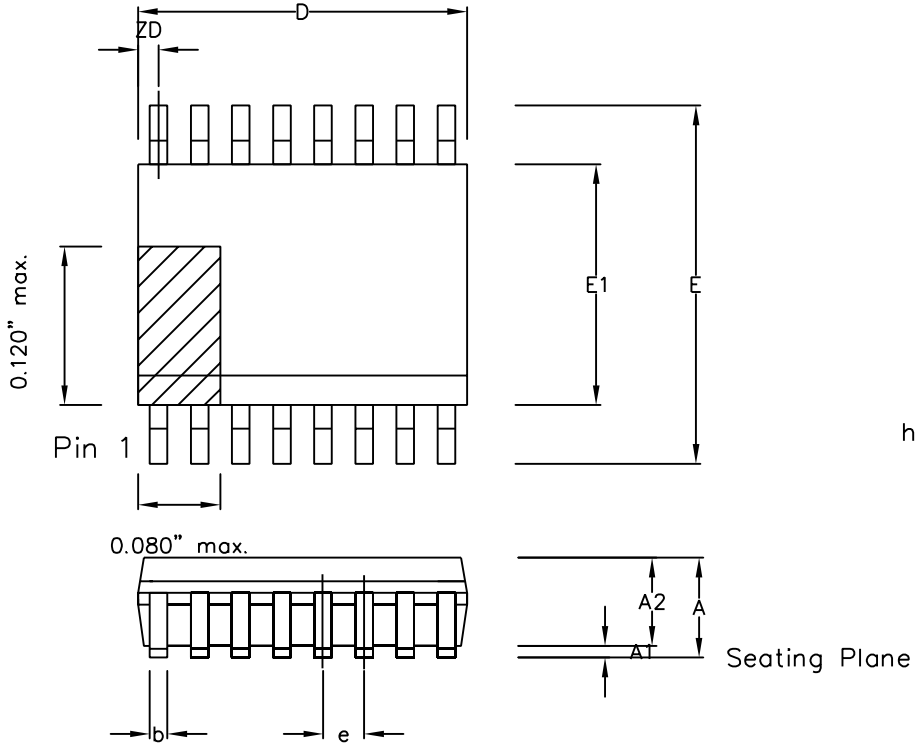
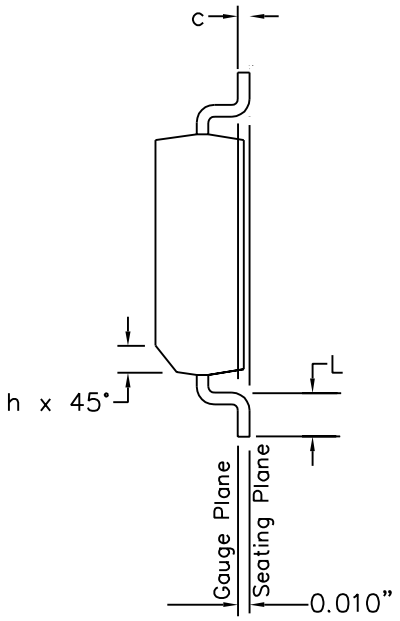


Figure 13 - Output Waveform Showing Addition of Read and Write Levels





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.189	0.197	4.80	5.00
ZD	0.009 REF.		0.23 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	16			
Conforms to JEDEC MO-137AB Iss. A				

This drawing supersedes
418/ED/51617/001 (Swindon/Plymouth)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	201928	207313	212474	
DATE	27Feb97	24Aug99	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
QP / Q

Package Code DG

Package Outline for 16 lead QSOP (0.150" Body Width)

GPD00290

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