Triple-Channel Synchronous-Rectified Buck MOSFET Driver

General Description

The RT9605A is a high frequency, triple-channel synchronous-rectified buck MOSFET driver specifically designed to drive six power N-MOSFETs. The part is promoted to pair with RichTek's multiphase buck PWM controller family for high-density power supply implementation. The output drivers of RT9605A can efficiently switch power MOSFETs at frequency 300kHz typically. Operating in higher frequency should consider the thermal dissipation carefully. Each driver of RT9605A is capable to drive a 3nF load in 30/40ns rising/falling time with little propagation delay from input transition to the gate of the power MOSFET. The device implements bootstrapping on the upper gate with only an external capacitor and a diode required. This reduces circuit complexity and allows the use of higher performance, cost effective N-MOSFETs. All drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. The RT9605A also detects the fault condition during initial start-up prior to the multi-phase PWM controller takes control. As a result, the input supply will latch into the shutdown state. The RT9605A comes to a small footprint package with VQFN-24L 4x4 package.

Ordering Information

RT9605A □ □

- Package Type
  QV : VQFN-24L 4x4 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

- **Drive Six N-MOSFETs for 3-Phase Buck PWM Control**
- **Adaptive Shoot-Through Protection**
- **Support High Switching Frequency**
- **Fast Output Rise/Fall Time**
- **Propagation Delay 40ns**
- **Tri-State Input for Bridge Shutdown**
- **Upper MOSFET Direct Short Protection**
- **Small 24-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

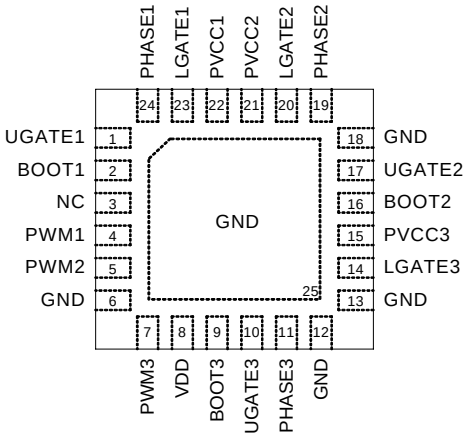
- CPU Core Voltage Supplies on Motherboard
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

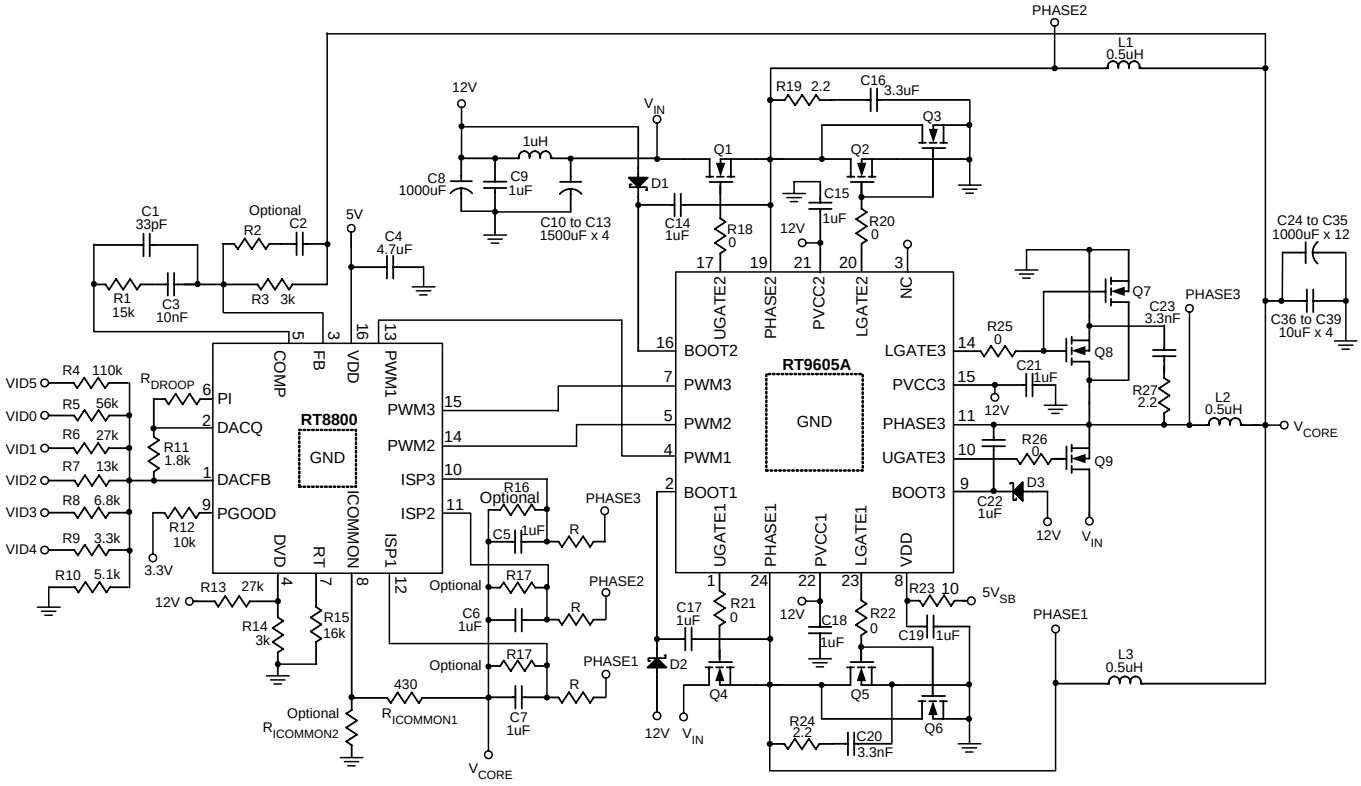
Pin Configurations

(TOP VIEW)



VQFN-24L 4x4

Typical Application Circuit



Functional Pin Description

UGATE1 (Pin 1), UGATE2 (Pin 17), UGATE3 (Pin 10)

Upper Gate Drive Output. Should be connected to the upper MOSFET gate.

BOOT1 (Pin 2), BOOT2 (Pin 16), BOOT3 (Pin 9)

Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

NC (Pin 3)

No connected.

PWM1 (Pin 4), PWM2 (Pin 5), PWM3 (Pin 7)

PWM input control signal. Connect this pin to the PWM output of the controller. If the PWM signal enters and remains within the shutdown window, are both UGATE and LGATE are drived low, disabling the output MOSFETs.

GND [Pin 6, 12, 13, 18, Exposed Pad (25)]

Chip power ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

VDD (Pin 8)

Supply Input. Connect to +5V stand-by power. Place a bypass capacitor between this pin and GND.

PHASE1 (Pin 24), PHASE2 (Pin 19), PHASE3 (Pin 11)

Upper driver return. Should be connected to the common node of upper and lower MOSFETs. The PHASE voltage is monitored for adaptive shoot-through protection.

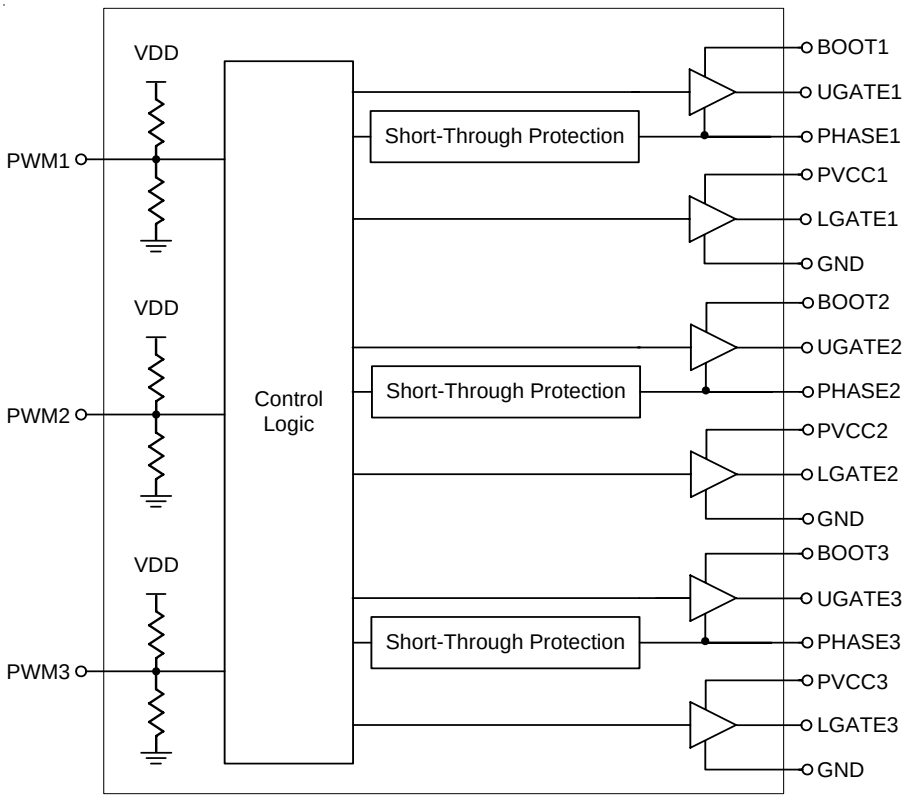
LGATE1 (Pin 23), LGATE2 (Pin 20), LGATE3 (Pin 14)

Lower Gate Drive Output. Should be connected to the lower MOSFET gate.

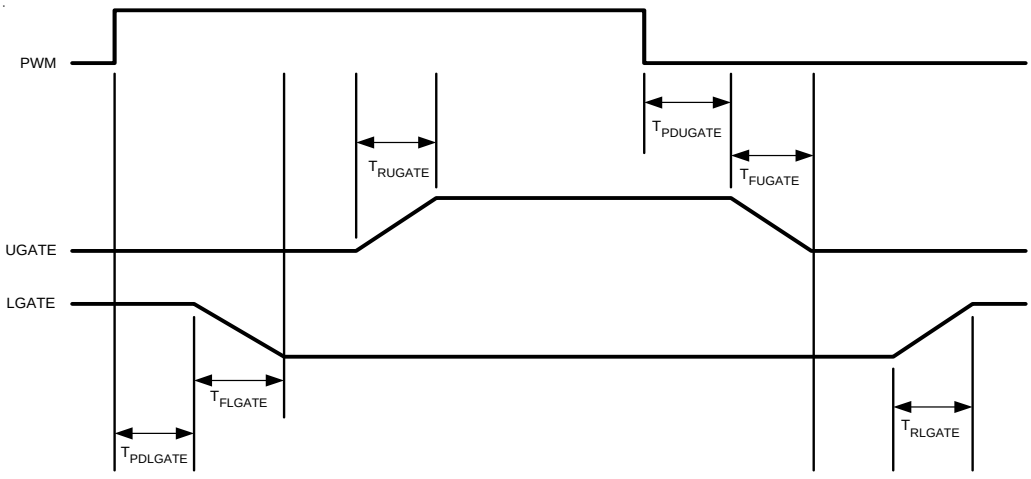
PVCC1 (Pin 22), PVCC2 (Pin 21), PVCC3 (Pin 15)

Supply Input. Connect to +12V supply. Place a bypass capacitor between this pin and PGND.

Function Block Diagram



Timing Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, P_{VCC} ---------- 15V
- Supply Voltage, V_{DD} ---------- 7V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC}+15V
  - < 200ns ---------- –0.3V to 42V
- PHASE to GND ---------- –4V to 15V
- PWM Input Voltage ---------- GND - 0.3V to 7V
- UGATE ---------- V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
- LGATE ---------- GND - 0.3V to V_{PVCC} + 0.3V
- Package Thermal Resistance (Note 4)
  - VQFN-24L 4x4, θ_{JA} ---------- 67°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 2)
  - HBM (Human Body Mode) ---------- 1kV
  - MM (Machine Mode) ---------- 100V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{DD} ---------- 12V ±10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(Recommended Operating Conditions, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDD Supply Current						
Operation Current	I_{VDD}	Frequency = 250kHz	--	--	10	mA
Power-On Reset						
POR Threshold	PV_{CCRTH}	PV_{CC} Rising	6	6.5	7.5	V
Hysteresis	PV_{CCHYS}		--	0.15	--	V
PWM Input						
Input Current	I_{PWM}	V_{PWM_IN} = 0V or 5V	200	300	500	µA
Floating Voltage	V_{PWMFL}	P_{VCC} = 12V	1.8	2.2	2.6	V
PWM Threshold	V_{PWMRTH}	PWM_IN Rising	3.3	3.7	4.3	V
	V_{PWMFTH}	PWM_IN Falling	1.0	1.38	1.5	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output						
UGATE Rise Time	T_{RUGATE}	PV_{CC} = 12V, 3nF load	--	30	--	ns
UGATE Fall Time	T_{FUGATE}	PV_{CC} = 12V, 3nF load	--	40	--	ns
LGATE Rise Time	T_{RLGATE}	PV_{CC} = 12V, 3nF load	--	30	--	ns
LGATE Fall Time	T_{FLGATE}	PV_{CC} = 12V, 3nF load	--	30	--	ns
UGATE Turn-Off Propagation Delay	$T_{PDUGATE}$	PV_{CC} = 12V, 3nF load	--	40	--	ns
LGATE Turn-Off Propagation Delay	$T_{PDLGATE}$	PV_{CC} = 12V, 3nF load	--	35	--	ns
Shutdown Window			1.0	--	4.3	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

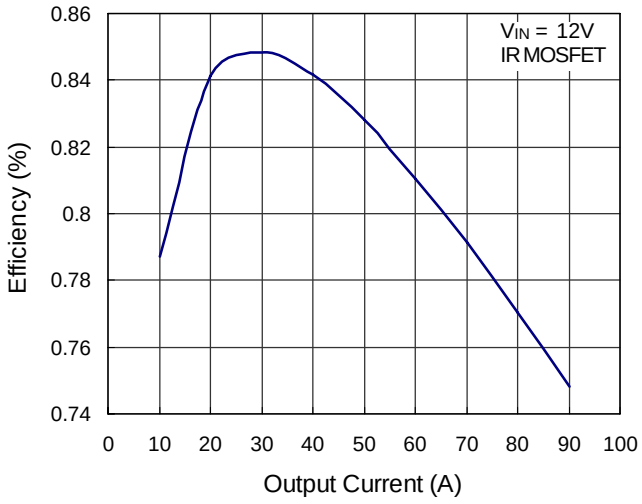
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

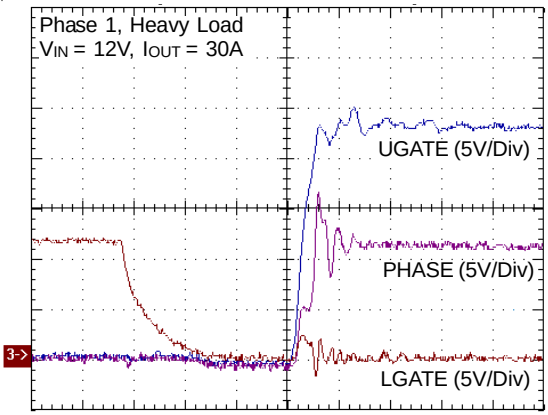
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

Efficiency vs. Output Current

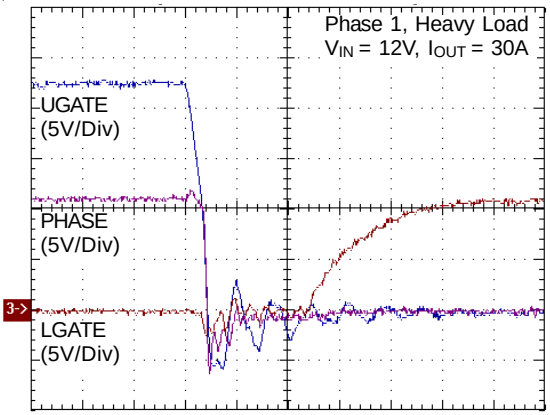


Dead Time



Time (50ns/Div)

Dead Time



Time (50ns/Div)

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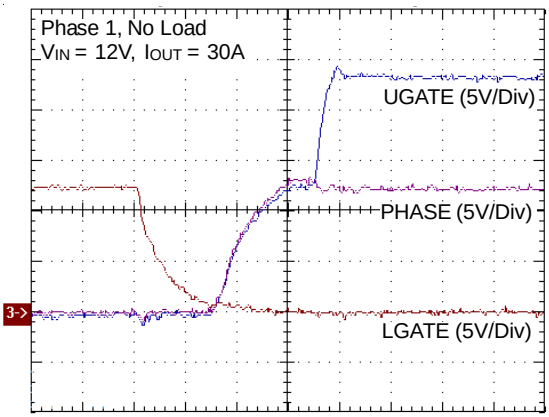
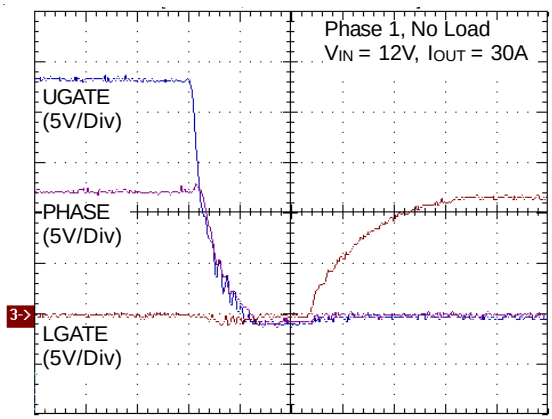


Time (50ns/Div)

Dead Time



Time (50ns/Div)

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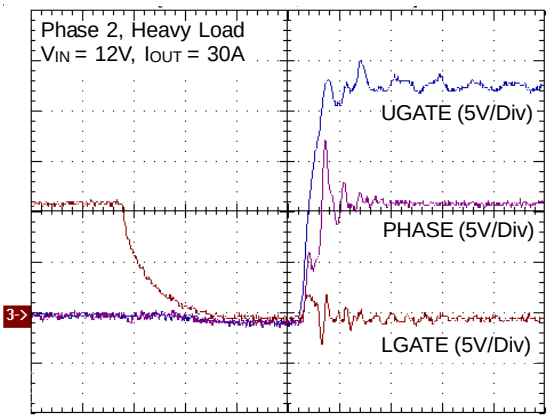
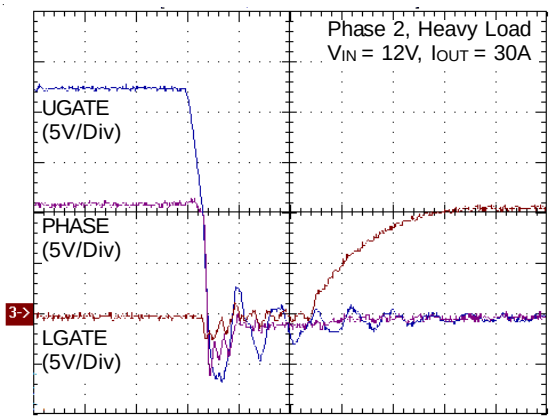


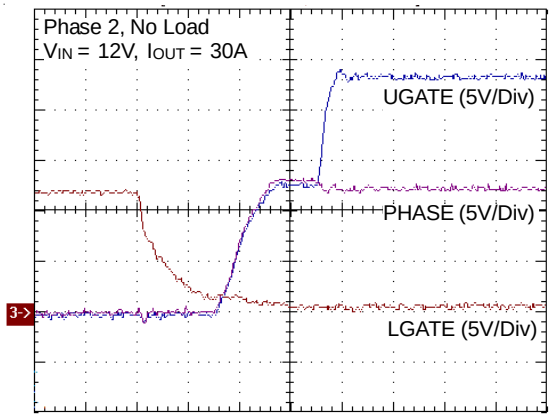
Time (50ns/Div)

Dead Time



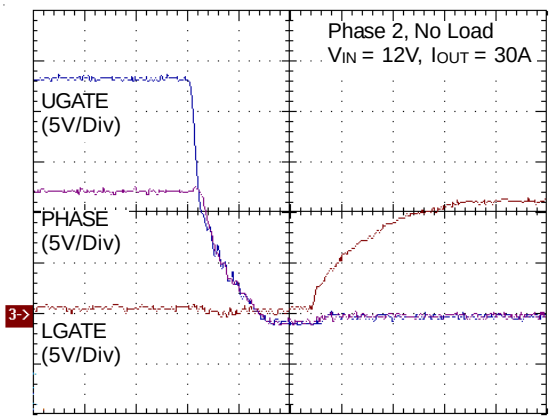
Time (50ns/Div)

Dead Time



Time (50ns/Div)

Dead Time



Time (50ns/Div)

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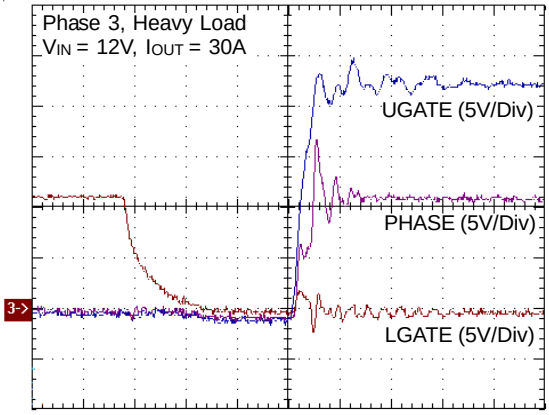
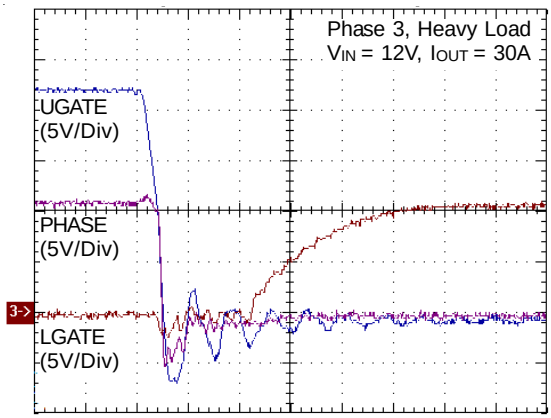


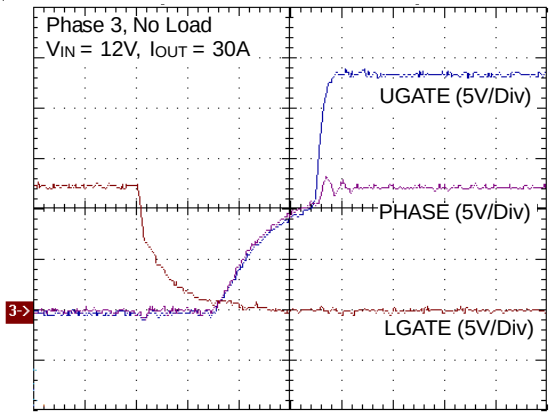
Time (50ns/Div)

Dead Time



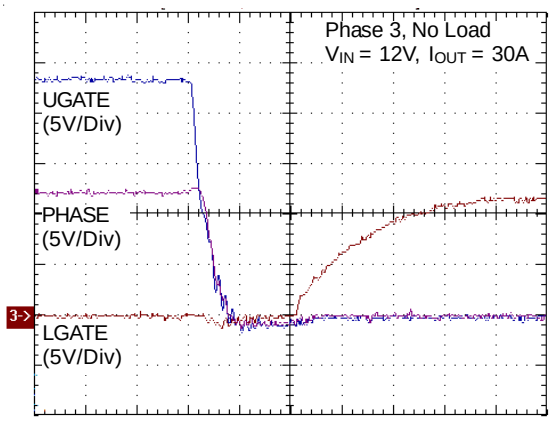
Time (50ns/Div)

Dead Time



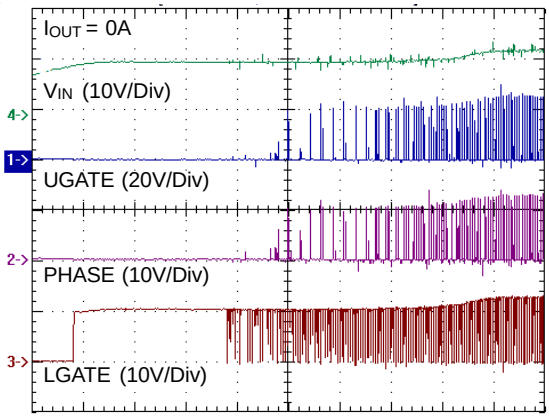
Time (50ns/Div)

Dead Time



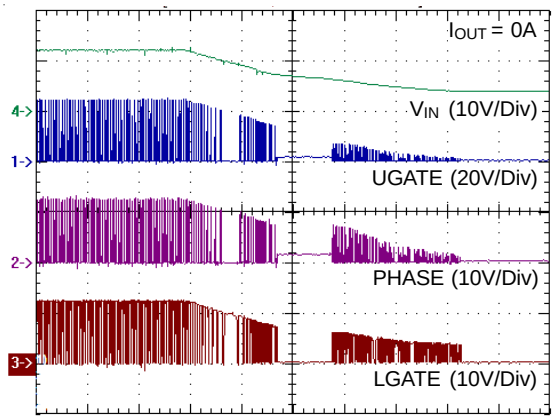
Time (50ns/Div)

Power On



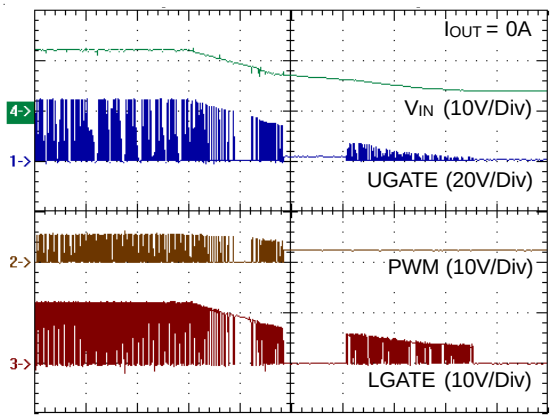
Time (1ms/Div)

Power Off



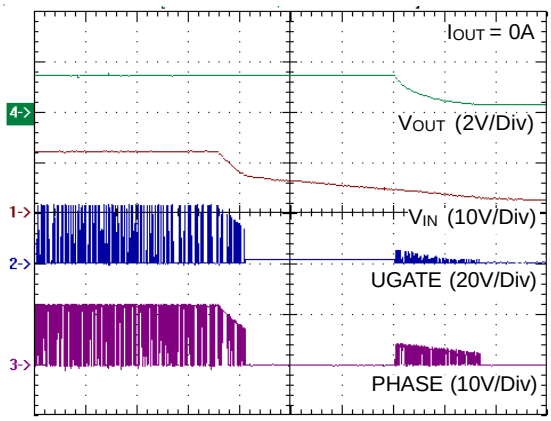
Time (50ms/Div)

Power Off



Time (50ms/Div)

Power Off



Time (250ms/Div)

Application Information

The RT9605A is designed to drive three sets of both high side and low side N-Channel MOSFET through externally input PWM control signal. It has power-on protection function which held UGATE and LGATE low before PV_{CC} rising across the threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE turns low then UGATE is allowed to go high just after a non-overlapping time to avoid shoot-through. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE reach a predetermined low level, LGATE is allowed to turn high. The non-overlapping function is also presented between UGATE and LGATE signal transient.

The PWM signal is acted as "High" if above the rising threshold and acted as "Low" if below the falling threshold. Any signal level remaining within the shutdown window is considered as "tri-state", the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWM signal floating, the pin will be kept at 2.1V by the internal divider and provide the PWM controller with a recognizable level.

The RT9605A typically operates at frequency of 200kHz to 300kHz. It shall be noted that to place a 1N4148 or schottky diode between the PVCC and BOOT pin as shown in the typical application circuit.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs} at 12V, the gate draws the current only few nano-amperes. Thus once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large current to source and sink the gate rapidly. It also needs to switch drain current on and off with high speed. The required gate drive currents are calculated as follows.

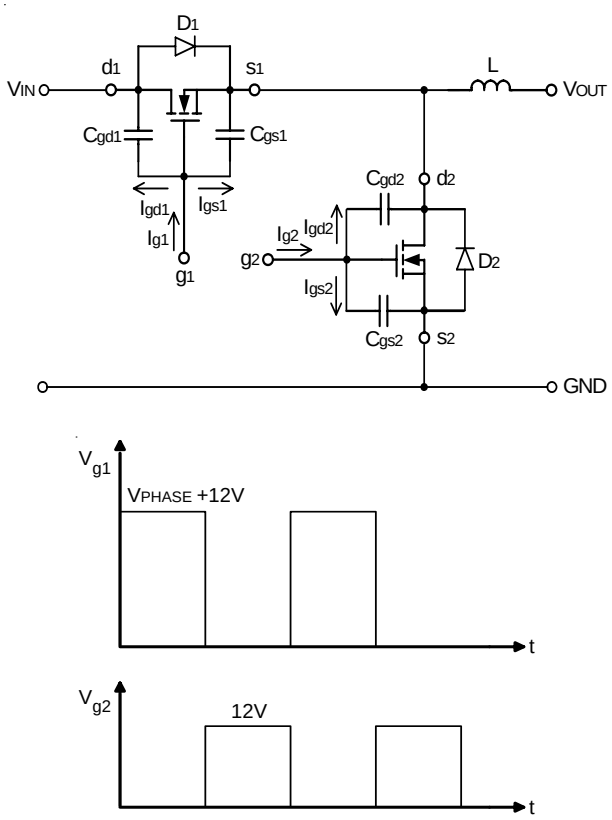


Figure 1. Equivalent Circuit and Associated Waveforms

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 12V. The operation consists of charging C_{gd} and C_{gs}. C_{gs1} and C_{gs2} are the capacitances from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs} is referred as "C_{iss}" which is the input capacitance. C_{gd1} and C_{gd2} are the capacitances from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}" the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and I_{gs2} are showed below:

$$I_{gs1} = C_{gs1}\frac{dV_{g1}}{dt} = \frac{C_{gs1}\times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2}\frac{dV_{g2}}{dt} = \frac{C_{gs2}\times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high side MOSFET up to 12V (or 5V), the low side MOSFET has to be off; and the high side MOSFET is turned off before the low side is turned on. From Figure 1, the body diode "D_2" had been turned on before high side MOSFETs turned on.

$$I_{gd1} = C_{g1}\frac{dV}{dt} = C_{gd1}\frac{12V}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to V_{IN}. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{V_{IN}+12V}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified buck converter, input voltage V_{IN} = 12V, V_{g1} = V_{g2} = 12V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660\times10^{-12}\times12}{14\times10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200\times10^{-12}\times12}{30\times10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380\times10^{-12}\times12}{14\times10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500\times10^{-12}\times12}{30\times10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source is

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.745 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Layout Consideration

Figure 2 shows the schematic circuit of a two-phase synchronous buck converter to implement the either phase of RT9605A. The converter operates at V_{IN} 12V.

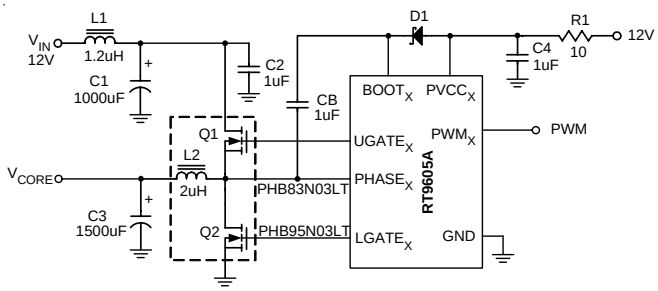


Figure 2. Sync. Buck Converter Circuit

When layout the PC board, it should be very careful. The power-circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 should be very close.

Next, the trace from UGATE, and LGATE to the gates of MOSFET should also be short to decrease the noise of the driver output signals. The bypass capacitor C4 should be connected to GND directly. Furthermore, the bootstrap capacitors (C_B) should always be placed as close to the pins of the IC as possible. The trace from PHASE to the common node of the two MOSFETs should be kept wide since it usually carries large current.

Select the Bootstrap Capacitor

Figure 3 shows part of the bootstrap circuit of RT9605A. The V_{CB} (the voltage difference between BOOT and PHASE pins provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is determined by following constraints.

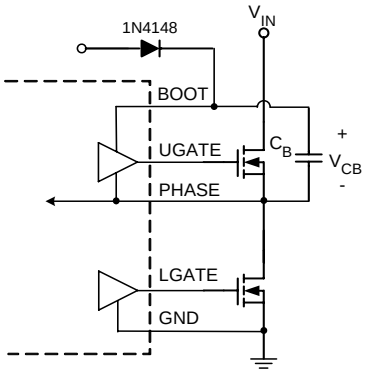


Figure 3. Part of Bootstrap Circuit of RT9605A

In practice, a low value capacitor C_B will lead the over-charging that could damage the IC. Therefore to minimize the risk of overcharging and reducing the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1µF, and the larger the better. In general design, using 1µF can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. Here, to adopt either a ceramic or tantalum capacitor is suitable.

Power Dissipation

For not exceeding the maximum allowable power dissipation to drive the IC beyond the maximum recommended operating junction temperature of 125°C, it is necessary to calculate power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET. Figure 4 shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is 1µF.

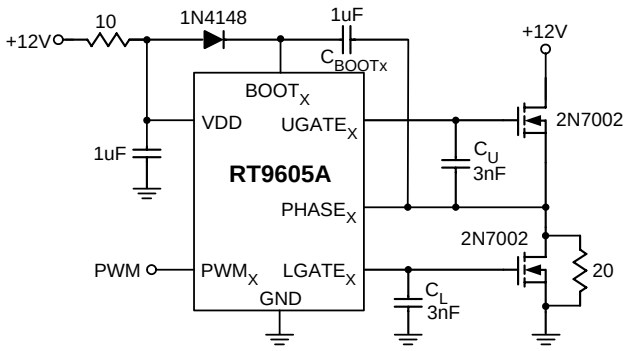


Figure 4. Test Circuit (One Phase is Shown)

Figure 5 shows the power dissipation of the RT9605A as a function of frequency and load capacitance. The value of the C_U and C_L are the same and the frequency is varied from 100kHz to 1MHz.

The operating junction temperature can be calculated from the power dissipation curves (Figure 5). Assume VDD = 12V, operating frequency is 200kHz and the C_U=C_L=1nF which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 5, the power dissipation is 100mW. For RT9605A, the package thermal resistance θ_{JA} is 67°C/W, the operating junction temperature is calculated as :

$$T_J = (67°C/W \times 100mW) + 25°C = 31.7°C \quad (11)$$

where the ambient temperature is 25°C.

The method to improve the thermal transfer is to increase the PC board copper area around the RT9605A firstly. Then, adding a ground pad under IC to transfer the heat to the peripheral of the board.

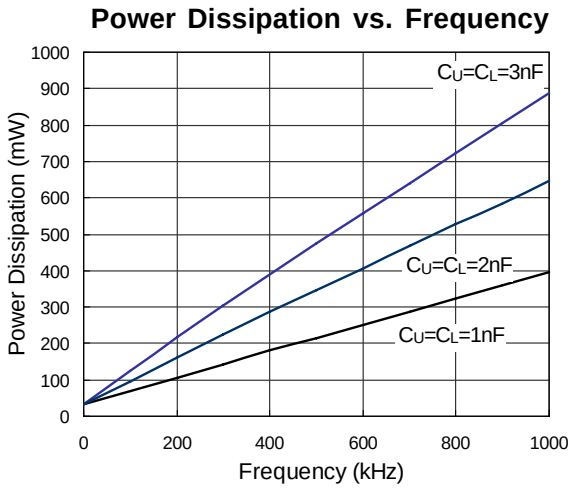


Figure 5. Power Dissipation vs. Frequency

Over-Voltage Protection Function at Power-On

An unique feature of the RT9605A is the addition of over-voltage protection in the event of upper MOSFET direct shorted before power-on. The RT9605A detects the fault condition during initial start-up, the internal power-on OVP sense circuitry will rapidly drive the low side MOSFET on before the multi-phase PWM controller takes control.

Figure 6 shows the measured waveforms with the high side MOSFET directly shorted to 12V.

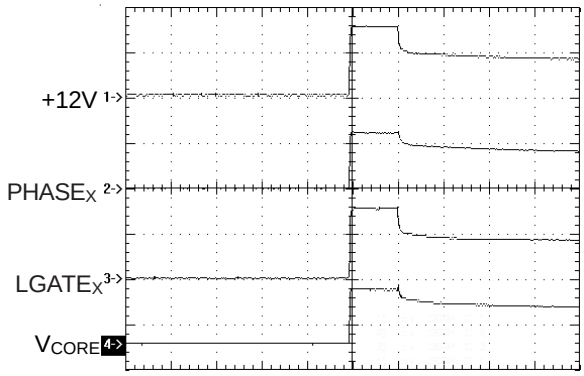
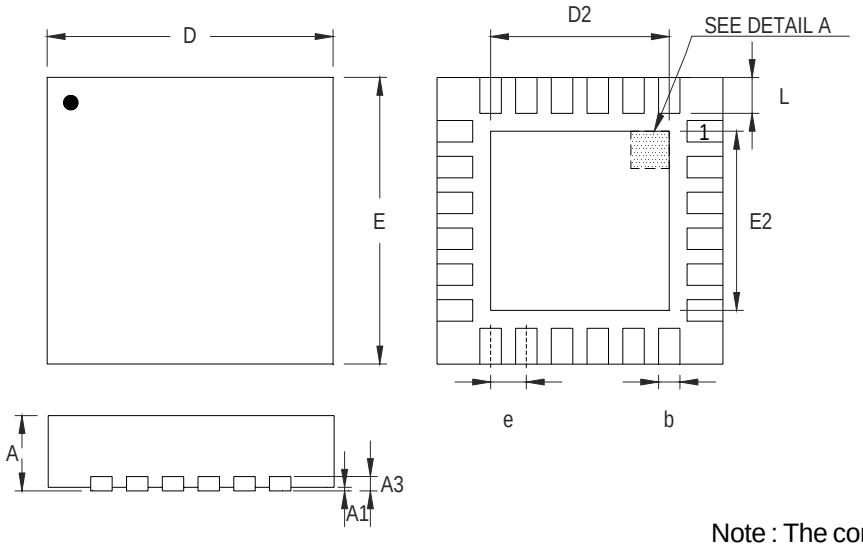
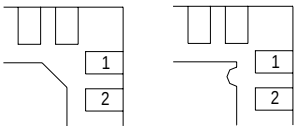


Figure 6. Waveforms at High Side MOSFET Shorted

Please note that the +12V trigger point to RT9605A is at 3V, and the clamped level on PHASE pin is at about 2.4V. Obviously since the PHASE pin voltage increases during initial start-up, the V_{CORE} increases correspondingly, but it would quickly drop-off following the voltage in LGATE and +12V.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 24L QFN 4x4 Package

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