Multi-Phase PWM Controller for CPU Core Power Supply

General Description

The RT9243 is a multi-phase buck DC/DC controller integrated with all control functions for GHz CPU VRM. The RT9243 controls 2, 3 or 4 buck switching stages operating in interleaved phase set automatically. The multi-phase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9243 controls both voltage and current loops to achieve good regulation, response & power stage thermal balance. Precise current loop using $R_{DS(ON)}$ as sense component builds precise load line for strict VRM DC & transient specification and also ensures thermal balance of different power stages. The settings of current sense, droop tuning, V_{CORE} initial offset and over current protection are independent to compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning.

The DAC output of RT9243 supports VRD10.x by 6-bit V_{ID} input, precise initial value & smooth V_{CORE} transient at VI_{ID} jump. The IC monitors the V_{CORE} voltage for PGOOD and over-voltage protection. Soft-start, over-current protection and programmable under-voltage lockout are also provided to assure the safety of microprocessor and power system.

Ordering Information

RT9243□□

- Package Type
  - S : SOP-32
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100%matte tin (Sn) plating.

Features

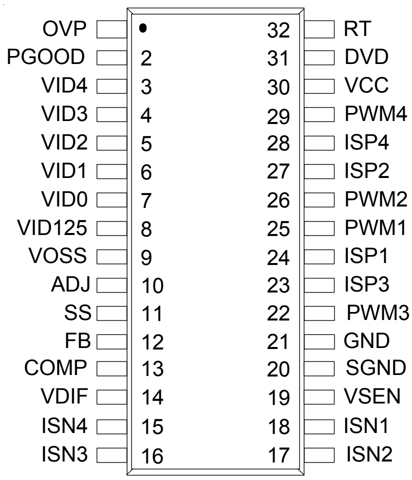
- **Multi-Phase Power Conversion with Automatic Phase Selection**
- **VRD10.x DAC Output with Active Droop Compensation for Fast Load Transient**
- **Smooth V_{CORE} Transition at VID Jump**
- **Power Stage Thermal Balance by $R_{DS(ON)}$ Current Sense**
- **Hiccup Mode Over-Current Protection**
- **Programmable Switching Frequency (50kHz to 400kHz per Phase), Under-Voltage Lockout and Soft-Start**
- **High Ripple Frequency Times Channel Number**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Intel® Processors Voltage Regulator: VRD10.x
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

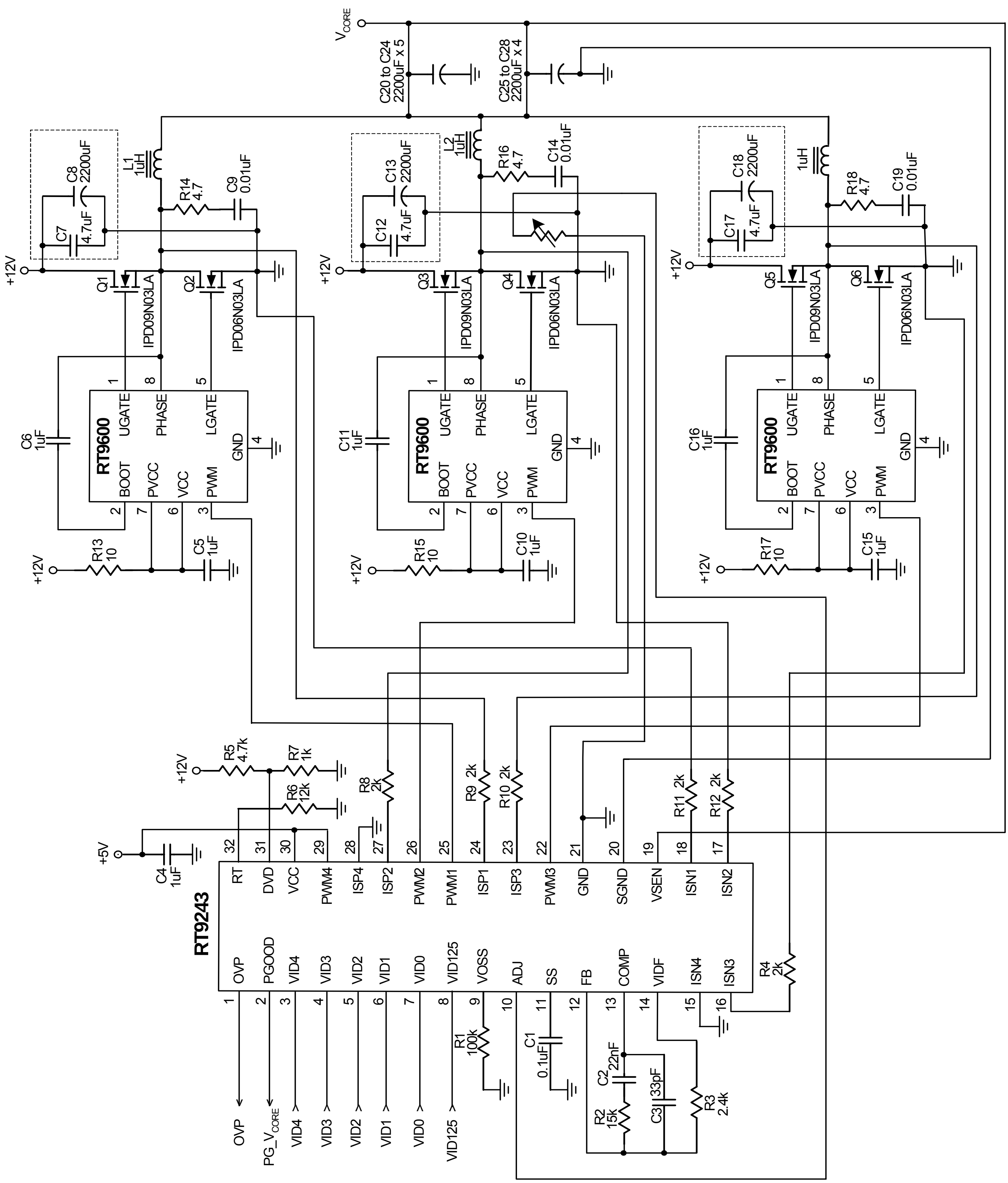
Pin Configurations

(TOP VIEW)



SOP-32

Typical Application Circuit



Functional Pin Description

OVP (Pin 1)

Over voltage trip output.

PGOOD (Pin 2)

Power good open-drain output.

VID4 (Pin 3), VID3 (Pin 4), VID2 (Pin 5), VID1 (Pin 6), VID0 (Pin 7) & VID125 (Pin 8)

DAC voltage identification inputs for VRD10.x. These pins are internally pulled to 3V if left open.

VOSS (Pin 9)

V_{CORE} initial value offset. Connect this pin to GND with a resistor to set the offset value.

ADJ (Pin 10)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the load droop.

SS (Pin 11)

Connect this SS pin to GND with a capacitor to set the soft-start time interval. Pulling this pin below 1V (ramp valley of sawtooth wave in pulse width modulator) would make all PWMs low, turn on low side MOSFETs and turn off high side MOSFETs.

FB (Pin 12)

Inverting input of the internal error amplifier.

COMP (Pin 13)

Output of the error amplifier and input of the PWM comparator.

VDIF (Pin 14)

V_{CORE} differential sense output.

VSEN (Pin 19)

V_{CORE} differential sense positive input.

SGND (Pin 20)

V_{CORE} differential sense negative input.

GND (Pin 21)

Ground for the IC.

PWM1 (Pin 25), PWM2 (Pin 26), PWM3 (Pin 22) & PWM4 (Pin 29)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver. For systems which use 3 channels, connect PWM4 high. Two channel systems connect PWM3 and PWM4 high.

ISN1 (Pin 18), ISN2 (Pin 17), ISN3 (Pin 16) & ISN4 (Pin 15)

$R_{DS(ON)}$ current sense inputs from each individual converter channel sense component's GND node.

ISP1 (Pin 24), ISP2 (Pin 27), ISP3 (Pin 23) & ISP4 (Pin 28)

$R_{DS(ON)}$ current sense inputs for each individual converter channel. Tie this pin to the component's sense node.

VCC (Pin 30)

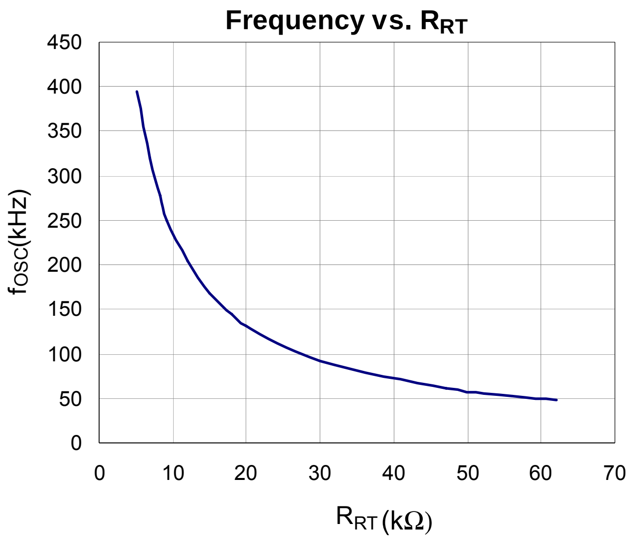
IC power supply. Connect this pin to a 5V supply.

DVD (Pin 31)

Programmable power UVLO detection input. Trip threshold = 2V at V_{DVD} rising.

RT (Pin 32)

Switching frequency setting. Connect this pin to GND with a resistor to set the frequency.



Function Block Diagram

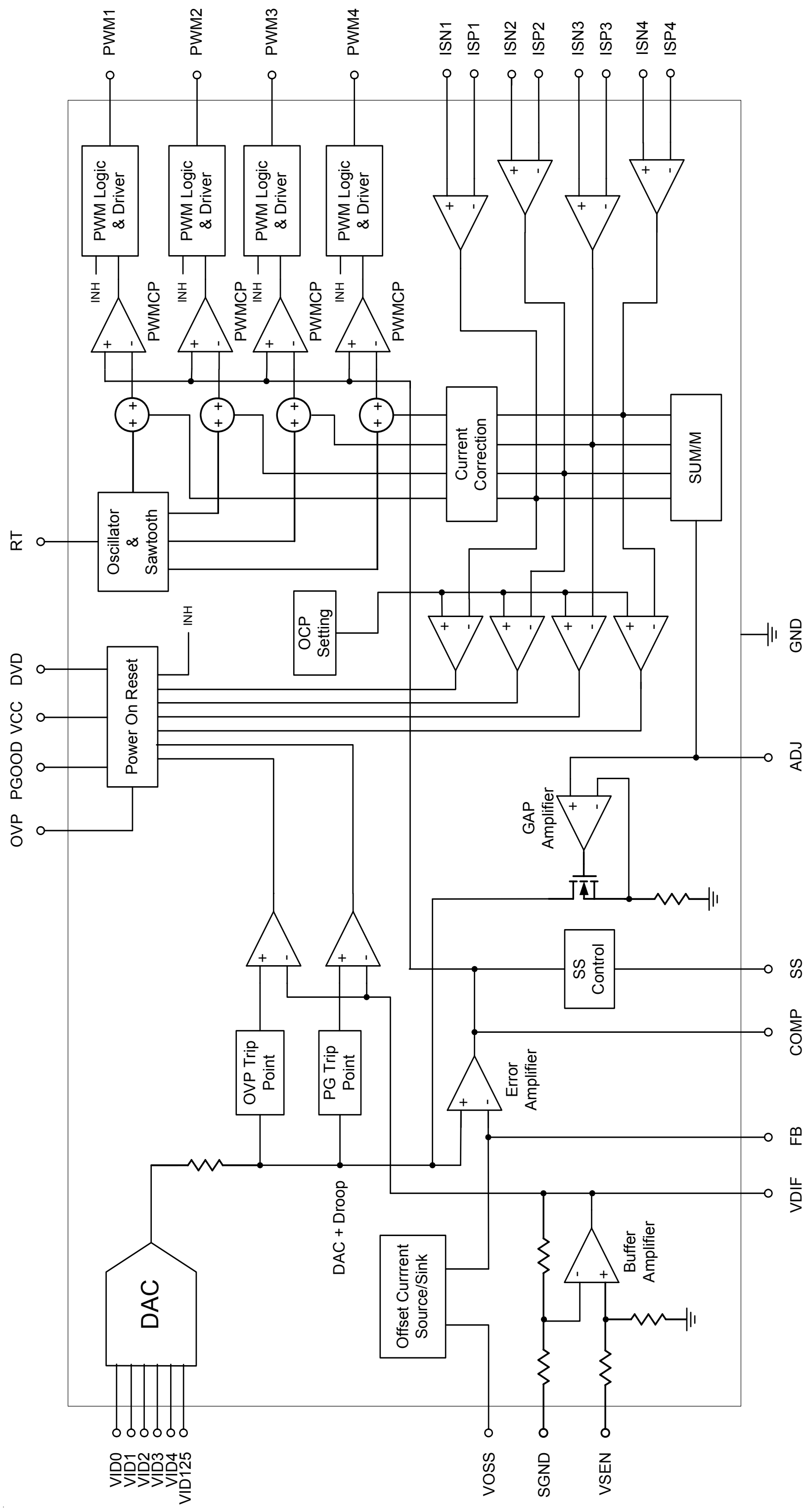


Table 1. Output Voltage Program

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	1	1	1	X	No CPU
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.850V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.875V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.900V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.925V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.950V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.025V
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.050V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.075V
0	0	0	0	0	0	1.0875V
1	1	1	1	0	1	1.100V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.125V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.150V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.175V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.200V
1	1	0	1	0	0	1.2125V

To be continued

Table 1. Output Voltage Program

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	0	0	1	1	1.225V
1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.250V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.275V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.300V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.325V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.350V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.375V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.400V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.425V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.450V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.475V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.500V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.525V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.550V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.575V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Note: (1) 0 : Connected to GND
(2) 1 : Open
(3) X : Don't Care

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 7V
- Input, Output or I/O Voltage ---------- GND-0.3V to V_{CC}+0.3V
- Package Thermal Resistance
  SOP-32, θ_{JA} ---------- 50°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 5V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current							
Nominal Supply Current		I_{CC}	PWM 1,2,3,4 Open	--	12	16	mA
Power-On Reset							
POR Threshold		V_{CCRTH}	V_{CC} Rising	4.0	4.2	4.5	V
Hysteresis		V_{CCHYS}		0.2	0.5	--	V
V_{DVD} Threshold	Trip (Low to High)	V_{DVDTP}	Enable	1.9	2.0	2.1	V
	Hysteresis	V_{DVDHYS}		--	100	--	mV
Oscillator							
Free Running Frequency		f_{OSC}	R_{RT} = 12kΩ	170	200	230	kHz
Frequency Adjustable Range		f_{OSC_ADJ}		50	--	400	kHz
Ramp Amplitude		ΔV_{OSC}	R_{RT} = 12kΩ	--	1.9	--	V
Ramp Valley		V_{RV}		0.7	1.0	--	V
Maximum On-Time of Each Channel				62	66	75	%
RT Pin Voltage		V_{RT}	R_{RT} = 12kΩ	0.55	0.60	0.65	V
Reference and DAC							
DACOUT Voltage Accuracy		ΔV_{DAC}	$V_{DAC} \geq 1V$	–1	--	+1	%
			V_{DAC} < 1V	–10	--	+10	mV
DAC (VID0-VID125) Input Low		V_{ILDAC}		--	--	0.4	V
DAC (VID0-VID125) Input High		V_{IHDAC}		0.8	--	--	V

To be continued

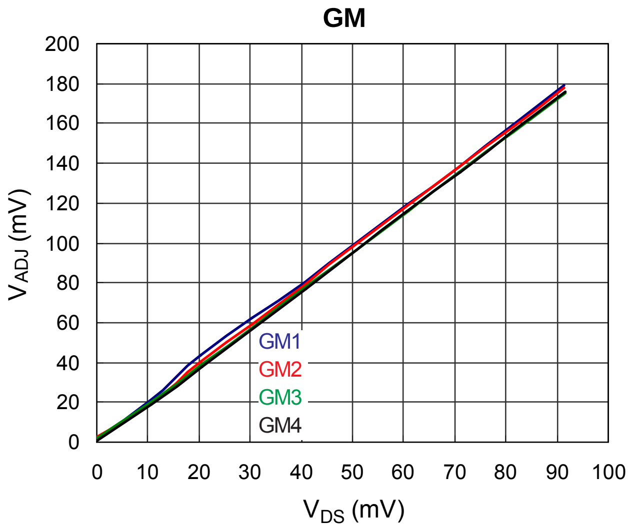
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DAC (VID0-VID125) Bias Current	I_{BIAS_DAC}		60	120	180	μA
VOSS Pin Voltage	V_{VOSS}	R_{VOSS} = 100kΩ	0.95	1.0	1.05	V
Error Amplifier						
DC Gain			--	85	--	dB
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR	COMP = 10pF	--	3	--	V/μs
Differential Sense Amplifier						
Input Impedance	Z_{IMP}		--	16	--	kΩ
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR		--	3	--	V/μs
Current Sense GM Amplifier						
ISP 1,2,3,4 Full Scale Source Current	I_{ISPFSS}		60	--	--	μA
ISP 1,2,3,4 Current for OCP	I_{ISPOCP}		--	100	--	μA
Protection						
SS Current	I_{SS}	V_{SS} = 1V	8	13	18	μA
Over-Voltage Trip (VSEN/DACOUT)	ΔOVT		130	140	150	%
OVP Voltage	V_{OVP}	I_{OVP} = 4mA	--	--	0.2	V
Power Good						
Lower Threshold (VSEN/DACOUT)	V_{PGOOD-}	VSEN Rising	--	92	--	%
Output Low Voltage	V_{PGOODL}	I_{PGOOD} = 4mA	--	--	0.2	V

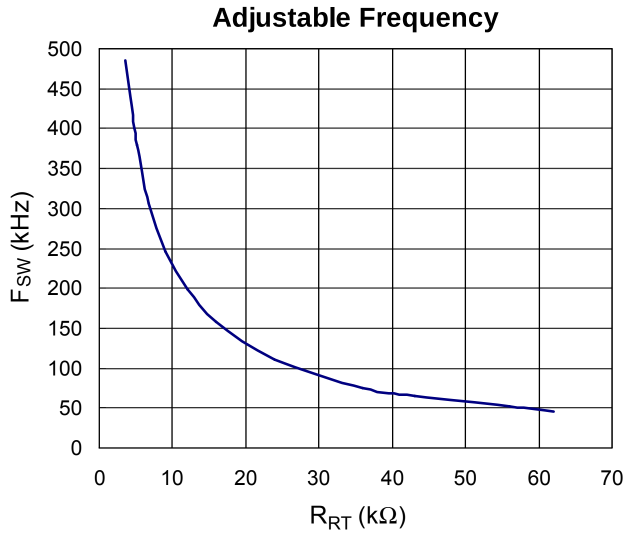
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

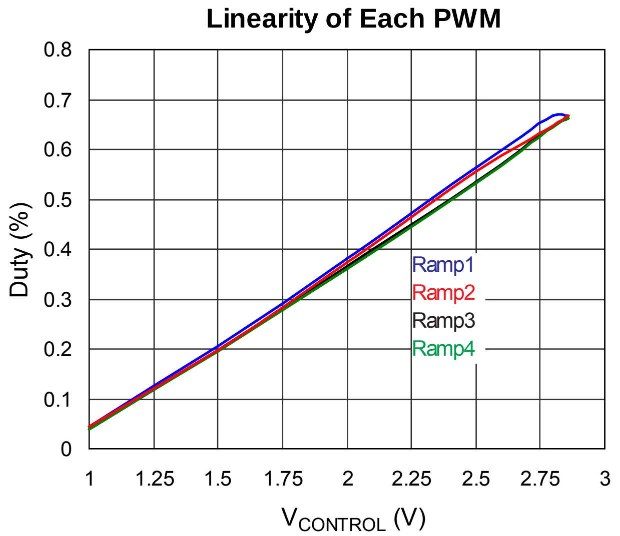
Note 2. Devices are ESD sensitive. Handling precaution recommended.

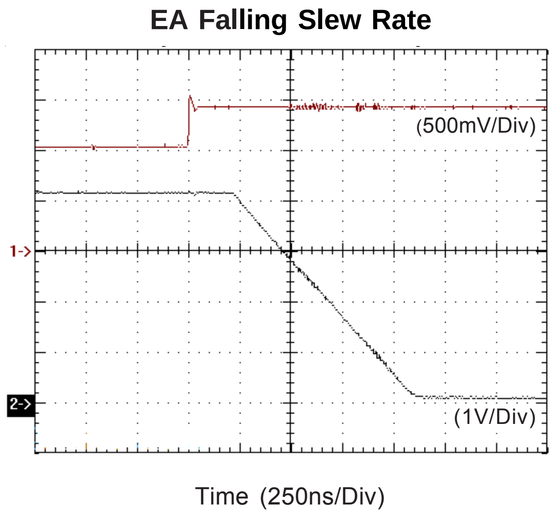
Note 3. The device is not guaranteed to function outside its operating conditions.

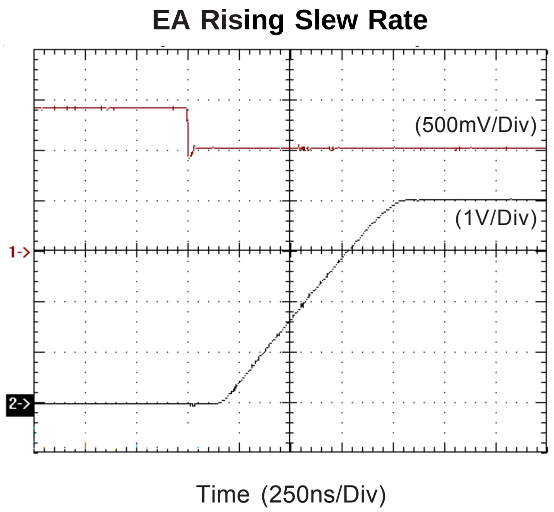
Typical Operating Characteristics

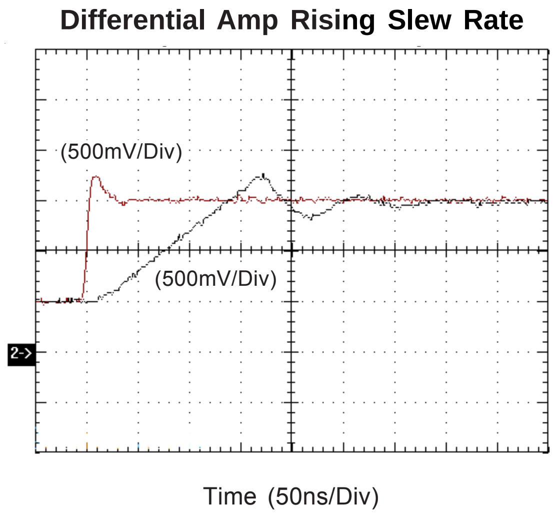




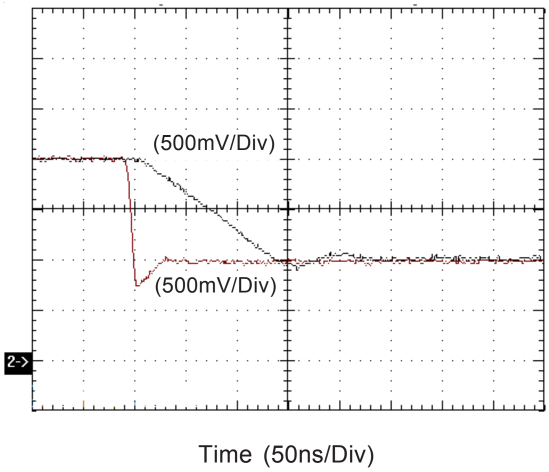




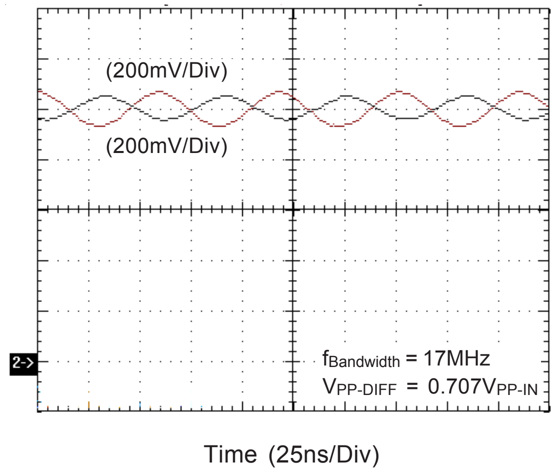




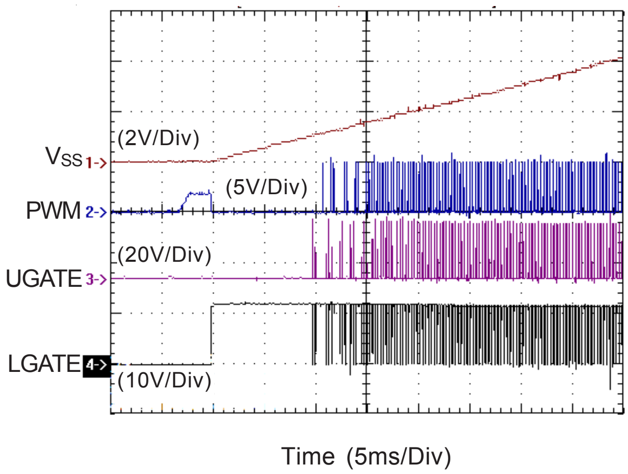
Differential Amp Falling Slew Rate



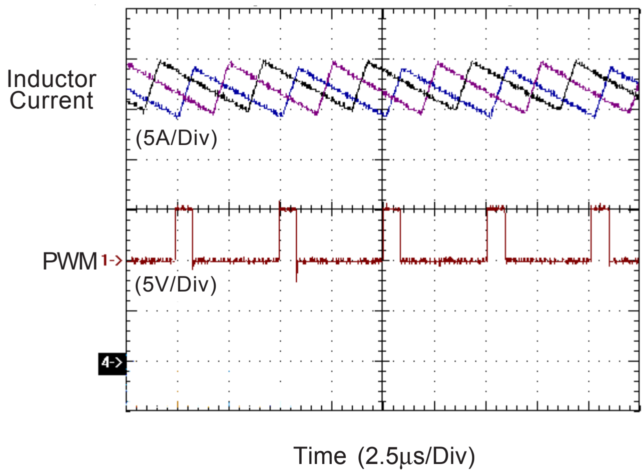
The Bandwidth of Differential Amplifier



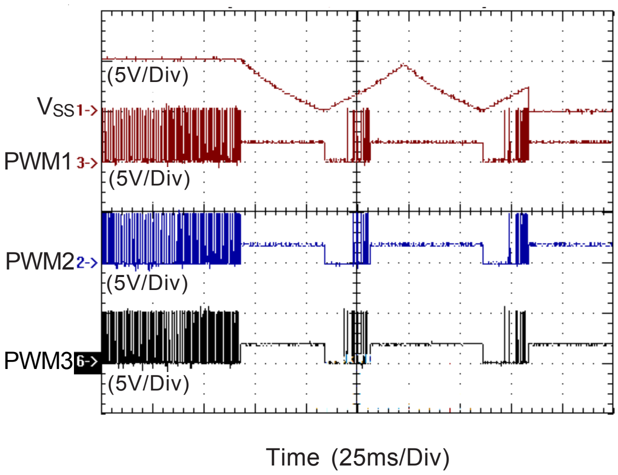
Start-up Waveforms @I_{OUT} = 60A



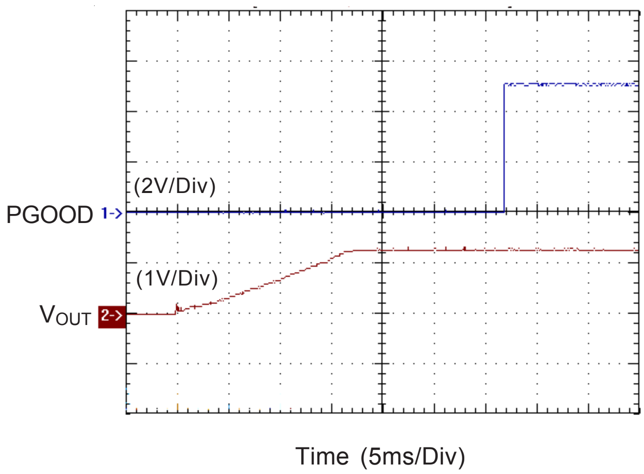
Current Sharing at I_{OUT} = 80A



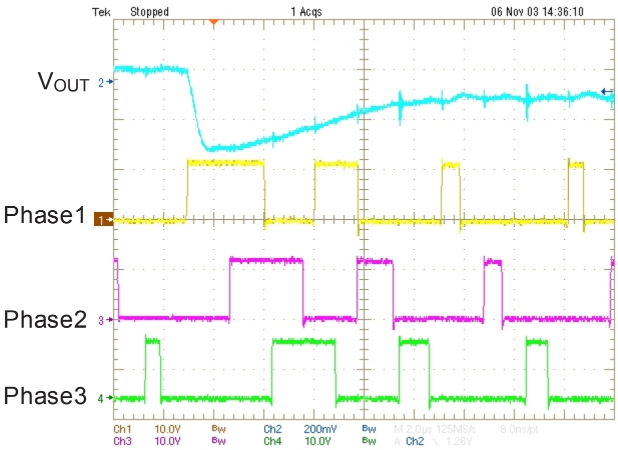
Over Current Protection



PGOOD Waveform



Transient Response



Application Information

RT9243 is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consisting of RT9243 and its companion MOSFET driver provides high quality CPU power and all protection functions to meet the requirement of modern VRM.

Voltage Control

RT9243 senses the CPU V_{CORE} by an precise instrumental amplifier to minimize the voltage drop on PCB trace at heavy load. VSEN & SGND are the differential inputs. VDIF is the output node of the differential voltage & the input for PGOOD & OVP sense. The internal high accuracy VID DAC provides the reference voltage for VRD10.x compliance. Control loop consists of error amplifier, multi-phase pulse width modulator, driver and power components. Like conventional voltage mode PWM controller, the output voltage is locked at the V_{REF} of error amplifier and the error signal is used as the control signal V_C of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase saw-tooth wave. Power stage transforms V_{IN} to output by PWM signal on-time ratio.

Current Balance

RT9243 senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal balance circuit. The current balance circuit sums and averages the current signals and then produces the balancing signals injected to pulse width modulator. If the current of some power channel is greater than average, the balancing signal reduces the output pulse width to keep the balance.

Load Droop

The sensed power channel current signals regulate the reference of DAC to form a output voltage droop proportional to the load current. The droop or so-called "active voltage positioning" can reduce the output voltage ripple at load transient and the LC filter size.

Fault Detection

The chip detects V_{CORE} for over voltage and power good detection. The "hiccup mode" operation of over-current protection is adopted to reduce the short circuit current. The inrush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

Phase Setting and Converter Start Up

RT9243 interfaces with companion MOSFET drivers (like RT9600, RT9602 series) for correct converter initialization. The tri-state PWM output (high, low and high impedance) pins sense the interface voltage at IC POR period (both VCC and DVD trip). The channel is enabled if the pin voltage is 1.2V less than VCC. Please tie the PWM output to VCC and the current sense pins to GND or left floating if the channel is unused. For 3-Channel application, connect PWM4 high.

Current Sensing Setting

RT9243 senses the current of low side MOSFET in each synchronous rectifier when it is conducting for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the $R_{DS(ON)}$ of the low side MOSFET) to current signal into internal circuit (see Figure 1).

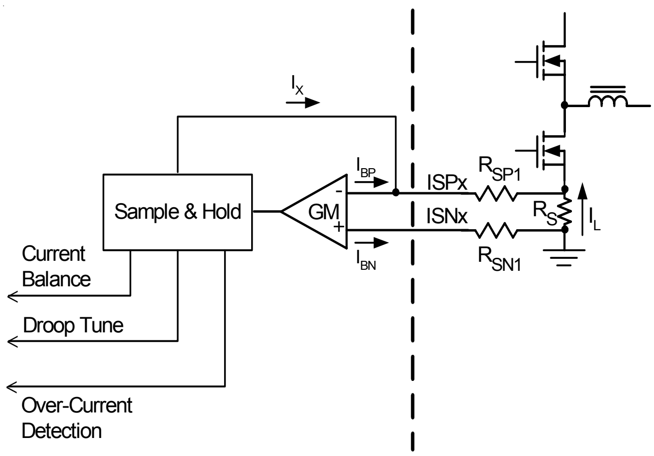


Figure 1. Current Sense Circuit

The sensing circuit gets $I_X = \frac{I_L \times R_S}{R_{SP}}$ by local feedback. $R_{SP} = R_{SN}$ to cancel the voltage drop caused by GM amplifier input bias current. I_X is sampled and held just before low side MOSFET turns off (See Figure 2). Therefore,

$$I_{X(S/H)} = \frac{I_{L(S/H)} \times R_S}{R_{SP}}, I_{L(S/H)} = I_{L(AVG)} - \frac{V_{OUT}}{L} \times \frac{T_{OFF}}{2},$$

$$T_{OFF} = \left[\frac{V_{IN} - V_{OUT}}{V_{IN}}\right] \times 5\mu s \quad \text{for fosc} = 200\text{kHz}$$

$$I_{X(S/H)} = \left[I_{L(AVG)} - \frac{V_{OUT} - \left[\frac{V_{IN} - V_{OUT}}{V_{IN}}\right] \times 5\mu s}{2L} \right] \times \frac{R_S}{R_{SP}}$$

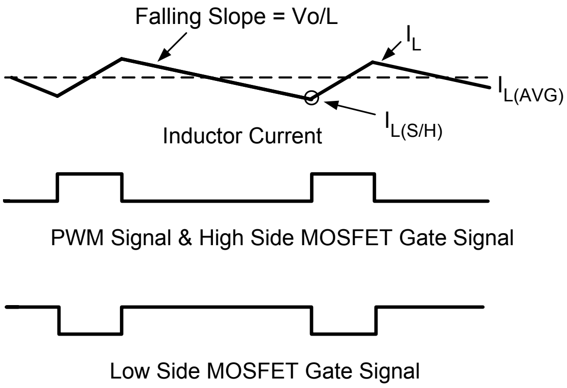


Figure 2. Inductor Current and PWM Signal

DAC Offset Voltage & Droop Tuning

The DAC offset voltage is set by compensation network & VOSS pin external resistors by $\left(\frac{1V}{R_{VOSS}}\right) \times \frac{R_{f1}}{4}$.

The S/H current signals from power channels are injected to ADJ pin to create droop voltage. $V_{ADJ} = R_{ADJ} \times \sum 2I_X$ The DAC output voltage decreases by V_{ADJ} to form the V_{CORE} load droop (see Figure 3).

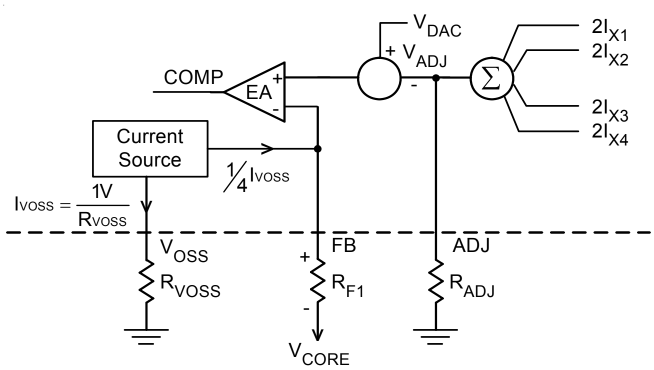


Figure 3. DAC Offset Voltage & Droop Tune Circuit

Protection and SS Function

For OVP, the RT9243 detects the V_{CORE} by V_{DIF} pin voltage of the differential amplifier output. Eliminate the delay due to compensation network (compared to sensing FB voltage) for fast and accurate detection. The trip point of OVP is 140% of normal output level. The PWM outputs are pulled low to turn on the low side MOSFET and turn off the high side MOSFET of the synchronous rectifier at OVP. The OVP latch can only be reset by V_{CC} or DVD restart power on reset sequence. The PGOOD detection trip point of V_{CORE} is 92% lower than the normal level. The PGOOD open drain output pulls low when V_{CORE} is lower than the trip point. For V_{ID} jumping issue, only power fail conditions (V_{CC} & DVD are lower than trip point or OVP) reset the output low.

Soft-start circuit generates a ramp voltage by charging external capacitor with 13µA current after IC POR acts. The PWM pulse width and V_{CORE} are clamped by the rising ramp to reduce the inrush current and protect the power devices.

Over-current protection trip point is internally set at around 100µA for each channel. OCP is triggered if one channel S/H current signal $I_X > \left(\frac{0.6V}{9K}\right) \times 1.5$. Controller forces PWM output latched at high impedance to turn off both high and low side MOSFETs in the power stage and initial the hiccup mode protection. The SS pin voltage is pulled low with a 13µA current after it is less than 90% V_{CC}. The converter restarts after SS pin voltage < 0.2V. Three times of OCP disable the converter and only release the latch by POR acts (see Figure 4).

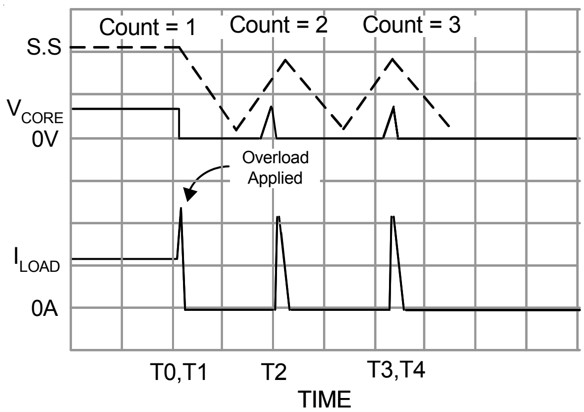
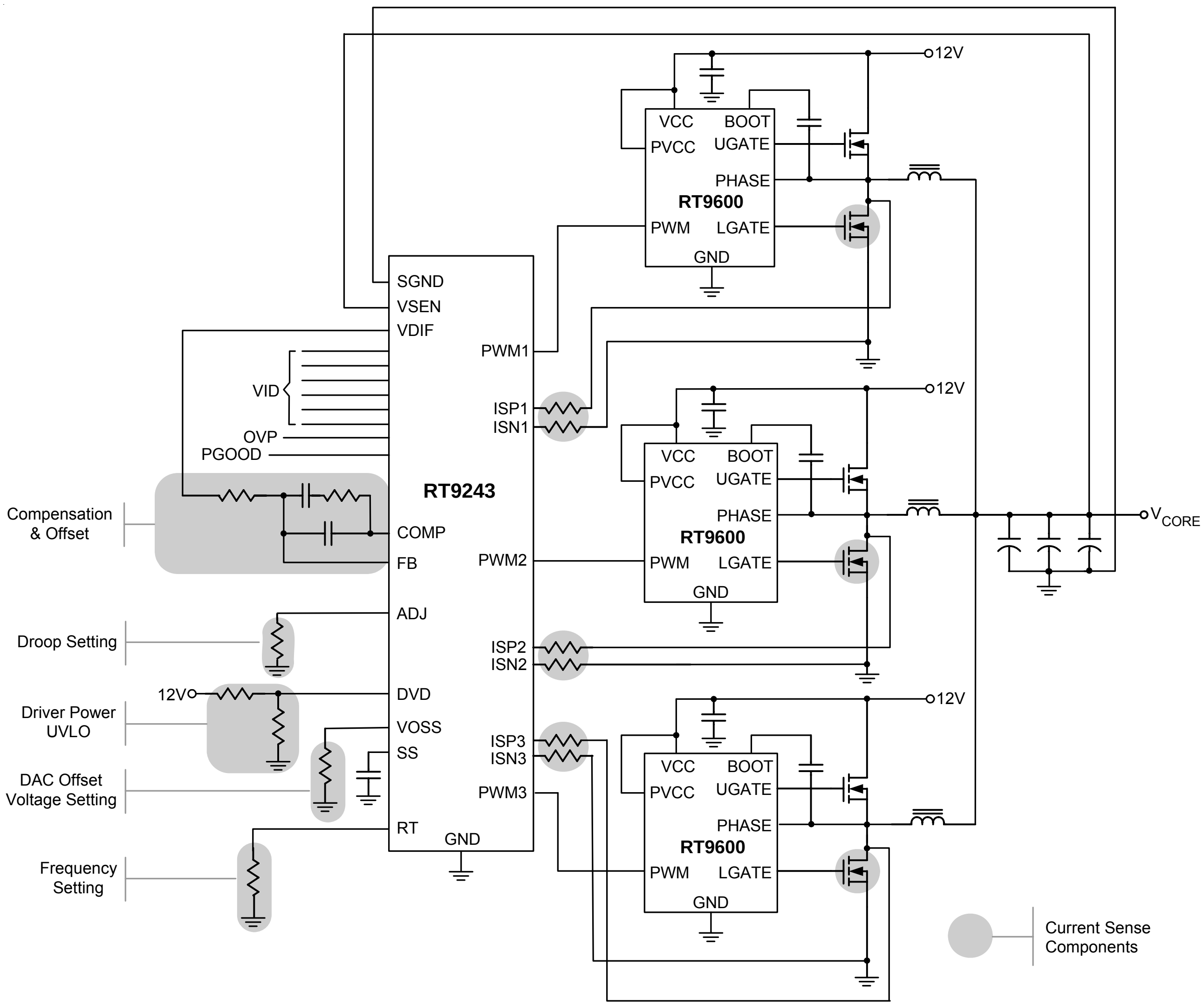


Figure 4.

3-Phase Converter and Components Function Grouping



Design Procedure Suggestion

Voltage Loop Setting

a. Output filter pole and zero (Inductor, output capacitor value & ESR).

b. Error amplifier compensation & sawtooth wave amplitude (compensation network).

c. Kelvin sense for V_{CORE}.

Current Loop Setting

a. GM amplifier S/H current (current sense component Ron, ISPx & ISNx pin external resistor value, keep ISPx current < 60μA at full load condition for better load line linearity).

b. Over-current protection trip point (Internal setting, keep ISPx current < 100μA at OCP condition for precision issue).

VRM Load Line Setting

a. Droop amplitude (ADJ pin resistor).

b. No load offset (additional resistor in compensation network).

c. DAC offset voltage setting (VOSS pin & compensation network resistor).

Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

a. Kelvin sense for current sense GM amplifier input.

b. Refer to layout guide for other item.

Design Example

Given:

Apply for three phase converter

V_{IN} = 12V

V_{CORE} = 1.5V

$I_{LOAD(MAX)}$ = 60A

V_{DROOP} = 120mV at full load

OCP trip point set at 33A for each channel (S/H)

$R_{DS(ON)}$ = 6mΩ of low side MOSFET at 27°C

L = 2μH

C_{OUT} = 9,000μF with 2mΩ ESR.

1. Compensation Setting

a. Modulator Gain, Pole and Zero:

From the following formula:

$$\text{Modulator Gain} = \frac{V_{IN}}{V_{RAMP}} = \frac{12V}{1.9V \times \frac{3}{2}} = 4.2\ (12.46dB)$$

where V_{RAMP} : ramp amplitude of sawtooth wave

$$\text{LC Filter Pole} = \frac{1}{2\pi \times \sqrt{LC}} = 1.2\text{kHz and}$$

$$\text{ESR Zero} = \frac{1}{2\pi \times ESR \times C_{OUT}} = 8.8\text{kHz}$$

b. EA Compensation Network :

Select R1 = 2.4kΩ, R2 = 24kΩ, C1 = 6.6nF, C2 = 33pF and use the type 2 compensation scheme shown in Figure 5.

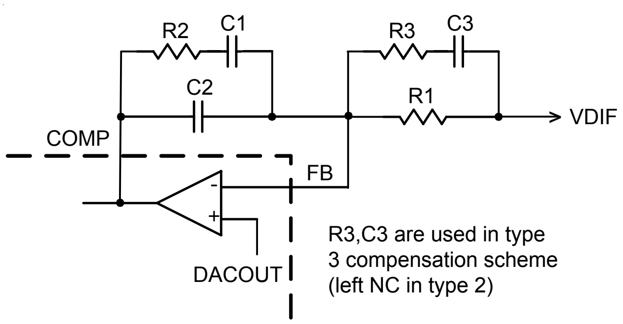


Figure 5.

From the following formulas :

$$F_Z = \frac{1}{2\pi \times R_2 \times C_1},\quad F_P = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$\text{Middle Band Gain} = \frac{R_2}{R_1}$$

By calculation, the F_Z = 1kHz, F_P = 200kHz and Middle Band Gain is 10 (i.e 20dB).

The asymptotic bode plot of EA compensation and PWM loop gain is shown as Figure 6.

Asymptotic Bode Plot of PWM Loop Gain

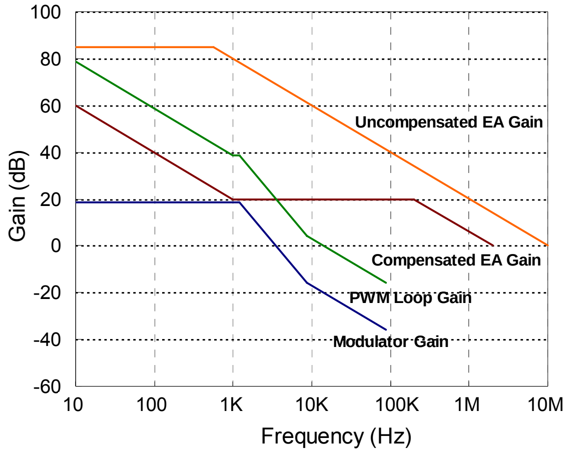


Figure 6.

2. Droop & DAC Offset Setting

For each channel the load current is 60A / 3 = 20A and the ripple current, ΔI_L, is given as :

$$5us \times \frac{1.5V}{2uH} \times \left(1 - \frac{1.5V}{12V}\right) = 3.28A$$

The load current, I_L, at S/H is $20A - \frac{\Delta I_L}{2} = 18.36A$.

Using the following formula to select the appropriate $I_{X\,(MAX)}$ for the S/H of GM amplifier :

$$I_{X\,(MAX)} = \frac{R_{DS(ON)} \times 18.36A}{R_{SP}}$$

The suggested I_X is in the order of 50 to 60μA, select $R_{SP} = R_{SN}$ = 2kΩ, then $I_{X\,(MAX)}$ will be 55μA.

V_{DROOP} = 120mV = 55μA × 2 × 3 (phase no.) × R_{ADJ}, therefore R_{ADJ} will be 360Ω.

The $R_{DS(ON)}$ of MOSFET varies with temperature rise. When the low side MOSFET working at 70°C and 5000ppm/°C temperature coefficient of $R_{DS(ON)}$, the $R_{DS(ON)}$ at 70°C is given as :

6mΩ × {1+ (70°C − 27°C) × 5000ppm/°C} = 7.3mΩ.

R_{ADJ} at 70°C is given as :

$R_{ADJ\_27°C} \times (R_{DS(ON)\_27°C} / R_{DS(ON)\_70°C})$ = 296Ω

3. Over-Current Protection Setting

OCP trip point is internally set at around 100μA of I_X for each channel. As above-selected $R_{SP} = R_{SN}$ = 2kΩ, the OCP trip point is found using :

$$I_{X\,(OCP)} = \frac{R_{DS(ON)} \times I_{L\,(TRIP)}}{R_{SP}} = \frac{6m\Omega \times 33A}{2K\Omega} = 100\,\mu A$$

4. Soft-Start Capacitor Selection

C_{SS} = 0.1μF is the suitable value for most application.

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. **Most critical path: the current sense circuit is the most sensitive part of the converter. The current sense resistors tied to ISP1,2,3,4 and ISN1,2,3,4 should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. Kelvin connection of the sense component (additional sense resistor or MOSFET $R_{DS(ON)}$) ensures the accurate stable current sensing.**

Keep well Kelvin sense to ensure the stable operation!

2. Switching ripple current path:
   a. Input capacitor to high side MOSFET.
   b. Low side MOSFET to output capacitor.
   c. The return path of input and output capacitor.
   d. Separate the power and signal GND.
   e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.
   f. Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.
3. MOSFET driver should be closed to MOSFET.
4. The compensation, bypass and other function setting components should be near the IC and away from the noisy power path.

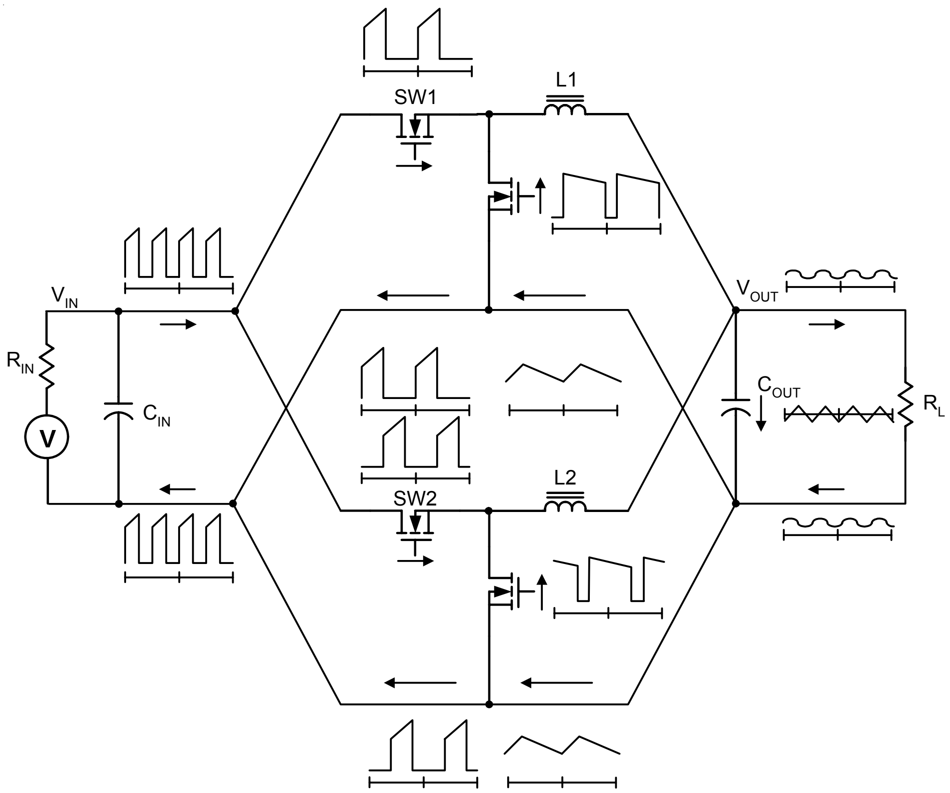


Figure 7. Power Stage Ripple Current Path

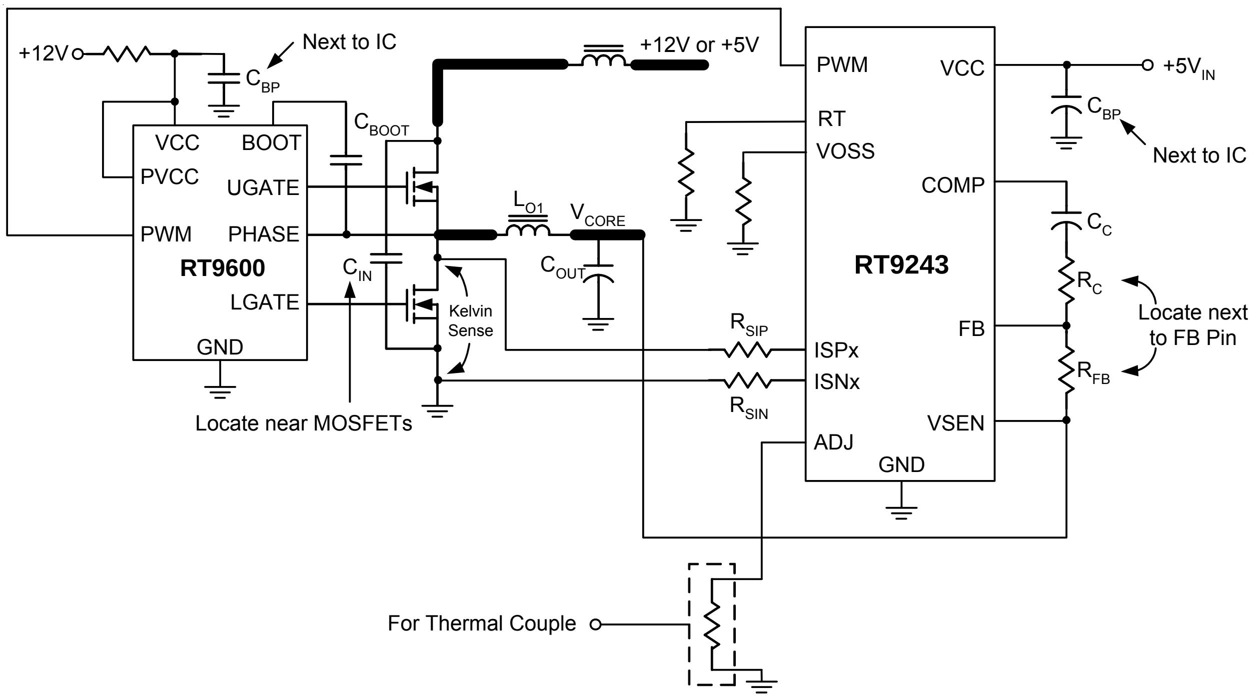
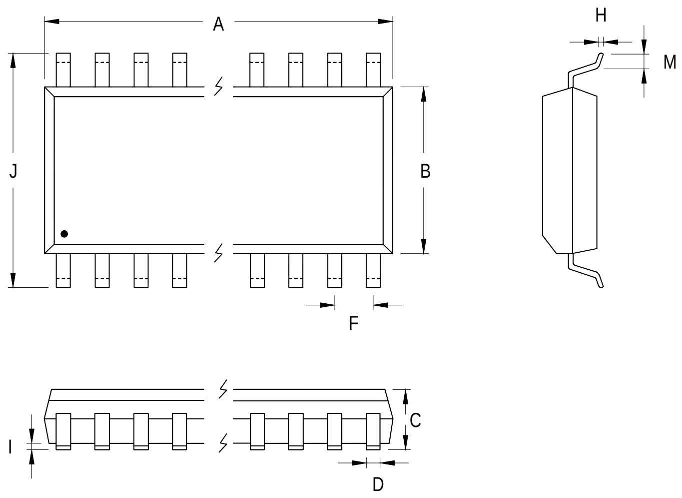


Figure 8. Layout Consideration

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	20.320	20.726	0.800	0.816
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.27		0.050	
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

32-Lead SOP Plastic Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
8F, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com