

Features

- Typical propagation delay: 20nS
- Wide power supply range: 2 - 6V
- Low quiescent current: 80 μ A maximum
- Low input current: 1 μ A maximum
- Fan out of 10 LS-TTL loads

Description

The PT74HC138 decoder utilizes advanced silicon-gate CMOS technology and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

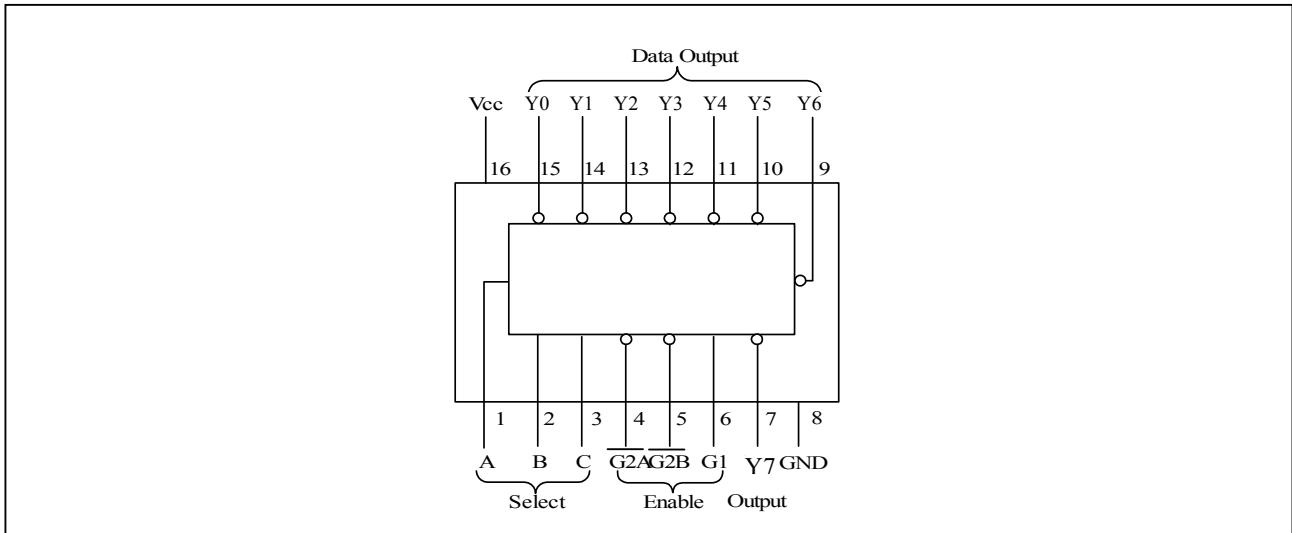
The PT74HC138 has 3 binary select inputs (A, B and C). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables ($\overline{G1}$, $\overline{G2A}$ and $\overline{G2B}$) are provided to ease the cascading of decoders.

Ordering Information

Ordering No.	Package
PT74HC138W	SOIC-16
PT74HC138WE	Lead free SOIC-16
PT74HC138P	PDIP-16
PT74HC138PE	Lead free PDIP-16

The decoder's outputs can drive 10 low power Schottky TTL equivalent loads and are functionally pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Information



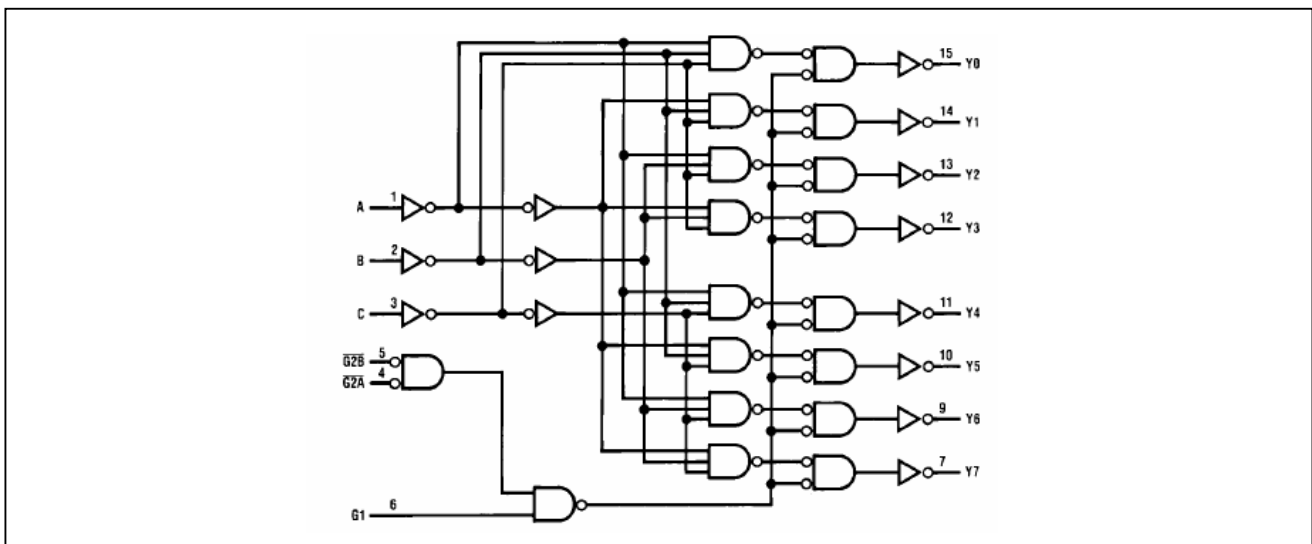
Truth table

Enable		Inputs			Outputs							
G1		Select										
G1	$\overline{G2}$ (Note)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H=HIGH Level, L=LOW Level, X=Don't care.

Note: $\overline{G2} = G2A + G2B$

Logic Diagram



Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (V _{CC} to GND).....	-0.5V to 7.0V
DC Input Voltage (V _{IN}).....	-1.5V to V _{CC} +1.5V
DC Output Voltage (V _{OUT}).....	-0.5V to V _{CC} +0.5V
Clamp Diode Current (I _R , I _{OK}).....	±20mA
DC Output Current, per pin (I _{OUT}).....	±25mA
DC V _{CC} or GND Current, per pin (I _{CC}).....	±50mA
Power Dissipation (P _D) *.....	600mW
S. O. Package only.....	500mW

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

* Power Dissipation temperature derating - plastic *PDIP* package: -12mW/°C from 65°C to 85°C.

Recommended operation conditions

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Supply voltage	-	2.0	-	6.0	V
V _{IN} , V _{OUT}	DC input or output voltage	-	0.0	-	V _{CC}	V
T _A	Operating temperature	-	-40	-	85	
T _r , T _f	Input rise or fall time	V _{CC} =2.0V	-	-	1000	nS
		V _{CC} =4.5V	-	-	500	
		V _{CC} =6.0V	-	-	400	

DC Electrical Characteristics

Sym	Parameter	Test Conditions	V _{CC}	T _A =25		T _A = -40 to 85		Unit
				Typ	Guaranteed Limits	Typ	Guaranteed Limits	
V _{IH}	Minimum High Level Input Voltage	-	2.0V	-	1.5	1.5	V	
			4.5V		3.15			3.15
			6.0V		4.2			4.2
V _{IL}	Maximum LOW Level Input Voltage	-	2.0V	-	0.5	0.5	V	
			4.5V		1.35			1.35
			6.0V		1.8			1.8
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	V	
			6.0V	5.7	5.48	5.34		
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1		
			6.0V	0	0.1	0.1		
		V _{IN} = V _{IH} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	V	
6.0V	0.2	0.26	0.33					
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V	-	±0.1	±0.1	μA	
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V	-	8	80	μA	

AC Electrical Characteristics

($V_{CC}=5V$, $T_A=25^{\circ}C$, $C_L=15pF$, $t_r=t_f=6nS$, Unless otherwise noted.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, Binary select to any output	-	18	25	nS
t_{PHL}	Maximum Propagation Delay, Binary select to any output	-	28	35	nS
t_{PLH}, t_{PHL}	Maximum Propagation Delay, G1 to any output	-	18	25	nS
t_{PHL}	Maximum propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to output	-	23	30	nS
t_{PLH}	Maximum propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to output	-	18	25	nS

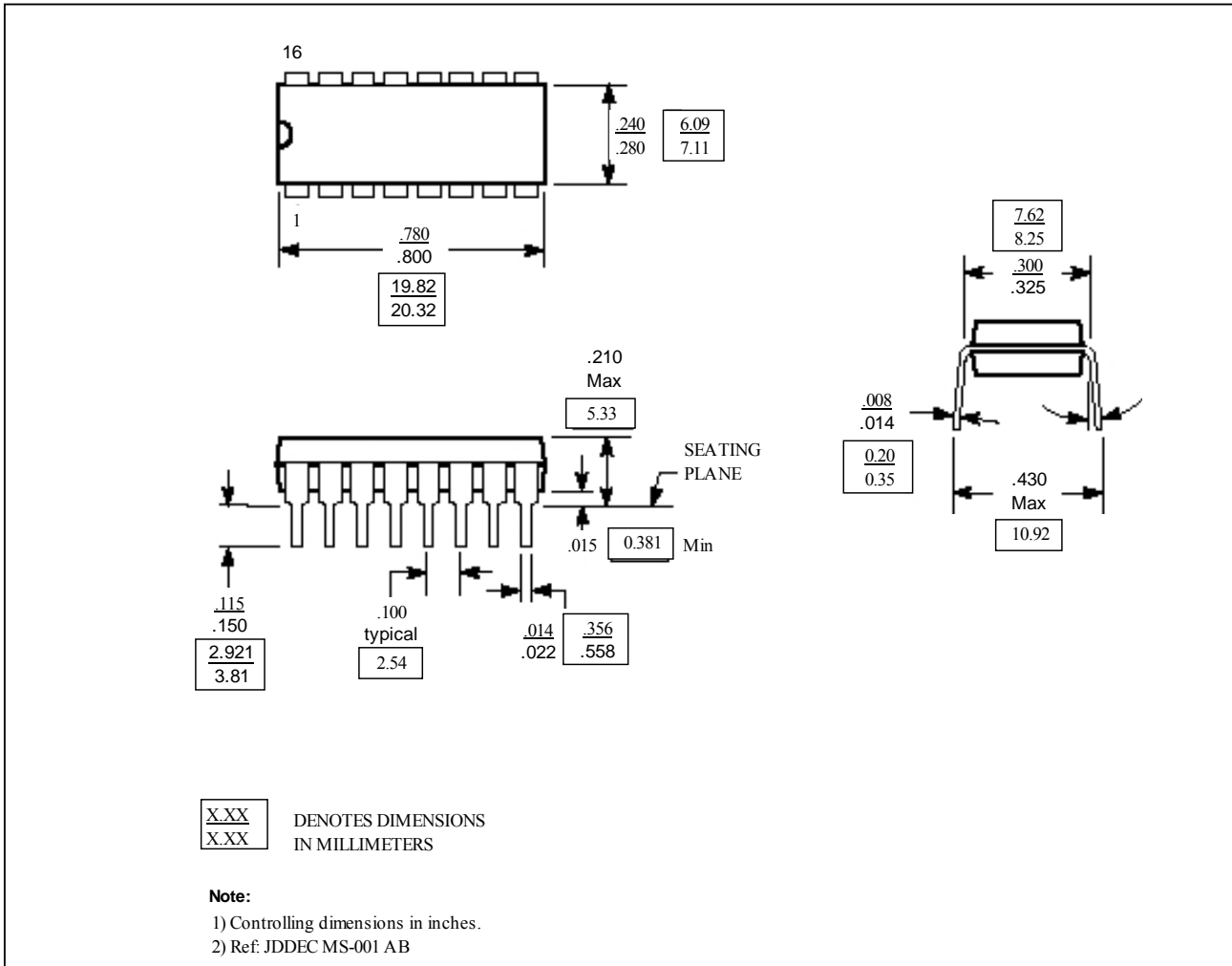
($V_{CC}=2.0V$ to $6.0V$, $C_L=50pF$, $t_r=t_f=6nS$, Unless otherwise noted.)

Sym	Parameter	Conditions	V_{CC}	$T_A=25^{\circ}C$		$T_A= -40$ to $85^{\circ}C$	Units
				Typ	GuaranteedLimits		
t_{PLH}	Maximum propagation Delay Binary Select to any output LOW-to-HIGH	-	2.0V	75	150	189	nS
			4.5V	15	30	38	
			6.0V	13	26	32	
t_{PHL}	Maximum Propagation Delay Binary Select to any output HIGH-to-LOW	-	2.0V	100	200	252	nS
			4.5V	20	40	50	
			6.0V	17	34	43	
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1 to any output	-	2.0V	75	150	189	nS
			4.5V	15	30	38	
			6.0V	13	26	32	
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to output	-	2.0V	82	175	221	nS
			4.5V	28	35	44	
			6.0V	22	30	37	
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to output	-	2.0V	75	150	189	nS
			4.5V	15	30	38	
			6.0V	13	26	32	
t_{TLH}, t_{THL}	Output Rise and Fall Time	-	2.0V	30	75	95	nS
			4.5V	8	15	19	
			6.0V	7	13	16	
C_{PD}	Power Dissipation Capacitance (Note)	-	-	75	-	-	pF
C_{IN}	Maximum Input Capacitance	-	-	3	10	10	pF

Note: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f + I_{CC}V_{CC}$, and the no load dynamic current consumption. $I_S=C_{PD}V_{CC}f + I_{CC}$.

Mechanical Information

P/PE (PDIP-16)



Notes

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