

**Single Digitally-Controlled (XDCP™) Potentiometer**

The X9111 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

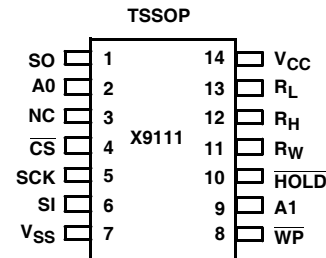
The digital controlled potentiometer is implemented using 1023 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Powerup recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

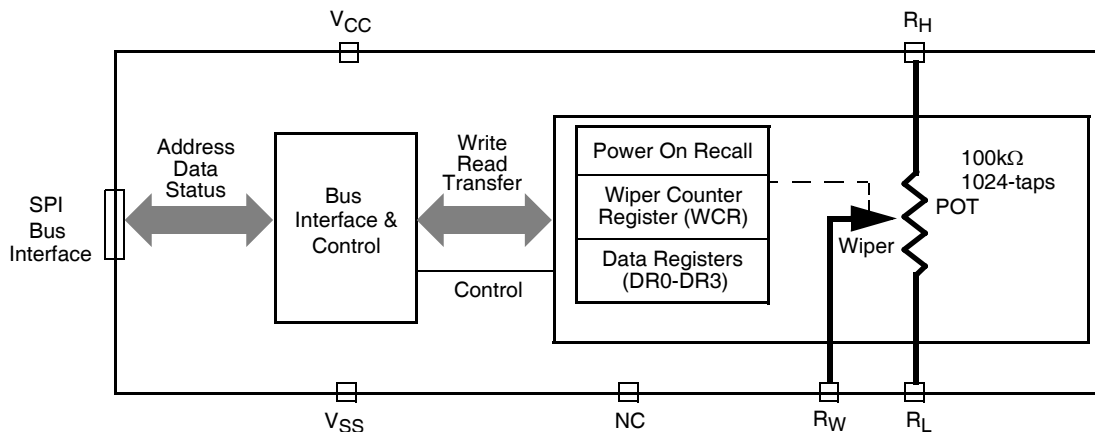
**Features**

- 1024 Resistor Taps – 10-Bit Resolution
- SPI Serial Interface for Write, Read, And Transfer Operations Of The Potentiometer
- Wiper Resistance, 40Ω Typical @ 5V
- Four Non-Volatile Data Registers
- Non-Volatile Storage of Multiple Wiper Positions
- Power On Recall. Loads Saved Wiper Position on Power-Up.
- Standby Current <3μA Max
- V<sub>CC</sub>: 2.7V to 5.5V Operation
- 100kΩ End to End Resistance
- 100 yr. Data Retention
- Endurance: 100,000 Data Changes Per Bit Per Register
- 14 Ld TSSOP
- Low Power CMOS
- Single Supply Version of the X9110
- Pb-Free Plus Anneal Available (RoHS Compliant)

**Pinout**



**Functional Diagram**



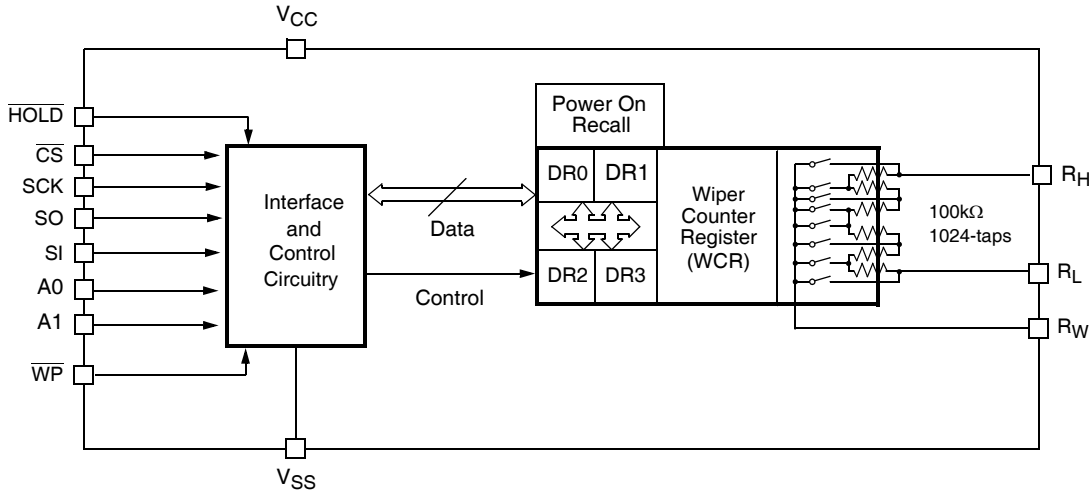
**Ordering Information**

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	POTENTIOMETER ORGANIZATION (k $\Omega$ )	TEMP RANGE (°C)	PACKAGE
X9111TV14I	X9111TV I	5 $\pm$ 10%	100	-40 to +85	14 Ld TSSOP (4.4mm)
X9111TV14IZ (Note)	X9111TV ZI			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)
X9111TV14	X9111TV			0 to +70	14 Ld TSSOP (4.4mm)
X9111TV14Z (Note)	X9111TV Z			0 to +70	14 Ld TSSOP (4.4mm) (Pb-free)
X9111TV14-2.7	X9111TV F	2.7 to 5.5		0 to +70	14 Ld TSSOP (4.4mm)
X9111TV14Z-2.7 (Note)	X9111TV ZF			0 to +70	14 Ld TSSOP (4.4mm) (Pb-free)
X9111TV14I-2.7*	X9111TV G			-40 to +85	14 Ld TSSOP (4.4mm)
X9111TV14IZ-2.7* (Note)	X9111TV ZG			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-free)

\*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Detailed Functional Diagram**



**Circuit Level Applications**

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

**System Level Applications**

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

## Pin Descriptions

PIN (TSSOP)	SYMBOL	FUNCTION
1	SO	Serial Data Output
2	A0	Device Address
3	NC	No Connect
4	$\overline{\text{CS}}$	Chip Select
5	SCK	Serial Clock
6	SI	Serial Data Input
7	V <sub>SS</sub>	System Ground
8	$\overline{\text{WP}}$	Hardware Write Protect
9	A1	Device Address
10	$\overline{\text{HOLD}}$	Device Select. Pause the Serial Bus
11	R <sub>W</sub>	Wiper Terminal of the Potentiometer
12	R <sub>H</sub>	High Terminal of the Potentiometer
13	R <sub>L</sub>	Low Terminal of the Potentiometer
14	V <sub>CC</sub>	System Supply Voltage

## Pin Descriptions

### Bus Interface Pins

#### SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### SERIAL INPUT (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

#### SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9111.

#### HOLD ( $\overline{\text{HOLD}}$ )

$\overline{\text{HOLD}}$  is used in conjunction with the  $\overline{\text{CS}}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{\text{HOLD}}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{\text{HOLD}}$  must be brought LOW while SCK is LOW. To resume communication,  $\overline{\text{HOLD}}$  is brought HIGH, again while SCK is LOW. If the pause feature is not used,  $\overline{\text{HOLD}}$  should be held HIGH at all times.

#### DEVICE ADDRESS (A<sub>0</sub>, A<sub>1</sub>)

The address inputs are used to set the 8-bit slave address. A match in the slave address serial data stream must be made with the address input (A<sub>1</sub>–A<sub>0</sub>) in order to initiate communication with the X9111.

#### CHIP SELECT ( $\overline{\text{CS}}$ )

When  $\overline{\text{CS}}$  is HIGH, the X9111 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.  $\overline{\text{CS}}$  LOW enables the X9111, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on  $\overline{\text{CS}}$  is required prior to the start of any operation.

#### HARDWARE WRITE PROTECT INPUT ( $\overline{\text{WP}}$ )

The  $\overline{\text{WP}}$  pin when LOW prevents nonvolatile writes to the Data Registers.

#### Potentiometer Pins

##### R<sub>H</sub>, R<sub>L</sub>

The R<sub>H</sub> and R<sub>L</sub> pins are equivalent to the terminal connections on a mechanical potentiometer.

##### R<sub>W</sub>

The wiper pin is equivalent to the wiper terminal of a mechanical potentiometer.

#### Bias Supply Pins

#### SYSTEM SUPPLY VOLTAGE (V<sub>CC</sub>) AND SUPPLY GROUND (V<sub>SS</sub>)

The V<sub>CC</sub> pin is the system supply voltage. The V<sub>SS</sub> pin is the system ground.

#### Other Pins

##### NO CONNECT (NC)

Pin should be left open. This pin is used for Intersil manufacturing and test purposes.

## Principles of Operation

### Device Description

#### Serial Interface

The X9111 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked-in on the rising SCK.  $\overline{\text{CS}}$  must be LOW and the  $\overline{\text{HOLD}}$  and  $\overline{\text{WP}}$  pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

#### Array Description

The X9111 is comprised of a resistor array (see Figure 1). The array contains the equivalent of 1023 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R<sub>H</sub> and R<sub>L</sub> inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R<sub>W</sub>) output. Within the individual array only one switch may be turned on at a time.

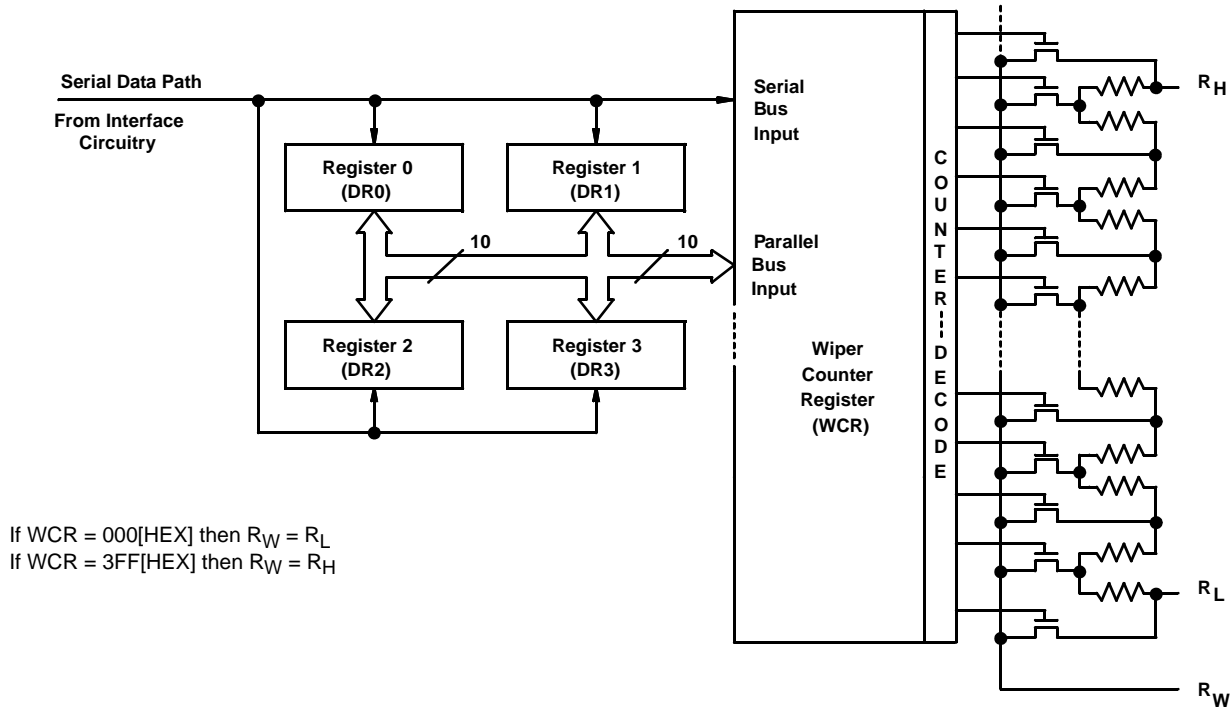


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

These switches are controlled by a Wiper Counter Register (WCR). The 10-bits of the WCR (WCR[9:0]) are decoded to select, and enable, one of 1024 switches.

### Wiper Counter Register (WCR)

The X9111 contains a Wiper Counter Register (see Table 1) for the XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 1024 switches along its resistor array. The contents of the WCR can be altered in one of three ways: (1) it may be written directly by the host via the write Wiper Counter Register instruction (serial load); (2) it may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register; (3) it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9111 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the R0 value into the WCR.

### Data Registers (DR3 to DR0)

The potentiometer has four 10-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

A DR[9:0] is used to store one of the 1024 wiper position (0 ~1023). Table 2

### Status Register (SR)

This 1-bit status register is used to store the system status (see Table 3).

WIP: Write In Progress status bit, read only.

- When WIP=1, indicates that high-voltage write cycle is in progress.
- When WIP=0, indicates that no high-voltage write cycle is in progress.

## Device Instructions

### Identification Byte (ID and A)

The first byte sent to the X9111 from the host, following a  $\overline{CS}$  going HIGH to LOW, is called the Identification Byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device ID for the X9111; this is fixed as 0101[B] (refer to Table 4).

The A1–A0 bits in the ID byte are the internal slave address. The physical device address is defined by the state of the A1–A0 input pins. The slave address is externally specified by the user. The X9111 compares the serial data stream with the address input state; a successful compare of the address

bits is required for the X9111 to successfully continue the command sequence. Only the device whose slave address matches the incoming device address sent by the master executes the instruction. The A1–A0 inputs can be actively driven by CMOS input signals or tied to V<sub>CC</sub> or V<sub>SS</sub>. The R/W bit is used to set the device to either read or write mode.

**Instruction Byte and Register Selection**

The next byte sent to the X9111 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (I[2:0]). The RB and RA bits point to one of the four registers. The format is shown in Table 5.

**TABLE 1. WIPER LATCH, WL (10-BIT), WCR9–WCR0: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE, V)**

WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V	V	V

(MSB) (LSB)

**TABLE 2. DATA REGISTER, DR (10-BIT), BIT 9–BIT 0: USED TO STORE WIPER POSITIONS OR DATA (NON-VOLATILE, NV)**

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

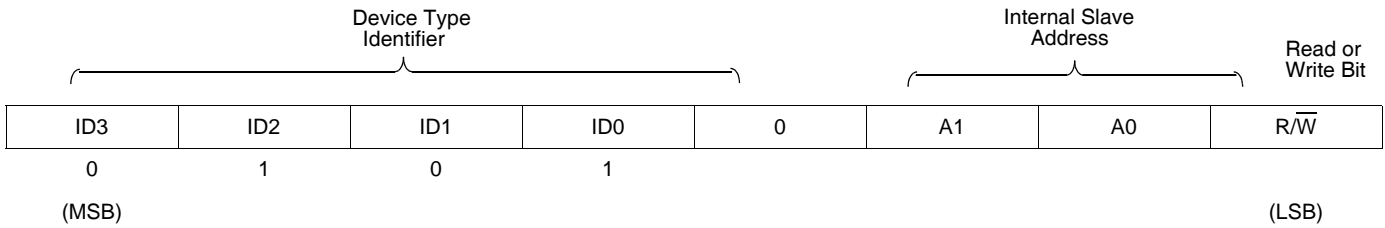
MSB LSB

**TABLE 3. STATUS REGISTER, SR (1-BIT)**

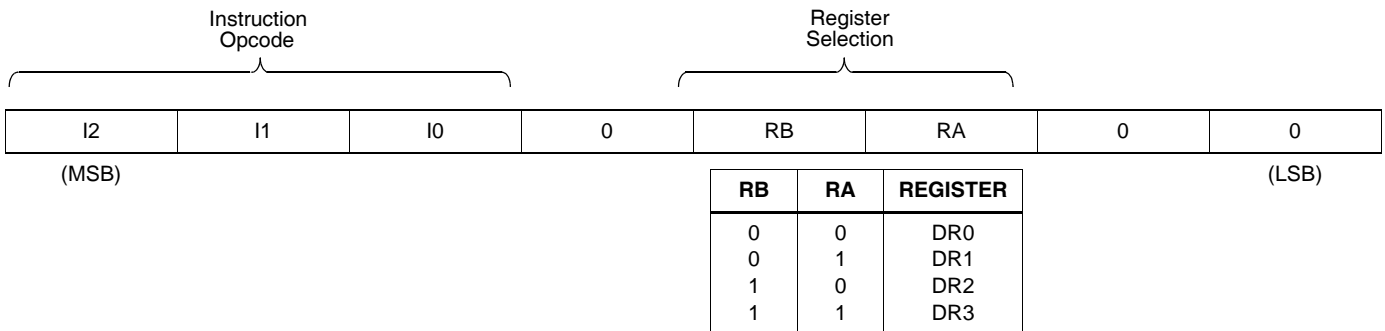
WIP
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(LSB)

**TABLE 3. IDENTIFICATION BYTE FORMAT**



**TABLE 4. INSTRUCTION BYTE FORMAT**



Five of the seven instructions are four bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected pot,
- **Write Wiper Counter Register** – change current wiper position of the selected pot,
- **Read Data Register** – read the contents of the selected data register;
- **Write Data Register** – write a new value to the selected data register.
- **Read Status** – This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The basic sequence of the four byte instructions is illustrated in Figure 3. These four-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by tWRL. A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of tWR to complete. The transfer can occur between the potentiometer and one of its associated registers. The Read Status Register instruction is the only unique format (see Figure 4).

Two instructions require a two-byte sequence to complete (see Figure 2). These instructions transfer data between the

host and the X9111; either between the host and one of the Data Registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.

See Instruction format for more details.

**Write in Process (WIP bit)**

The contents of the Data Registers are saved to nonvolatile memory when the  $\overline{CS}$  pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a Write In Process bit (WIP). The WIP bit is read with a Read Status command (see Figure 4).

**Power Up and Down Requirements**

There are no restrictions on the power-up condition of  $V_{CC}$  and the voltages applied to the potentiometer pins provided that the  $V_{CC}$  is always more positive than or equal to the voltages at  $R_H$ ,  $R_L$ , and  $R_W$ , i.e.,  $V_{CC} \geq R_H, R_L, R_W$ . There are no restrictions on the power-down condition. However, the datasheet parameters for the DCP do not apply until 1 millisecond after  $V_{CC}$  reaches its final value.

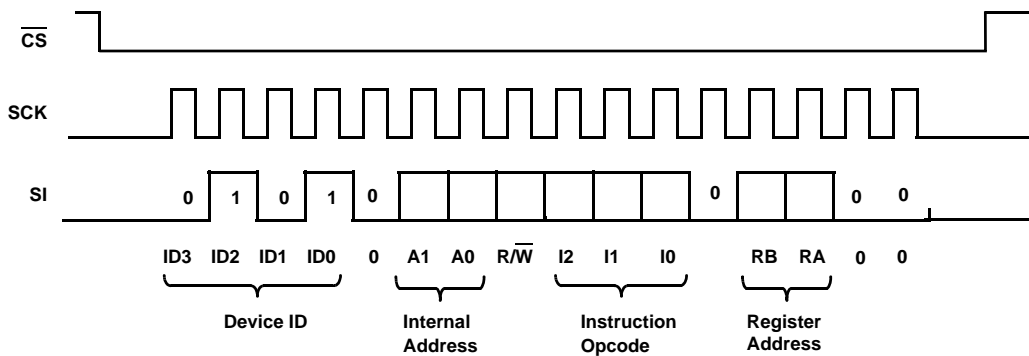


FIGURE 2. TWO-BYTE INSTRUCTION SEQUENCE

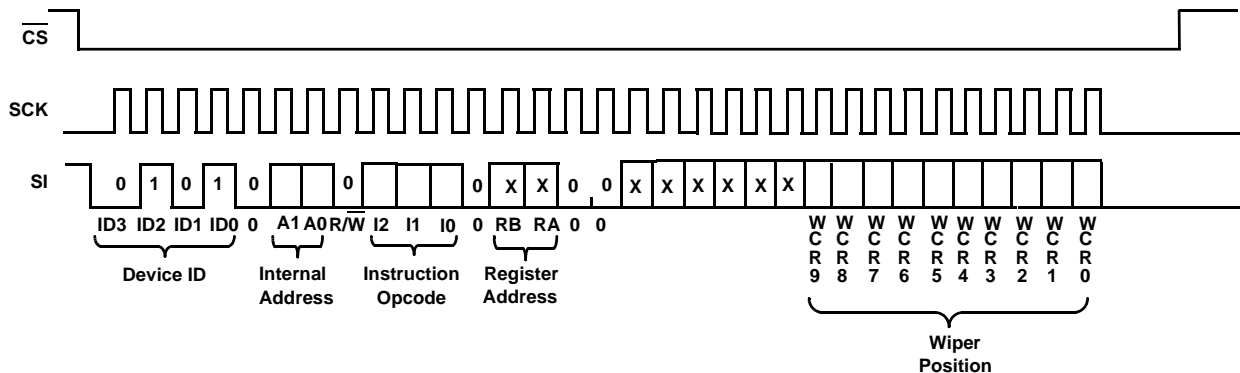


FIGURE 3. FOUR-BYTE INSTRUCTION SEQUENCE (WRITE OR READ FOR WCR OR DATA REGISTERS)



**Read Data Register (DR)**

$\overline{\text{CS}}$ Falling Edge	Device Type Identifier		Device Addresses		Instruction Opcode		Register Addresses		Wiper Position (Sent by X9111 on SO)						Wiper Position (sent by X9111 on SO)						$\overline{\text{CS}}$ Rising Edge												
	0	1	0	1	0	A1	A0	R/W = 1	1	0	1	0	RB	RA	0	0	X	X	X	X		X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
	0	1	0	1	0	A1	A0	R/W = 1	1	0	1	0	RB	RA	0	0	X	X	X	X	X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

**Write Data Register (DR)**

$\overline{\text{CS}}$ Falling Edge	Device Type Identifier		Device Addresses		Instruction Opcode		Register Addresses		Wiper Position or Data (Sent by Master on SI)						Wiper Position or Data (Sent by Master on SI)						$\overline{\text{CS}}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE											
	0	1	0	1	0	A1	A0	R/W = 0	1	1	0	0	R	R	0	0	X	X	X	X			X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1
	0	1	0	1	0	A1	A0	R/W = 0	1	1	0	0	R	R	0	0	X	X	X	X	X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

**Transfer Data Register (DR) to Wiper Counter Register (WCR)**

$\overline{\text{CS}}$ Falling Edge	Device Type Identifier		Device Addresses		Instruction Opcode		Register Addresses		$\overline{\text{CS}}$ Rising Edge								
	0	1	0	1	0	A1	A0	R/W = 1									
	0	1	0	1	0	A1	A0	R/W = 1	1	1	0	0	RB	RA	0	0	

**Transfer Wiper Counter Register (WCR) to Data Register (DR)**

$\overline{\text{CS}}$ Falling Edge	Device Type Identifier		Device Addresses		Instruction Opcode		Register Addresses		$\overline{\text{CS}}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE							
	0	1	0	1	0	A1	A0	R/W = 0									
	0	1	0	1	0	A1	A0	R/W = 0	1	1	1	0	RB	RA	0	0	

**Read Status Register (SR)**

$\overline{\text{CS}}$ Falling Edge	Device Type Identifier		Device Addresses		Instruction Opcode		Register Addresses		Status Data (Sent by Slave on SO)						Status Data (Sent by Slave on SO)						$\overline{\text{CS}}$ Rising Edge															
	0	1	0	1	0	A1	A0	R/W = 1	0	1	0	0	0	0	0	1	X	X	X	X		X	X	X	X	0	0	0	0	0	0	0	WI	P		
	0	1	0	1	0	A1	A0	R/W = 1	0	1	0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	WI	P	

NOTES:

1. "A0 and A1": stand for the device address sent by the master.
2. WCRx refers to wiper position data in the Wiper Counter Register
3. "X": Don't Care.



**Absolute Maximum Ratings**

Temperature under bias . . . . . -65°C to +135°C  
 Storage temperature . . . . . -65°C to +150°C  
 Voltage on SCK any address input  
 with respect to V<sub>SS</sub> . . . . . -1V to +7V  
 $\Delta V = | (V_H - V_L) |$  . . . . . 0V to V<sub>CC</sub>  
 Lead temperature (soldering, 10s) . . . . . +300°C  
 I<sub>W</sub> (10s) . . . . . ±6mA

**Recommended Operating Conditions**

Temperature Range  
 Commercial . . . . . 0°C to +70°C  
 Industrial . . . . . -40°C to +85°C  
 Supply Voltage (V<sub>CC</sub>) Limits  
 X9111 . . . . . .5V±10%  
 X9111-2.7 . . . . . 2.7V to 5.5V

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**Analog Characteristics** Over recommended industrial operation conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
R <sub>TOTAL</sub>	End to End Resistance			100		kΩ
	End to End Resistance Tolerance				±20	%
	Power Rating	+25°C, each pot			50	mW
I <sub>W</sub>	Wiper Current				±3	mA
R <sub>W</sub>	Wiper Resistance	Wiper Current = ±50μA, V <sub>CC</sub> = 5V		40	110	Ω
		Wiper Current = ±50μA, V <sub>CC</sub> = 3V		150	300	Ω
V <sub>TERM</sub>	Voltage on any R <sub>H</sub> or R <sub>L</sub> Pin	V <sub>SS</sub> = 0V	V <sub>SS</sub>		V <sub>CC</sub>	V
	Noise	Ref: 1V		-120		dBV
	Resolution			1.6		%
	Absolute Linearity (Note 1)	R <sub>w(n)(actual)</sub> - R <sub>w(n)(expected)</sub> , where n = 8 to 1006			±1	MI (Note 3)
		R <sub>w(n)(actual)</sub> - R <sub>w(n)(expected)</sub> (Note 4)		±1.5	±2.0	MI (Note 3)
	Relative Linearity (Note 2)	R <sub>w(m+1)</sub> - [R <sub>w(m)</sub> + MI], where m = 8 to 1006			±0.5	MI (Note 3)
		R <sub>w(m+1)</sub> - [R <sub>w(m)</sub> + MI] (Note 4)		±0.5	±1.0	MI (Note 3)
	Temperature Coefficient of R <sub>TOTAL</sub>			±300		ppm/°C
	Ratiometric Temp. Coefficient				20	ppm/°C
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>	Potentiometer Capacitancies	See Macro model		10/10/25		pF

**NOTES:**

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
2. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
3. MI = RTOT/1023 or (R<sub>H</sub> - R<sub>L</sub>)/1023, single pot
4. n = 0, 1, 2, ..., 1023; m = 0, 1, 2, ..., 1022.
5. ESD Rating on RH, RL, RW pins is 1.5kV (HBM, 1.0μA leakage maximum), ESD rating on all other pins is 2.0kV.

**D.C. Operating Characteristics** Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
I <sub>CC1</sub>	V <sub>CC</sub> supply current (active)	f <sub>SCK</sub> = 2.5 MHz, SO = Open, V <sub>CC</sub> = 5.5V Other Inputs = V <sub>SS</sub>			400	μA
I <sub>CC2</sub>	V <sub>CC</sub> supply current (nonvolatile write)	f <sub>SCK</sub> = 2.5MHz, SO = Open, V <sub>CC</sub> = 5.5V Other Inputs = V <sub>SS</sub>		1	5	mA
I <sub>SB</sub>	V <sub>CC</sub> current (standby)	SCK = SI = V <sub>SS</sub> , Addr. = V <sub>SS</sub> , CS = V <sub>CC</sub> = 5.5V			3	μA
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>			10	μA
V <sub>IH</sub>	Input HIGH voltage		V <sub>CC</sub> × 0.7		V <sub>CC</sub> + 1	V
V <sub>IL</sub>	Input LOW voltage		-1		V <sub>CC</sub> × 0.3	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 3mA			0.4	V
V <sub>OL</sub>	Output LOW voltage	I <sub>OH</sub> = -1mA, V <sub>CC</sub> ≥ +3V	V <sub>CC</sub> - 0.8			V
V <sub>OL</sub>	Output LOW voltage	I <sub>OH</sub> = -0.4mA, V <sub>CC</sub> ≤ +3V	V <sub>CC</sub> - 0.4			V

**Endurance And Data Retention**

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	years

**Capacitance**

SYMBOL	TEST	TEST CONDITIONS	MAX	UNITS
C <sub>IN/OUT</sub> (Note 6)	Input/Output capacitance (SI)	V <sub>OUT</sub> = 0V	8	pF
C <sub>OUT</sub> (Note 6)	Output capacitance (SO)	V <sub>OUT</sub> = 0V	8	pF
C <sub>IN</sub> (Note 6)	Input capacitance (A0, CS, WP, HOLD, and SCK)	V <sub>IN</sub> = 0V	6	pF

**Power-Up Timing**

SYMBOL	PARAMETER	MIN	MAX	UNITS
t <sub>r</sub> V <sub>CC</sub> (Note 6)	V <sub>CC</sub> power-up rate	0.2	50	V/ms
t <sub>PUR</sub> (Note 7)	Power-up to initiation of read operation		1	ms
t <sub>PWU</sub> (Note 7)	Power-up to initiation of write operation		50	ms

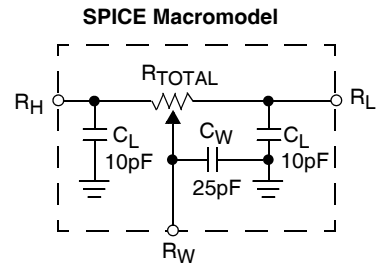
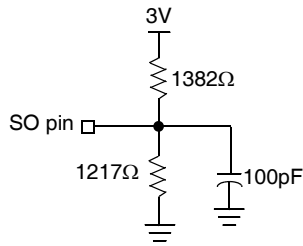
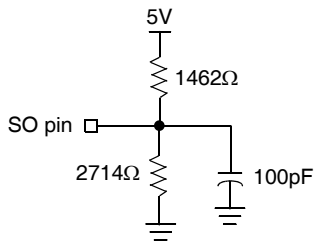
NOTES:

- This parameter is not 100% tested.
- t<sub>PUR</sub> and t<sub>PWU</sub> are the delays required from the time the (last) power supply (V<sub>CC</sub>) is stable until the specific instruction can be issued. These parameters are not 100% tested.

**A.C. Test Conditions**

Input pulse levels	V <sub>CC</sub> × 0.1 to V <sub>CC</sub> × 0.9
Input rise and fall times	10ns
Input and output timing level	V <sub>CC</sub> × 0.5

**Equivalent A.C. Load Circuit**



**AC Timing**

SYMBOL	PARAMETER	MIN	MAX	UNITS
f <sub>SCK</sub>	SSI/SPI clock frequency		2.0	MHz
t <sub>CYC</sub>	SSI/SPI clock cycle time	400		ns
t <sub>WH</sub>	SSI/SPI clock high time	150		ns
t <sub>WL</sub>	SSI/SPI clock low time	150		ns
t <sub>LEAD</sub>	Lead time	150		ns
t <sub>LAG</sub>	Lag time	150		ns
t <sub>SU</sub>	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input setup time	50		ns
t <sub>H</sub>	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input hold time	50		ns
t <sub>RI</sub>	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input rise time		50	ns
t <sub>FI</sub>	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input fall time		50	ns
t <sub>DIS</sub>	SO output disable time	0	500	ns
t <sub>V</sub>	SO output valid time		100	ns
t <sub>HO</sub>	SO output hold time	0		ns
t <sub>RO</sub>	SO output rise time		50	ns
t <sub>FO</sub>	SO output fall time		50	ns
t <sub>HOLD</sub>	$\overline{\text{HOLD}}$ time	400		ns
t <sub>HSU</sub>	$\overline{\text{HOLD}}$ setup time	50		ns
t <sub>HH</sub>	$\overline{\text{HOLD}}$ hold time	50		ns
t <sub>HZ</sub>	$\overline{\text{HOLD}}$ low to output in high Z		100	ns
t <sub>LZ</sub>	$\overline{\text{HOLD}}$ high to output in low Z		100	ns
T <sub>I</sub>	Noise suppression time constant at SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ inputs		20	ns
t <sub>CS</sub>	$\overline{\text{CS}}$ deselect time	100		ns
t <sub>WPASU</sub>	$\overline{\text{WP}}$ , A0, A1 setup time	0		ns
t <sub>WPAH</sub>	$\overline{\text{WP}}$ , A0, A1 hold time	0		ns

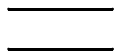


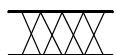

**High-voltage Write Cycle Timing**

SYMBOL	PARAMETER	TYP	MAX	UNITS
$t_{WR}$	High-voltage write cycle time (store instructions)	5	10	ms

**XDCP Timing**

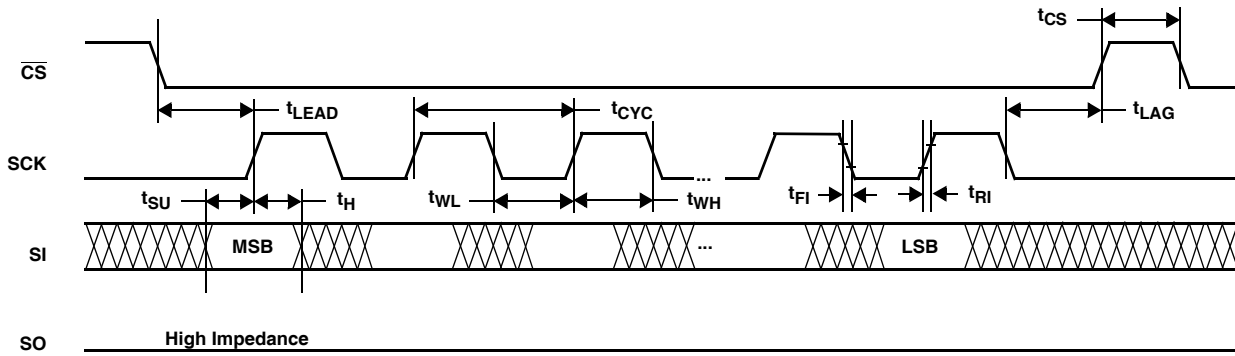
SYMBOL	PARAMETER	MIN	MAX	UNITS
$t_{WRPO}$	Wiper response time after the third (last) power supply is stable	5	10	$\mu$ s
$t_{WRL}$	Wiper response time after instruction issued (all load instructions)	5	10	$\mu$ s

**Symbol Table**

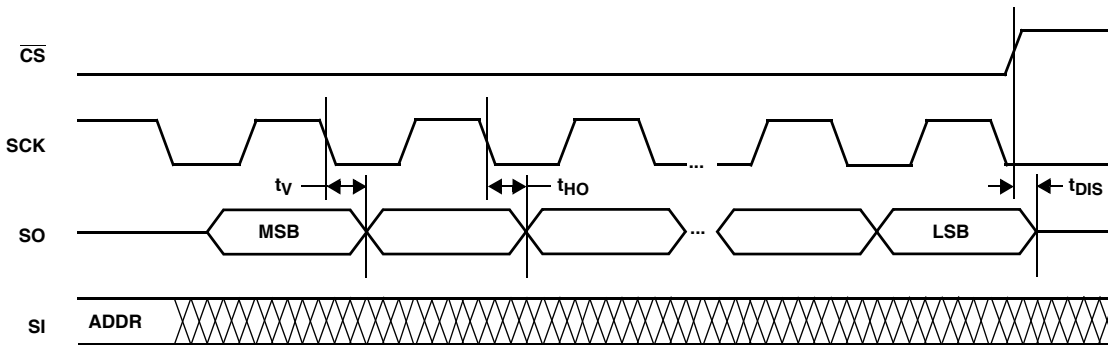
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

## Timing Diagrams

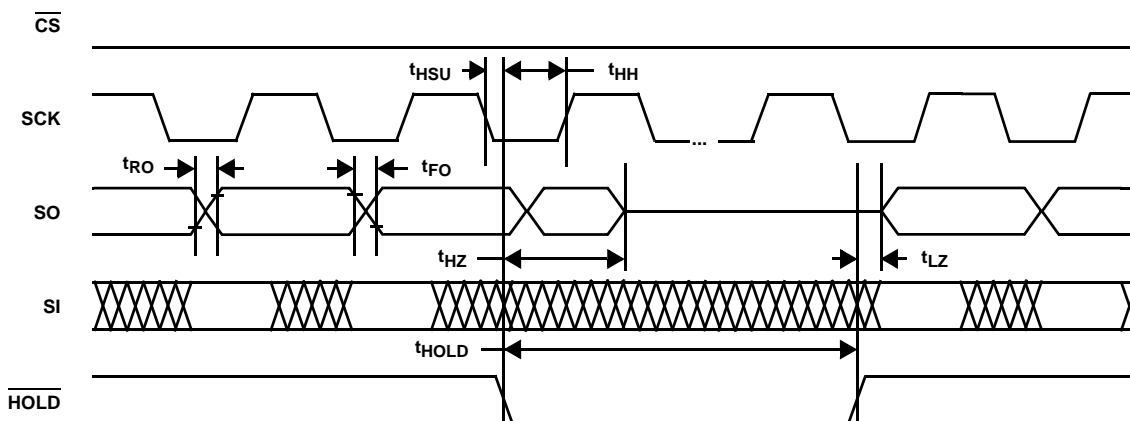
### Input Timing



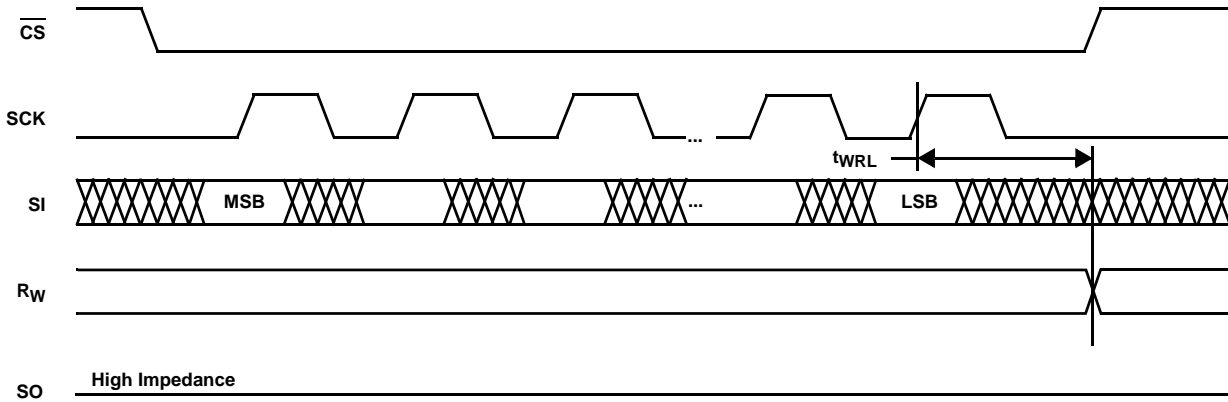
### Output Timing



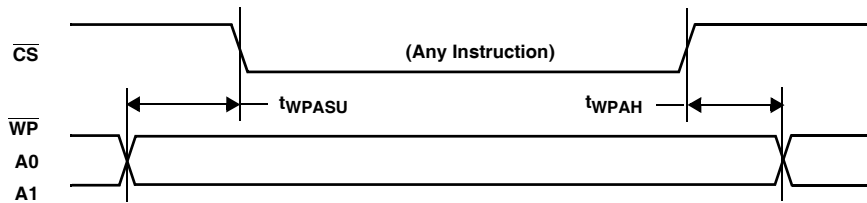
### Hold Timing



**XDCP Timing (for All Load Instructions)**

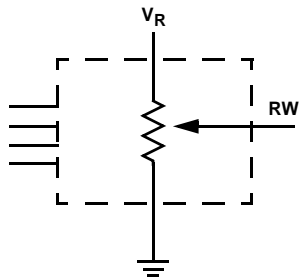


**Write Protect and Device Address Pins Timing**

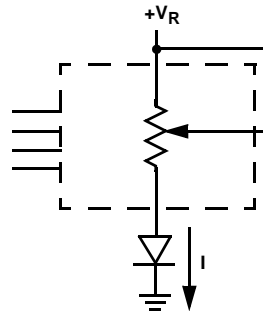


**Applications information**

**Basic Configurations of Electronic Potentiometers**



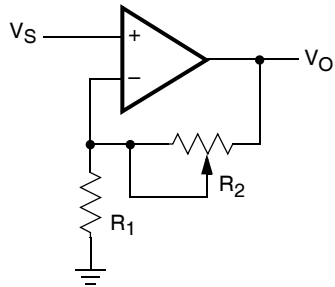
Three terminal Potentiometer;  
Variable voltage divider



Two terminal Variable Resistor;  
Variable current

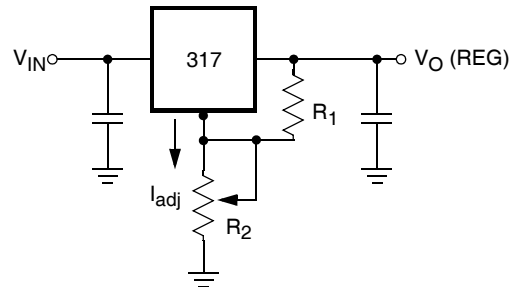
Application Circuits

Noninverting Amplifier



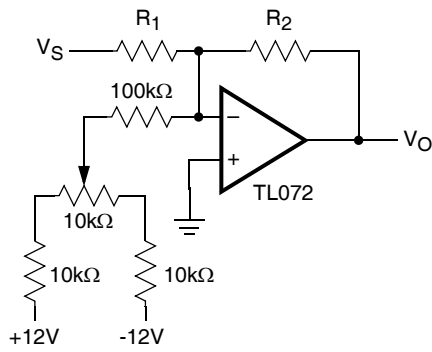
$$V_O = (1 + R_2/R_1)V_S$$

Voltage Regulator

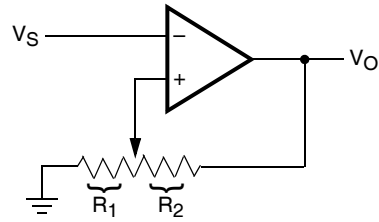


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

Offset Voltage Adjustment



Comparator with Hysteresis

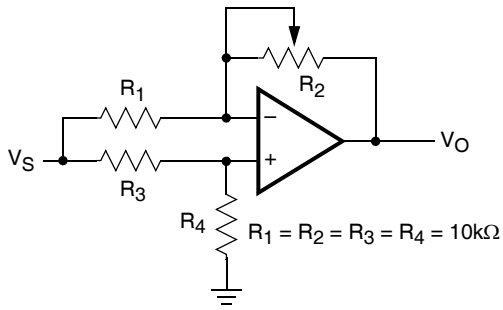


$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(\text{max})$$

$$V_{LL} = \{R_1/(R_1 + R_2)\} V_O(\text{min})$$

Application Circuits (Continued)

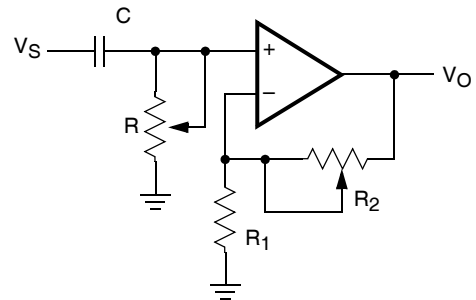
Attenuator



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

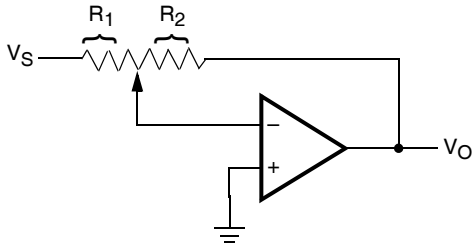
Filter



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

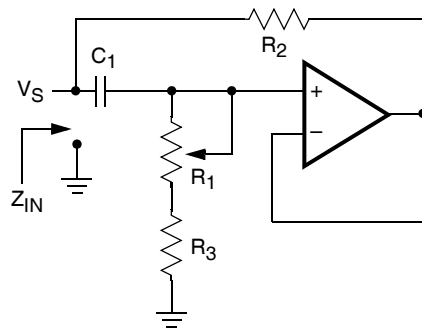
Inverting Amplifier



$$V_O = G V_S$$

$$G = -R_2/R_1$$

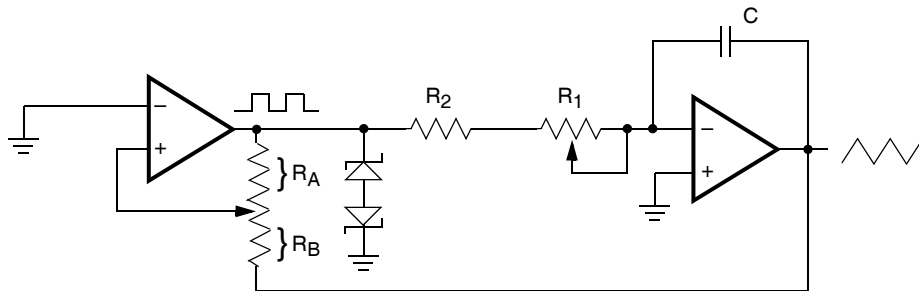
Equivalent L-R Circuit



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) \quad C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

Function Generator

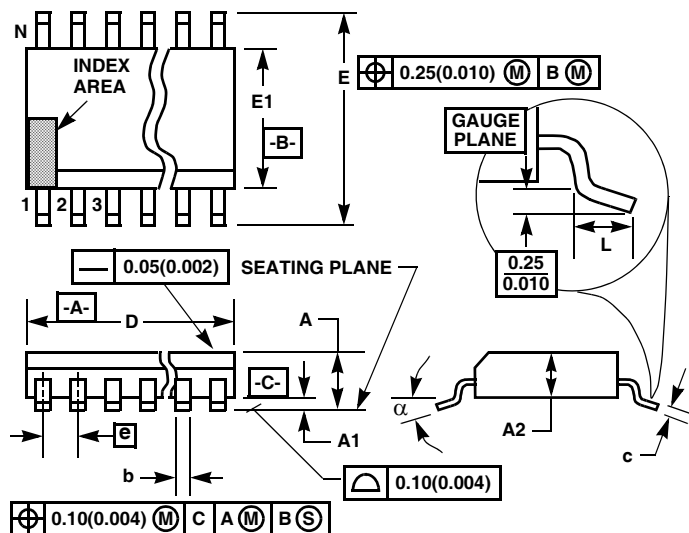


$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$



## Thin Shrink Small Outline Plastic Packages (TSSOP)



## NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

**M14.173**  
**14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
$\alpha$	0°	8°	0°	8°	-

Rev. 2 4/06

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