WM8591

24-bit, 192kHz Stereo CODEC

DESCRIPTION

The WM8591 is a high performance, stereo audio CODEC with single-ended inputs and differential outputs. It is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

The stereo 24-bit multi-bit sigma delta ADC has programmable gain with limiting control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

A stereo multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz.

The WM8591 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I^2S, left justified, right justified and DSP formats.

The device is controlled in software via a 2-wire serial interface which provides access to all features including volume controls, mutes, and de-emphasis facilities. The device is available in a 28-lead SSOP package.

FEATURES

- Audio Performance
  - 110dB SNR ('A' weighted @ 48kHz) DAC
  - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Stereo ADC input analogue gain adjust from +24dB to –21dB in 0.5dB steps
- ADC digital gain from -21.5dB to -103dB in 0.5dB steps
- Programmable Limiter on ADC input.
- Stereo DAC with differential analogue line outputs.
- 2-wire Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- 4.5V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation
- 28-lead SSOP Package

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

BLOCK DIAGRAM

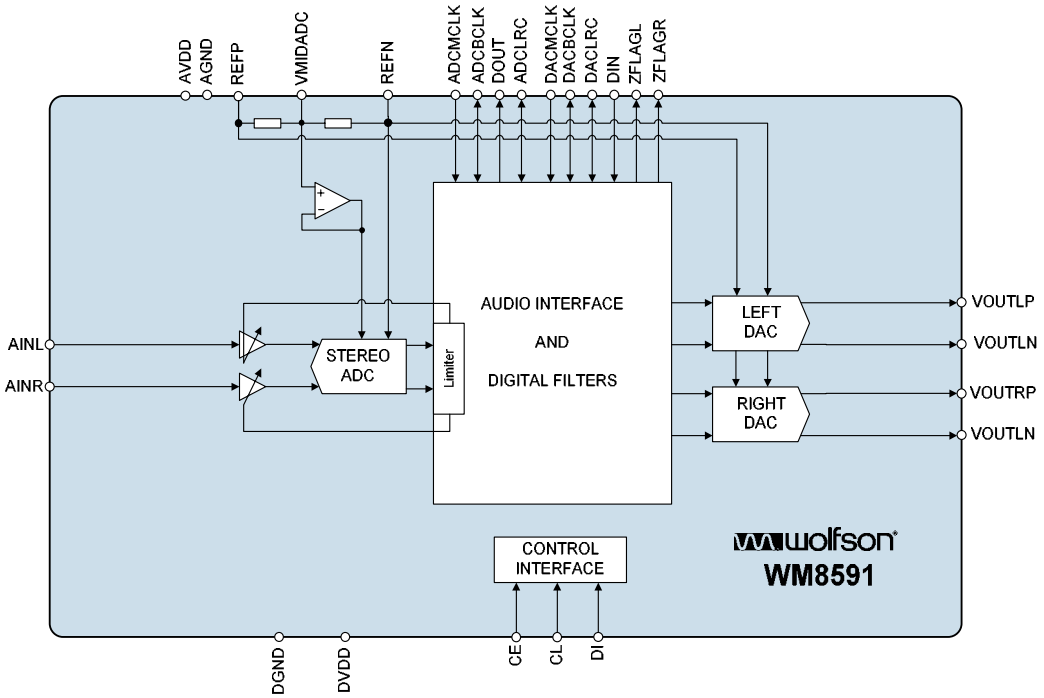
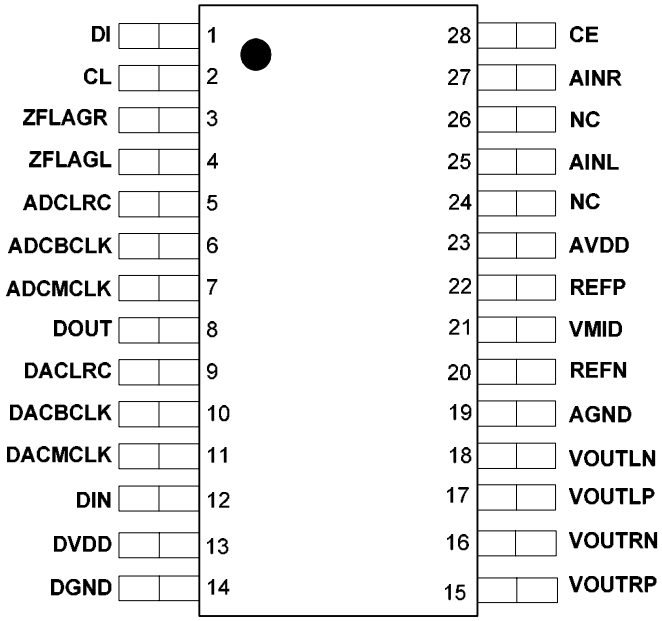


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8591GEDS/V	-25 to +85°C	28-lead SSOP (Pb-free)	MSL2	260°C
WM8591GEDS/RV	-25 to +85°C	28-lead SSOP (Pb-free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DI	Digital Input	Serial interface data
2	CL	Digital Input	Serial interface clock
3	ZFLAGR	Digital Output (open drain)	Right channel zero flag output (external pull-up required)
4	ZFLAGL	Digital Output (open drain)	Left channel zero flag output (external pull-up required)
5	ADCLRC	Digital Input/Output	ADC left/right word clock
6	ADCBCLK	Digital Input/Output	ADC audio interface bit clock
7	ADCMCLK	Digital Input	Master ADC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
8	DOUT	Digital Output	ADC data output
9	DACLRC	Digital Input/Output	DAC left/right word clock
10	DACBCLK	Digital Input/Output	DAC audio interface bit clock
11	DACMCLK	Digital Input	Master DAC clock; 256, 384, 512, 768fs or 1152fs (fs = word clock frequency)
12	DIN	Digital Input	DAC data input
13	DVDD	Supply	Digital positive supply
14	DGND	Supply	Digital negative supply
15	VOUTRP	Analogue Output	DAC right channel positive output
16	VOUTRN	Analogue Output	DAC right channel negative output
17	VOUTLP	Analogue Output	DAC left channel positive output
18	VOUTLN	Analogue Output	DAC left channel negative output
19	AGND	Supply	Analogue negative supply and substrate connection
20	REFN	Analogue Input	Negative reference input
21	VMID	Analogue Output	Midrail divider decoupling pin; must be externally decoupled
22	REFP	Analogue Input	Positive reference input
23	AVDD	Supply	Analogue positive supply
24	NC		No Connection
25	AINL	Analogue Input	Left channel input
26	NC		No Connection
27	AINR	Analogue Input	Right channel input
28	CE	Digital Input	2-wire address select

Notes:

1. Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage, DVDD	-0.3V	+4.5V
Analogue supply voltage, AVDD	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7	3.3	3.6	V
Analogue supply range	AVDD, DACREFP		4.5	5	5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Notes:

1. Digital supply DVDD must never be more than 0.3V greater than AVDD in normal operation.
2. It is possible to hold the device in reset with AVDD=0V and DVDD=3.3V.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}=1mA	0.9 x DVDD			V
Digital Input Leakage Current				0.9		µA
Digital Input Leakage Capacitance				5		pF
Analogue Reference Levels						
Reference voltage	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50		kΩ
DAC Performance (Load = 10kΩ, 50pF)						
0dBFs Full scale output voltage				2.0 x AVDD/5		Vrms
SNR (Note 1,2)	SNR	A-weighted, @ fs = 48kHz	105	110		dB
SNR (Note 1,2)	SNR	A-weighted @ fs = 96kHz		109		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input	105	110		dB
Total Harmonic Distortion	THD	1kHz, 0dBFs		-97	-90	dB
DAC channel separation				130		dB
Channel Level Matching		1kHz signal		0.1		dB
Channel Phase Deviation		1kHz signal		0.04		Degree
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		Vrms
SNR (Note 1,2)	SNR	A-weighted, 0dB gain @ fs = 48kHz ADCMCLK2DAC=1	93	102		dB
SNR (Note 1,2)	SNR	A-weighted, 0dB gain @ fs = 96kHz 64 x OSR ADCMCLK2DAC=1		99		dB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

Dynamic Range (note 2)	DNR	A-weighted, -60dB full scale input	93	102		dB
Total Harmonic Distortion	THD	1kHz, -3dBFs		-95	-85	dB
ADC Channel Separation		1kHz Input		85		dB
Channel Level Matching		1kHz signal		0.1		dB
Channel Phase Deviation		1kHz signal		0.06		Degree
Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Mute Attenuation (Note 4)		1kHz Input, 0dB gain		97		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		59		dB
		20Hz to 20kHz 100mVpp		56		dB
Input Resistance		PGA Gain = +24dB		4.5		kΩ
		PGA Gain = 0dB		37.4		kΩ
		PGA Gain = -21dB		69.0		kΩ
Input Capacitance				1		pF
Supply Current						
Analogue supply current		AVDD = 5V		60		mA
Digital supply current		DVDD = 3.3V		6		mA
Analogue Powerdown Current		AVDD = 5V		132		µA
Digital Powerdown Current		DVDD = 3.3V		2.7		µA
Crosstalk						
DAC to ADC		1kHz signal, ADC fs = 48kHz, DAC fs = 44.1kHz		115		dB
		20kHz signal, ADC fs = 48kHz, DAC fs = 44.1kHz		130		dB
ADC to DAC		1kHz signal, ADC fs = 48kHz, DAC fs = 44.1kHz		131		dB
		20kHz signal, ADC fs = 48kHz, DAC fs = 44.1kHz		138		dB

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements obtained with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. All performance measurements obtained using certain timings conditions (ADCLRC and DACLRC should be synchronous with MCLK). Please refer to section 'Digital Audio Interface'.
4. A better MUTE Attenuation can be achieved if the ADC gain is set to minimum.
5. All performance measurements specified for ADC and DAC operating in isolation.

TERMINOLOGY

1. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) – DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD (dB) – THD is a ratio, of the rms values, of Distortion/Signal.
4. Stop band attenuation (dB) – Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple – Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

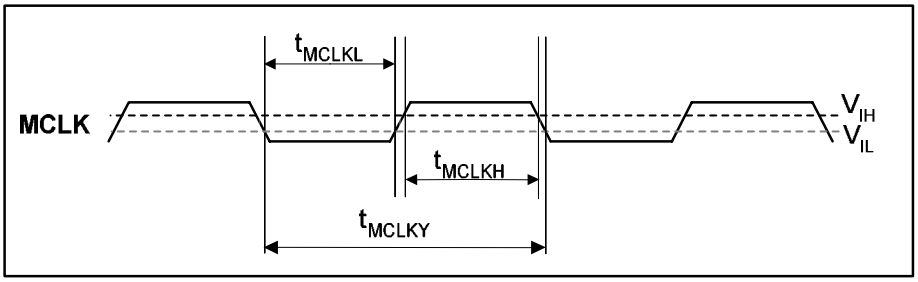


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
ADC/DACMCLK System clock pulse width high	t_{MCLKH}		11			ns
ADC/DACMCLK System clock pulse width low	t_{MCLKL}		11			ns
ADC/DACMCLK System clock cycle time	t_{MCLKY}		27			ns
ADC/DACMCLK Duty cycle			40:60		60:40	

Table 1 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

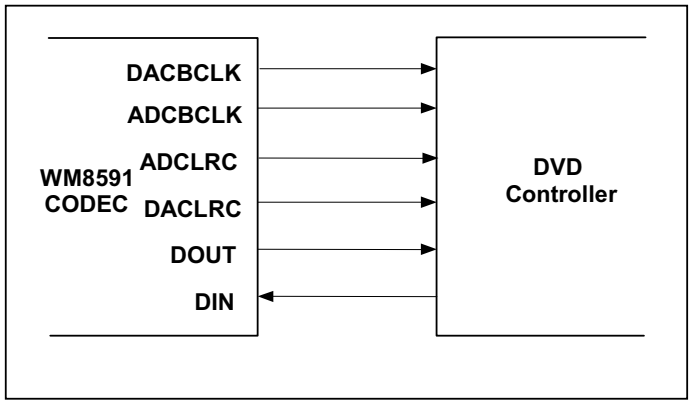


Figure 2 Audio Interface – Master Mode

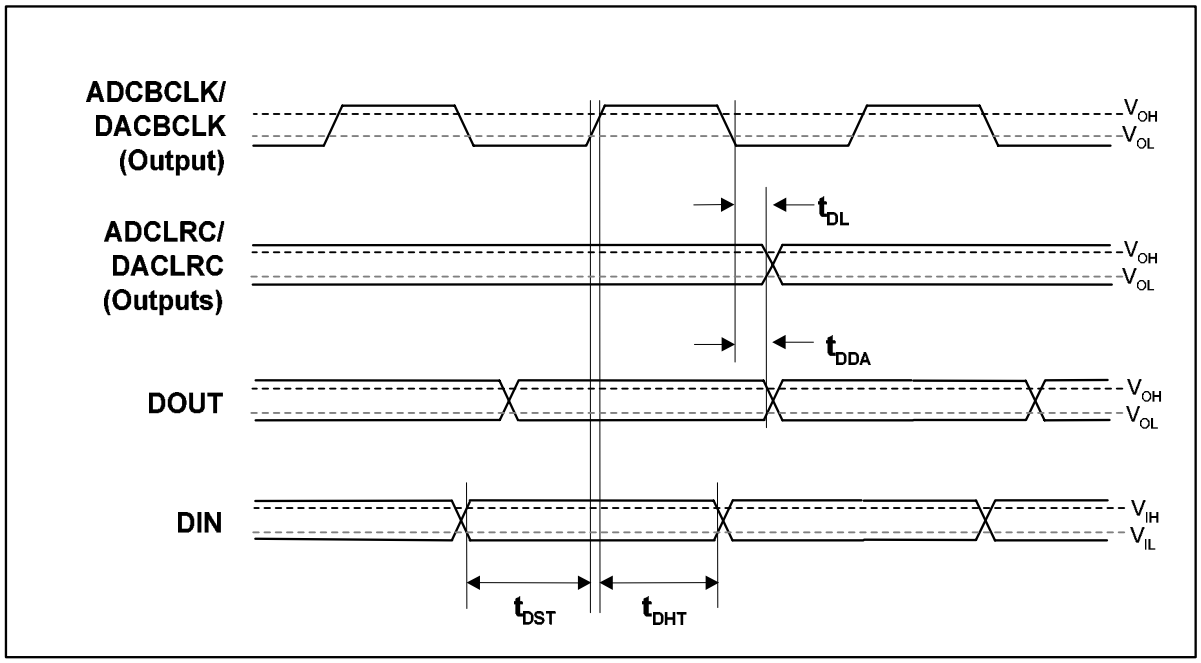


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, ADC/DACMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADC/DACLRC propagation delay from ADC/DACBCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from ADCBCLK falling edge	t_{DDA}		0		10	ns
DIN setup time to DACBCLK rising edge	t_{DST}		10			ns
DIN hold time from DACBCLK rising edge	t_{DHT}		10			ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

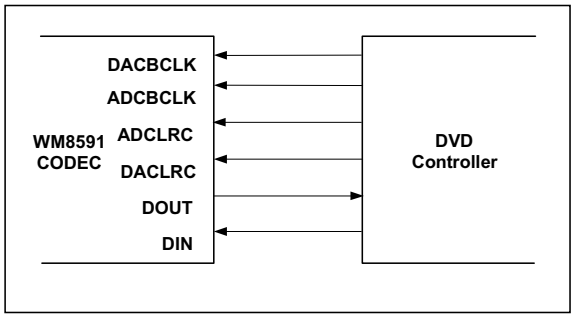


Figure 4 Audio Interface – Slave Mode

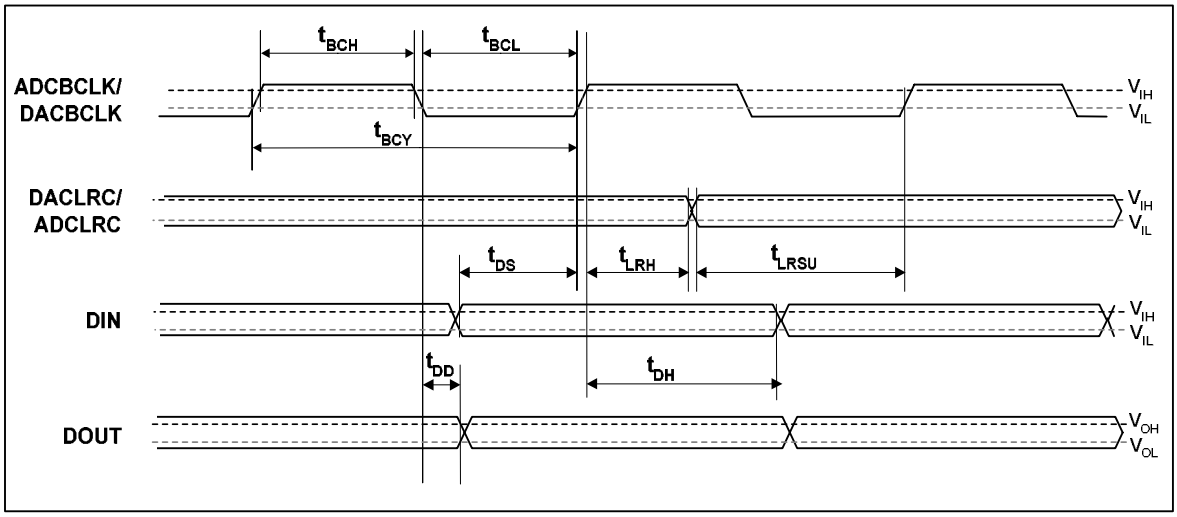


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADC/DACMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADC/DACBCLK cycle time	t_{BCY}		50			ns
ADC/DACBCLK pulse width high	t_{BCH}		20			ns
ADC/DACBCLK pulse width low	t_{BCL}		20			ns
DACLRC/ADCLRC set-up time to ADC/DACBCLK rising edge	t_{LRSU}		10			ns
DACLRC/ADCLRC hold time from ADC/DACBCLK rising edge	t_{LRH}		10			ns
DIN set-up time to DACBCLK rising edge	t_{DS}		10			ns
DIN hold time from DACBCLK rising edge	t_{DH}		10			ns
DOUT propagation delay from ADCBCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

Note:

ADCLRC and DACLRC should be synchronous with MCLK, although the WM8591 interface is tolerant of phase variations or jitter on these signals.

CONTROL INTERFACE TIMING – 2-WIRE SERIALCONTROL

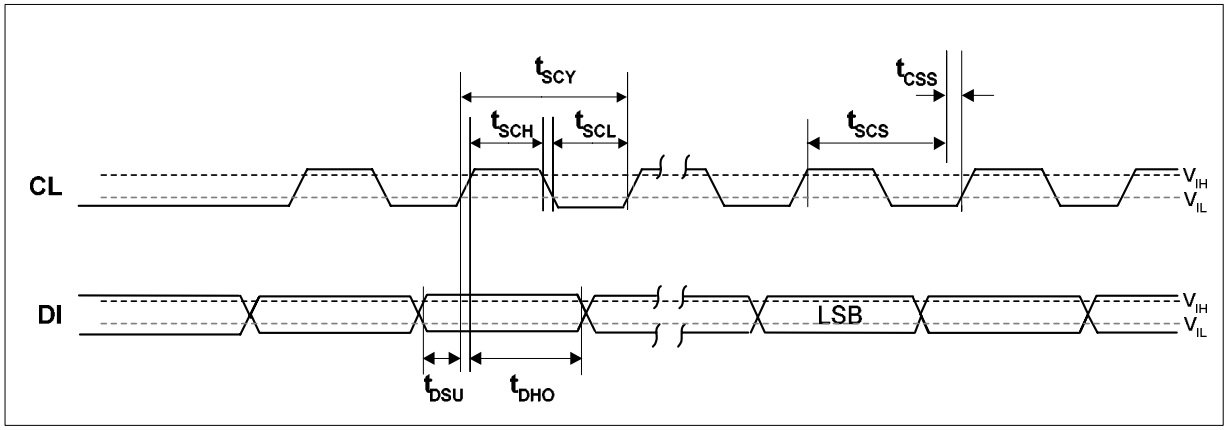


Figure 6 Control Interface Timing – 2-Wire Serial Control Mode (MODE=0)

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CL Frequency		0		526	kHz
CL Low Pulse-Width	t_1	1.3			us
CL High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
DI, CL Rise Time	t_6			300	ns
DI, CL Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

Table 4 2-wire Control Interface Timing Information

DEVICE DESCRIPTION

INTRODUCTION

WM8591 is a complete differential 2-channel DAC, single-ended 2-channel ADC audio CODEC, including digital interpolation and decimation filters, multi-bit sigma delta stereo ADC, and switched capacitor multi-bit sigma delta DACs with output smoothing filters. It is available in a single package and controlled by a 2-wire serial interface.

The DAC and ADC have separate left/right clocks, bit clocks, master clocks and data I/Os. The Audio Interfaces may be independently configured to operate in either master or slave mode. In Slave mode ADCLRC, DACLRC, ADCBCLK and DACBCLK are all inputs. In Master mode ADCLRC, DACLRC, ADCBCLK and DACBCLK are outputs, and clock signals should not be driven into these pins by external circuitry. The ADC audio interface defaults to master mode, and the DAC audio interface defaults to slave mode.

The ADC has an analogue input PGA and a digital gain control, accessed by one register write. The input PGA allows input signals to be gained up to +24dB and attenuated down to -21dB in 0.5dB steps. The digital gain control allows attenuation from -21.5dB to -103dB in 0.5dB steps. This allows the user maximum flexibility in the use of the ADC.

The DAC has its own digital volume control, which is adjustable between 0dB and -127.5dB in 0.5dB steps. In addition a zero cross detect circuit is provided for digital volume controls. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

Control of internal functionality of the device is by 2-wire serial control interface. The interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

Operation using system clock of 128fs, 192fs, 256fs, 384fs, 512fs, 768fs or 1152fs (DAC only) is provided. ADC and DAC may run at different rates. Master clock sample rates (fs) from 32kHz up to 192kHz are allowed, provided the appropriate system clock is input.

The audio data interface supports right, left and I^2S interface formats along with a highly flexible DSP serial port interface.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The WM8591 uses separate master clocks for the ADC and DAC. The external master system clocks can be applied directly through the ADCMCLK and DACMCLK input pins with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC and DAC.

In Slave mode the WM8591 has a master detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error the interface is disabled and maintains the output level at the last sample. The master clock must be synchronised with ADCLRC/DACLRC, although the WM8591 is tolerant of phase variations or jitter on this clock.

The ADC supports system clock to sampling clock ratios of 256fs to 768fs. The DACs support ratios of 256fs to 1152fs when the DAC signal processing of the WM8591 is programmed to operate at 128 times oversampling rate (DACOSR=0). The DACs support system clock to sampling clock ratios of 128fs and 192fs when the WM8591 is programmed to operate at 64 times oversampling rate (DACOSR=1).

The ADC signal processing in the WM8591 can operate at either 128 times oversampling rate (ADCOSR=0) or 64 times oversampling rate (ADCOSR=1). It is recommended that ADCOSR is set to 1 for ADC operation at 96kHz.

Table 5 shows the typical system clock frequencies for ADC operation at both 128 times oversampling rate (ADCOSR=0) and 64 times oversampling rate (ADCOSR=1), and DAC operation at 128 times oversampling rate (DACOSR=0). Table 6 shows typical system clock frequencies for DAC operation at 64 times oversampling rate (DACOSR =1).

SAMPLING RATE (ADCLRC/ DACLRC)	System Clock Frequency (MHz)				
	256fs	384fs	512fs	768fs	1152fs (DAC only)
32kHz	8.192	12.288	16.384	24.576	36.864
44.1kHz	11.2896	16.9340	22.5792	33.8688	Unavailable
48kHz	12.288	18.432	24.576	36.864	Unavailable
96kHz	24.576	36.864	Unavailable	Unavailable	Unavailable

Table 5 ADC and DAC System Clock Frequencies Versus Sampling Rate (ADC operation at either 128 times oversampling rate (ADCOSR=0) or 64 times oversampling rate (ADCOSR=1), DAC operation at 128 times oversampling rate, DACOSR=0)

SAMPLING RATE (DACLRC)	System Clock Frequency (MHz)	
	128fs	192fs
96kHz	12.288	18.432
192kHz	24.576	36.864

Table 6 DAC System Clock Frequencies Versus Sampling Rate at 64 Times Oversampling Rate (DACOSR=1)

In Master mode DACBCLK, ADCBCLK, DACLRC and ADCLRC are generated by the WM8591, and these pins should not be driven by external circuitry. The frequencies of ADCLRC and DACLRC are set by setting the required ratio of DACMCLK to DACLRC and ADCMCLK to ADCLRC using the DACRATE and ADCRATE control bits (Table 7).

ADCRATE[2:0]/ DACRATE[2:0]	ADCMCLK/DACMCLK: ADCLRC/DACLRC RATIO
000	128fs (DAC Only)
001	192fs (DAC Only)
010	256fs
011	384fs
100	512fs
101	768fs

Table 7 Master Mode MCLK: ADCLRC/DACLRC Ratio Select

Table 8 shows the settings for ADCRATE and DACRATE for common sample rates and ADCMCLK/DACMCLK frequencies.

SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	DACRATE =000	DACRATE =001	ADCRATE/ DACRATE =010	ADCRATE/ DACRATE =011	ADCRATE/ DACRATE =100	ADCRATE/ DACRATE =101
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 8 Master Mode ADC/DACLRC Frequency Selection

ADCBCLK and DACBCLK are also generated by the WM8591. The frequency of ADCBCLK and DACBCLK can be set in software.

BCLK can be set to MCLK/4, 64fs or 128fs. If DSP mode is selected as the audio interface mode then BCLK can be set to MCLK, 64fs or 128fs. Note that DSP mode cannot be used in 128fs mode for word lengths greater than 16 bits or in 192fs mode for word lengths greater than 24 bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R28 (1Ch) 0011100 ADC/DAC Synchronization	3:2	BCLK_RATE	00	Sets ADCBCLK and DACBCLK rate in master mode	
				BCLK_RATE	**BCLK Output Frequency**
				00	MCLK/4 (MCLK in DSP Mode)
				01	MCLK/4 (MCLK in DSP Mode)
				10	64fs
				11	128fs

ZERO DETECT

The WM8591 has a zero detect circuit for each DAC channel, which detects when 1024 consecutive zero samples have been input. The two zero flag outputs (ZFLAGL and ZFLAGR) may be programmed to output the zero detect signals (see Table 9) that may then be used to control external muting circuits. The ZFLAGL and ZFLAGR pins require a pull-up resistor to be connected (see external components diagram). The ZFLAGL and ZFLAGR pads will pull low to indicate that the zero condition has been detected.

The polarity of the zero flag signals can be changed by setting the ZFLAGPOL bit. When this bit is set, the ZFLAGL and ZFLAGR pins will pull low when the zero condition is not found and will go to high impedance when the zero condition is detected.

The zero detect may also be used to automatically enable the mute by setting IZD. The zero flag output may be disabled by setting DZFM to 00.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R9 (09h) 0001001 DAC Mute	2:1	DZFM	10	ZFLAG decode		
				DZFM	**ZFLAGL**	**ZFLAGR**
				00	Zero flag disabled	Zero flag disabled
				01	Left channel zero	Right channel zero
				10	Both channel zero	Both channel zero
				11	Either channels zero	Either channel zero
	4	ZFLAGPOL	0	ZFLAG polarity		
				ZFLAGPOL	**ZFLAGL**	**ZFLAGR**
				0	Pin pulls low to indicate zero conidition, high impedance otherwise	
				1	Pin is high impedance when zero condition detected, pulls low otherwise	

Table 9 Zero Flag Control

POWERDOWN MODES

The WM8591 has powerdown control bits allowing specific parts of the WM8591 to be powered off when not being used. Control bit ADCPD powers off the ADC. The stereo DAC has a separate powerdown control bit, DACPD allowing the DAC to be powered off when not in use.

Setting ADCPD and DACPD will powerdown everything except the references VMID, REFN and REFP. Setting PDWN will override all other powerdown control bits. It is recommended that ADCPD and DACPD are set before setting PDWN. The default is for all blocks to be enabled.

INTERNAL POWER ON RESET CIRCUIT

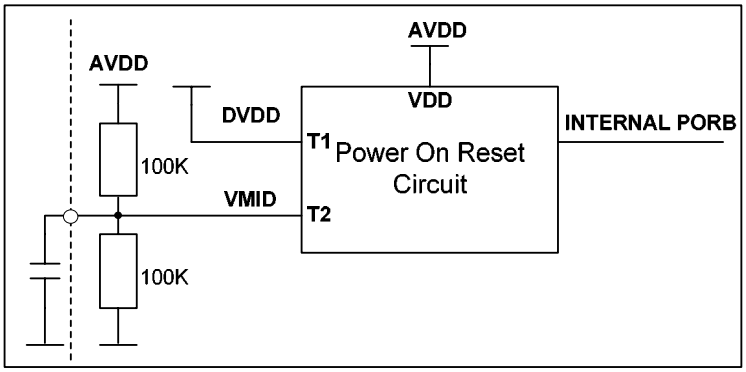


Figure 7 Internal Power on Reset Circuit Schematic

The WM8591 includes an internal Power On Reset Circuit which is used reset the digital logic into a default state after power up.

Figure 7 shows a schematic of the internal POR circuit. The POR circuit is powered from AVDD. The circuit monitors DVDD and VMID and asserts PORB low if DVDD or VMID are below the minimum threshold Vpor_off.

On power up, the POR circuit requires AVDD to be present to operate. PORB is asserted low until AVDD and DVDD and VMID are established. When AVDD, DVDD, and VMID have been established, PORB is released high, all registers are in their default state and writes to the digital interface may take place.

On power down, PORB is asserted low whenever DVDD or VMID drop below the minimum threshold Vpor_off.

If AVDD is removed at any time, the internal Power On Reset circuit is powered down and PORB will follow AVDD.

In most applications the time required for the device to release PORB high will be determined by the charge time of the VMID node.

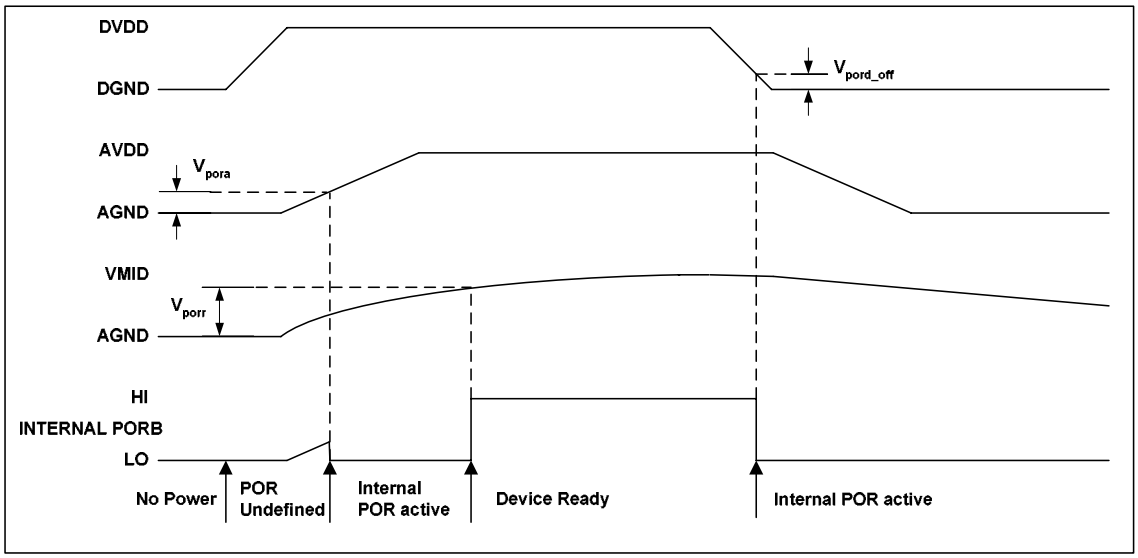


Figure 8 Typical Power up Sequence where DVDD is Powered before AVDD

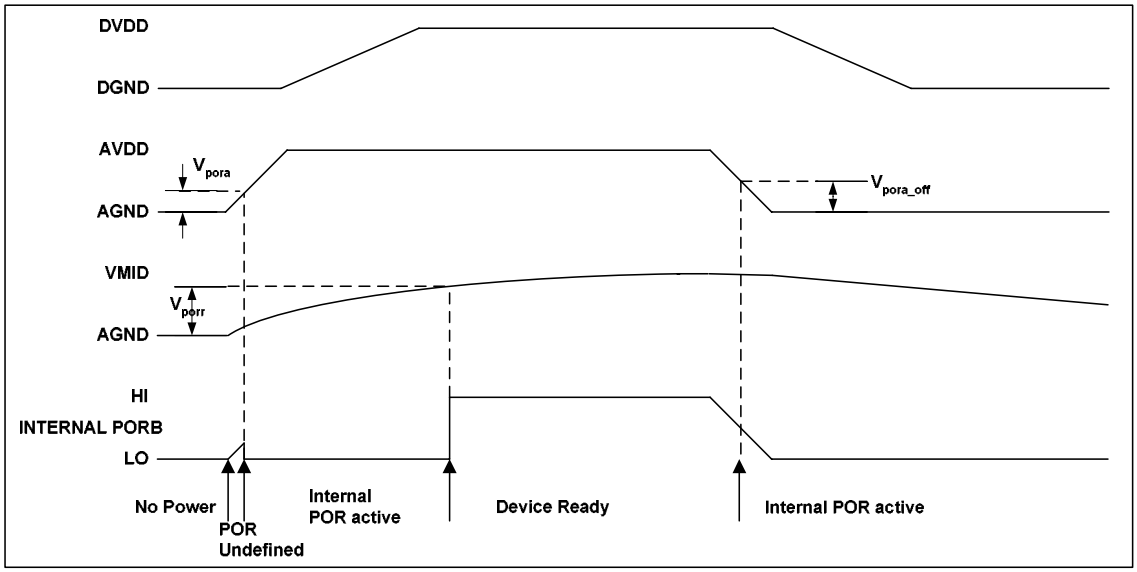


Figure 9 Typical Power up Sequence where AVDD is Powered before DVDD

Typical POR Operation (typical values, not tested)

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.5	0.7	1.0	V
V_{porr}	0.5	0.7	1.1	V
V_{pora_off}	1.0	1.4	2.0	V
V_{pord_off}	0.6	0.8	1.0	V

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. Using the POR circuit to monitor VMID ensures a reasonable delay between applying power to the device and Device Ready.

Figure 8 and Figure 9 show typical power up scenarios in a real system. Both AVDD and DVDD must be established and VMID must have reached the threshold Vporr before the device is ready and can be written to. Any writes to the device before Device Ready will be ignored.

Figure 8 shows DVDD powering up before AVDD. Figure 9 shows AVDD powering up before DVDD. In both cases, the time from applying power to Device Ready is dominated by the charge time of VMID.

A 10uF cap is recommended for decoupling on VMID. The charge time for VMID will dominate the time required for the device to become ready after power is applied. The time required for VMID to reach the threshold is a function of the VMID resistor string and the decoupling capacitor. The Resistor string has an typical equivalent resistance of 50kohm (+/-20%). Assuming a 10uF capacitor, the time required for VMID to reach threshold of 1V is approx 110ms.

DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes DIN is always an input to the WM8591 and DOUT is always an output. The default for the DAC is Slave mode, and the default for the ADC is Master mode.

In Slave mode (MS=0) ADCLRC, DACLRC, ADCBCLK and DACBCLK are inputs to the WM8591 (Figure 10). DIN and DACLRC are sampled by the WM8591 on the rising edge of DACBCLK, ADCLRC is sampled on the rising edge of ADCBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK. By setting control bits ADCBCP or DACBCP the polarity of ADCBCLK and DACBCLK may be reversed so that DIN and DACLRC are sampled on the falling edge of DACBCLK, ADCLRC is sampled on the falling edge of ADCBCLK and DOUT changes on the rising edge of ADCBCLK.

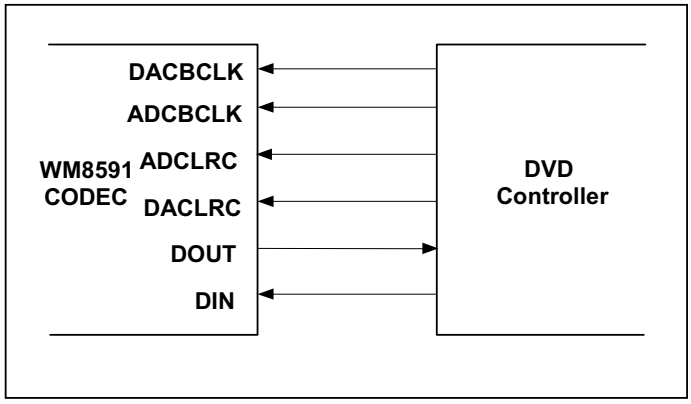


Figure 10 Slave Mode

In Master mode (MS=1) ADCLRC, DACLRC, ADCBCLK and DACBCLK are outputs from the WM8591 (Figure 11), and these pins should not be driven by external circuitry. ADCLRC, DACLRC, ADCBCLK and DACBCLK are generated by the WM8591. DIN is sampled by the WM8591 on the rising edge of DACBCLK so the controller must output DAC data that changes on the falling edge of DACBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK. By setting control bits ADCBCP and DACBCP, the polarity of ADCBCLK and DACBCLK may be reversed so that DIN is sampled on the falling edge of DACBCLK and DOUT changes on the rising edge of ADCBCLK.

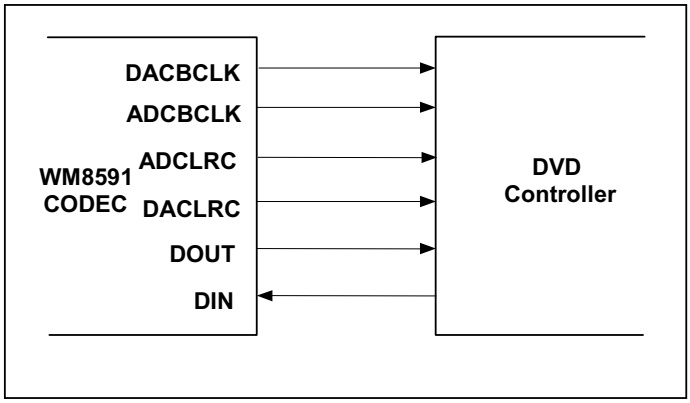


Figure 11 Master Mode

AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters or output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified Mode
- Right Justified Mode
- I^2S Mode
- DSP Mode A
- DSP Mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I^2S modes, the digital audio interface receives DAC data on the DIN input and outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with ADCLRC/DACLRC indicating whether the left or right channel is present. ADCLRC/DACLRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I^2S modes; the minimum number of BCLKs per DACLRC/ADCLRC period is 2 times the selected word length. ADCLRC/DACLRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on ADCLRC/DACLRC is acceptable provided the above requirements are met.

In DSP Mode A or Mode B, DACLRC is used as a frame sync signal to identify the MSB of the first word. The minimum number of DACBCLKs per DACLRC period is 2 times the selected word length. Any mark to space ratio is acceptable on DACLRC provided the rising edge is correctly positioned. The ADC data may also be output in DSP Mode A or Mode B, with ADCLRC used as a frame sync to identify the MSB of the first word. The minimum number of ADCBCLKs per ADCLRC period is 2 times the selected word length.

LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN is sampled by the WM8591 on the first rising edge of DACBCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the same falling edge of ADCBCLK as ADCLRC and may be sampled on the rising edge of ADCBCLK. ADCLRC and DACLRC are high during the left samples and low during the right samples (Figure 12).

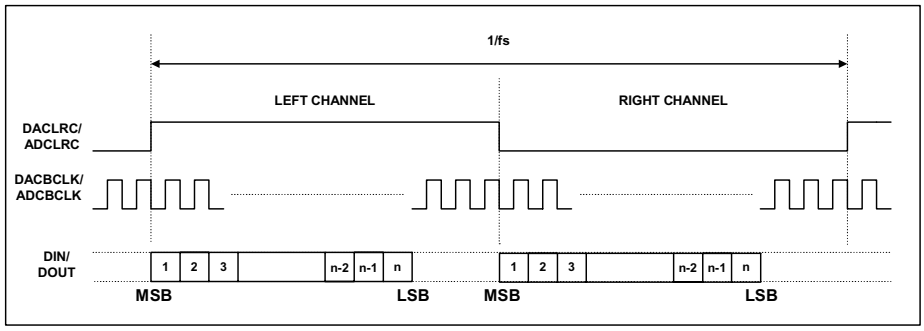


Figure 12 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN is sampled by the WM8591 on the rising edge of DACBCLK preceding a DACLRC transition. The LSB of the ADC data is output on DOUT and changes on the falling edge of ADCBCLK preceding a ADCLRC transition and may be sampled on the rising edge of ADCBCLK. ADCLRC and DACLRC are high during the left samples and low during the right samples (Figure 13).

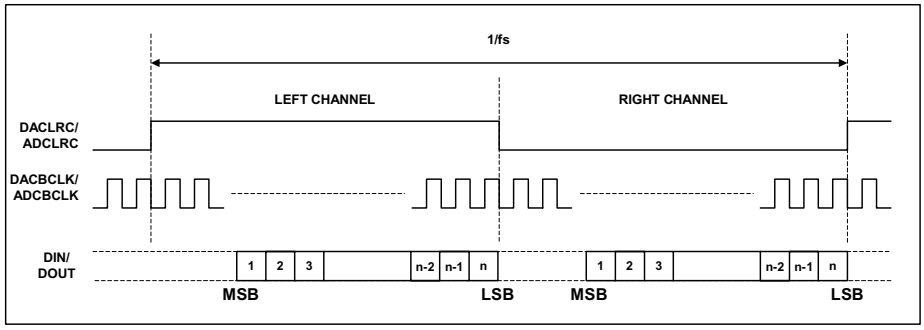


Figure 13 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB of DIN is sampled by the WM8591 on the second rising edge of DACBCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the first falling edge of ADCBCLK following an ADCLRC transition and may be sampled on the rising edge of ADCBCLK. ADCLRC and DACLRC are low during the left samples and high during the right samples.

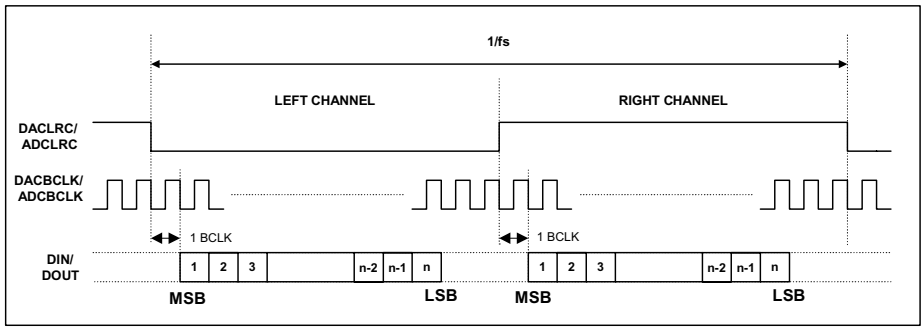


Figure 14 I²S Mode Timing Diagram

DSP MODES

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 15 and Figure 16. In device slave mode, Figure 17 and Figure 18, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

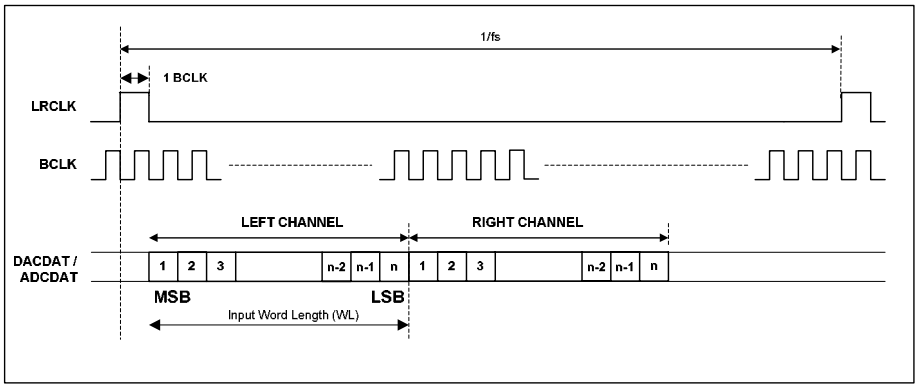


Figure 15 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

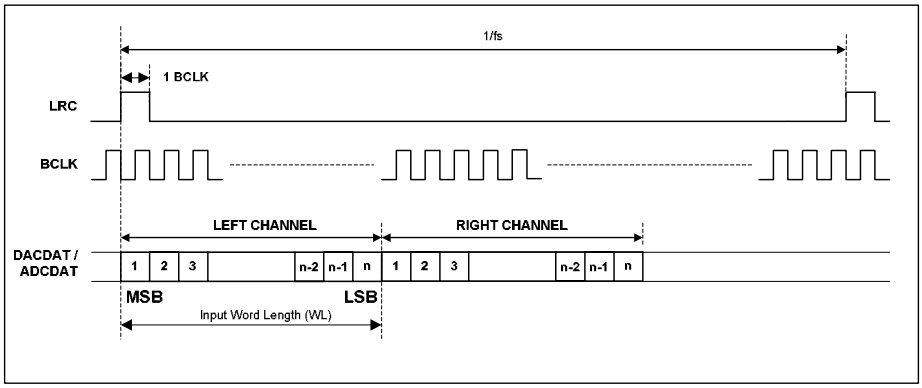


Figure 16 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

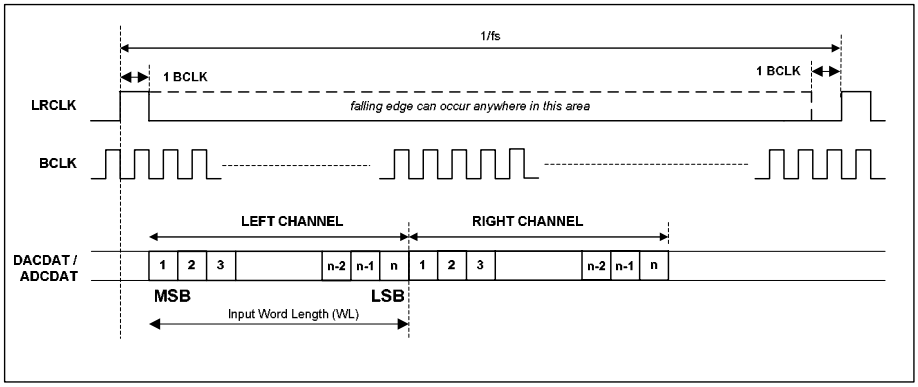


Figure 17 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

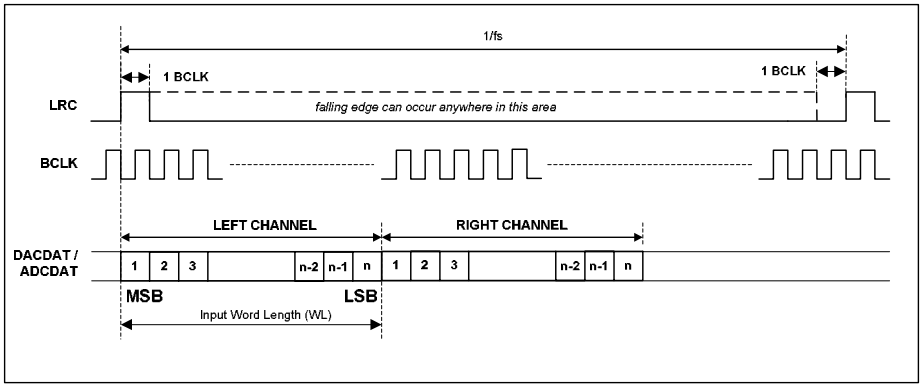


Figure 18 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

CONTROL INTERFACE OPERATION

The WM8591 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 bits in each control register. The control interface operates as a 2-wire MPU interface.

2-WIRE SERIAL CONTROL

The WM8591 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8591).

The controller indicates the start of data transfer with a high to low transition on DI while CL remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on DI (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8591 and the R/W bit is '0', indicating a write, then the WM8591 responds by pulling DI low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8591 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8591 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8591 register address plus the first bit of register data). The WM8591 then acknowledges the first data byte by pulling DI low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8591 acknowledges again by pulling DI low.

The transfer of data is complete when there is a low to high transition on DI while CL is high. After receiving a complete address and data sequence the WM8591 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. DI changes while CL is high), the device jumps to the idle condition.

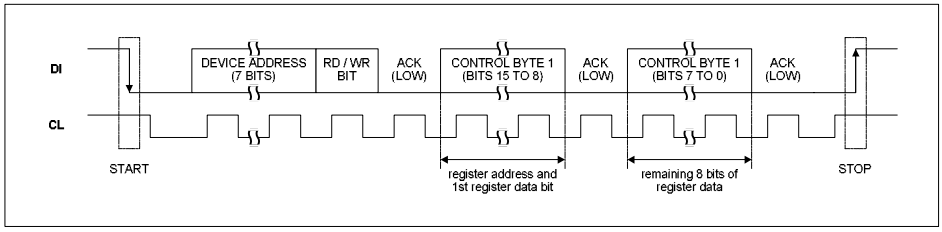


Figure 19 2-wire Serial Interface

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

The WM8591 has two possible device addresses, which can be selected using the CE pin.

CE STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

Table 10 2-Wire MPU Interface Address Selection

CONTROL INTERFACE REGISTERS

DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the FMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	1:0	DACFMT [1:0]	01	Interface format Select 00 : right justified mode 01: left justified mode 10: I^2S mode 11: DSP mode A or B (selected by DACLRP and ADCLRP)
R11 (0Bh) 0001011 ADC Interface Control	1:0	ADCFMT [1:0]	01	

In left justified, right justified or I^2S modes, the LRP register bit controls the polarity of ADCLRC/DACLRC. If this bit is set high, the expected polarity of ADCLRC/DACLRC will be the opposite of that shown Figure 12, Figure 13, etc. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the LRP register bit is used to select between early and late modes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	2	DACLRP	0	In left/right/ I^2S modes: ADCLRC/DACLRC Polarity (normal) 0 : normal ADCLRC/DACLRC polarity 1: inverted ADCLRC/DACLRC polarity In DSP mode: 0 : DSP mode A 1: DSP mode B
R11 (0Bh) 0001011 ADC Interface Control	2	ADCLRP	0	

By default, ADCLRC, DACLRC and DIN are sampled on the rising edge of ADCBCLK and DACBCLK and should ideally change on the falling edge. Data sources that change ADCLRC/DACLRC and DIN on the rising edge of ADCBCLK/DACBCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figure 12, Figure 13, etc.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	3	DACBCP	0	BCLK Polarity (DSP modes) 0 : normal BCLK polarity 1: inverted BCLK polarity
R11 (0Bh) 0001011 ADC Interface Control	3	ADCBCP	0	

The WL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	5:4	DACWL [1:0]	10	Word Length 00 : 16 bit data 01: 20 bit data 10: 24 bit data 11: 32 bit data
R11 (0Bh) 0001011 ADC Interface Control	5:4	ADCWL [1:0]	10	

Note: If 32-bit mode is selected in right justified mode, the WM8591 defaults to 24 bits.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8591 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

Note: In 24 bit I^2S mode, any width of 24 bits or less is supported provided that ADCLRC/DACLRC is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

A number of options are available to control how data from the Digital Audio Interface is applied to the DAC.

MASTER MODES

Control bit ADCMS selects between audio interface Master and Slave Modes for ADC. In ADC Master mode ADCLRC and ADCBCLK are outputs and are generated by the WM8591. In Slave mode ADCLRC and ADCBCLK are inputs to WM8591.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 Interface Control	8	ADCMS	1	Audio Interface Master/Slave Mode select for ADC: 0 : Slave Mode 1: Master Mode

Control bit DACMS selects between audio interface Master and Slave Modes for the DAC. In DAC Master mode DACLRC and DACBCLK are outputs and are generated by the WM8591. In Slave mode DACLRC and DACBCLK are inputs to WM8591.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 Interface Control	7	DACMS	0	Audio Interface Master/Slave Mode select for DAC: 0 : Slave Mode 1: Master Mode

MASTER MODE ADCLRC/DACLRC FREQUENCY SELECT

In ADC Master mode the WM8591 generates ADCLRC and ADCBCLK, in DAC master mode the WM8591 generates DACLRC and DACBCLK. These clocks are derived from the master clock (ADCMCLK or DACMCLK). The ratios of ADCMCLK to ADCLRC and DACMCLK to DACLRC are set by ADCRATE and DACRATE respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 ADCLRC and DACLRC Frequency Select	2:0	ADCRATE[2:0]	010	Master Mode MCLK:ADCLRC Ratio Select: 010: 256fs 011: 384fs 100: 512fs 101: 768fs
	6:4	DACRATE[2:0]	010	Master Mode MCLK:DACLRC Ratio Select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs 101: 768fs

ADC OVERSAMPLING RATE SELECT

For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs. Operation is explained further in Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 ADC Oversampling Rate	3	ADCOSR	0	ADC Oversampling Rate Select 0: 128x oversampling 1: 64x oversampling

DAC OVERSAMPLING RATE SELECT

Control bit DACOSR allows the user to select the DAC internal signal processing oversampling rate. Operation is described in Table 5 and Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Oversampling Rate	8	DACOSR	0	DAC Oversampling Rate Select 0: 128x oversampling 1: 64x oversampling

MUTE MODES

Setting MUTE for the DAC will apply a 'soft' mute to the input of the digital filters of the channel muted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) 0001001 DAC Mute	3	DMUTE	0	DAC Soft Mute Select 0 : Normal Operation 1: Soft mute enabled

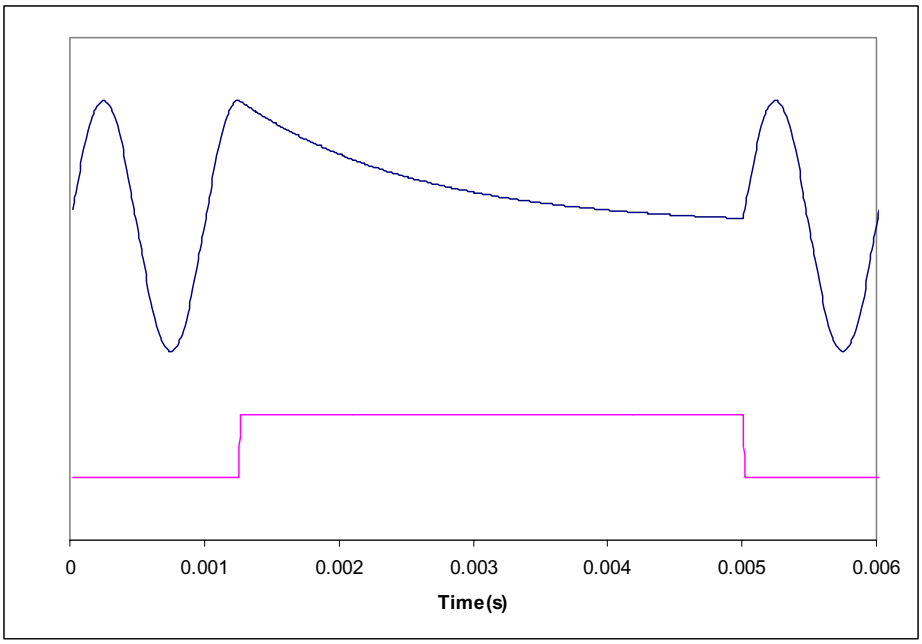


Figure 20 Application and Release of Soft Mute

Figure 20 shows the application and release of DMUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When DMUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. If DMUTE is applied to both channels for 1024 or more input samples the DAC will be muted if IZD is set. When DMUTE is de-asserted, the output will restart immediately from the current input sample.

Note that all other means of muting the DAC: setting the PL[3:0] bits to 0, setting the PDWN bit or setting attenuation to 0 will cause much more abrupt muting of the output.

ADC MUTE

Each ADC channel also has an individual mute control bit, which mutes the input to the ADC PGA. By setting the LRBOTH bit (reg22, bit 8) both channels can be muted simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) 0010101 ADC Mute Left	1	MUTELA	0	ADC Mute Select 0 : Normal Operation 1: mute ADC left
R21 (15h) 0001111 ADC Mute Right	0	MUTERA	0	ADC Mute Select 0 : Normal Operation 1: mute ADC right

DE-EMPHASIS MODE

The De-emphasis filter for the DAC is enabled under the control of DEEMP.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) 0001001 DAC De-emphasis Control	0	DEEMPH	0	De-emphasis Mode Select: 0 : Normal Mode 1: De-emphasis Mode

Refer to Figure 30, Figure 31, Figure 32, Figure 33, Figure 34 and Figure 35 for details of the De-Emphasis modes at different sample rates.

POWERDOWN MODE AND ADC/DAC DISABLE

Setting the PDWN register bit immediately powers down the WM8591, including the references, overriding all other powerdown control bits. All trace of the previous input samples is removed, but all control register settings are preserved. When PDWN is cleared, the digital filters will be re-initialised. It is recommended that the buffer, ADC and DAC are powered down before setting PDWN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 (0Dh) 0001101 Powerdown Control	0	PDWN	0	Power Down Mode Select: 0 : Normal Mode 1: Power Down Mode

The ADC and DAC may also be powered down by setting the ADCPD and DACPD disable bits. Setting ADCPD will disable the ADC and select a low power mode. The ADC digital filters will be reset and will reinitialise when ADCPD is reset. The DAC has a separate disable DACPD. Setting DACPD will disable the DAC, mixer and output PGAs. Resetting DACPD will reinitialise the digital filters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 (0Dh) 0001101 Powerdown Control	1	ADCPD	0	ADC Powerdown: 0 : Normal Mode 1: Power Down Mode
	2	DACPD	0	DAC Powerdown: 0 : Normal Mode 1: Power Down Mode

DIGITAL ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) 0000111 DAC Channel Control	1	ATC	0	Attenuator Control Mode: 0 : Right channel use Right attenuation 1: Right Channel use Left Attenuation

INFINITE ZERO DETECT ENABLE

Setting the IZD register bit will enable the internal infinite zero detect function:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) 0000111 DAC Channel Control	2	IZD	0	Infinite Zero Mute Enable 0 : disable infinite zero mute 1: enable infinite zero Mute

With IZD enabled, applying 1024 consecutive zero input samples to the DAC will cause both DAC outputs to be muted. Mute will be removed as soon as any channel receives a non-zero input.

DAC OUTPUT CONTROL

The DAC output control word determines how the left and right inputs to the audio Interface are applied to the left and right DACs:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R7 (07h) 0000111 DAC Control	7:4	PL[3:0]	1001	PL[3:0]	Left Output	Right Output
				0000	Mute	Mute
				0001	Left	Mute
				0010	Right	Mute
				0011	(L+R)/2	Mute
				0100	Mute	Left
				0101	Left	Left
				0110	Right	Left
				0111	(L+R)/2	Left
				1000	Mute	Right
				1001	Left	Right
				1010	Right	Right
				1011	(L+R)/2	Right
				1100	Mute	(L+R)/2
				1101	Left	(L+R)/2
				1110	Right	(L+R)/2
				1111	(L+R)/2	(L+R)/2

DAC DIGITAL VOLUME CONTROL

The DAC volume may also be adjusted in the digital domain using independent digital attenuation control registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) 0000011 Digital Attenuation DACL	7:0	LDA[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL in 0.5dB steps. See Table 11
	8	UPDATED	Not latched	Controls simultaneous update of Attenuation Latches 0: Store LDA in intermediate latch (no change to output) 1: Store LDA and update attenuation on both channels
R4 (04h) 0000100 Digital Attenuation DACR	7:0	RDA[6:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR in 0.5dB steps. See Table 11
	8	UPDATED	Not latched	Controls simultaneous update of Attenuation Latches 0: Store RDA in intermediate latch (no change to output) 1: Store RDA and update attenuation on both channels.
R5 (05h) 0000101 Master Digital Attenuation (both channels)	7:0	MDA[7:0]	11111111 (0dB)	Digital Attenuation data for DAC channels in 0.5dB steps. See Table 11
	8	UPDATED	Not latched	Controls simultaneous update of Attenuation Latches 0: Store gain in intermediate latch (no change to output) 1: Store gain and update attenuation on channels.

The volume update circuit of the WM8591 has two registers LDA and RDA. These can be accessed individually by writing to registers R3 and R4, or simultaneously by writing to R5 (MDA - Master Digital Attenuation). Writing to R5 will overwrite the contents of R3 and R4. There is no separate MDA register.

L/RDA[7:0]	ATTENUATION LEVEL
00(hex)	-∞ dB (mute)
01(hex)	-127dB
:	:
:	:
:	:
FE(hex)	-0.5dB
FF(hex)	0dB

Table 11 Digital Volume Control Attenuation Levels

The digital volume control also incorporates a zero cross detect circuit which detects a transition through the zero point before updating the digital volume control with the new volume. This is enabled by control bit DZCEN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) 0000111 DAC Control	0	DZCEN	0	DAC Digital Volume Zero Cross Enable: 0: Zero cross detect disabled 1: Zero cross detect enabled

DAC OUTPUT PHASE

The DAC Phase control word determines whether the output of the DAC is non-inverted or inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R6 (06h) 0000110 DAC Phase	1:0	PHASE [1:0]	00	Bit	DAC	Phase
				0	DACL	1 = invert
				1	DACR	1 = invert

ADC GAIN CONTROL

The ADC has an analogue input PGA and digital gain control for each stereo channel. Both the analogue and digital gains are adjusted by the same register, LAG for the left and RAG for the right. The analogue PGA has a range of +24dB to -21dB in 0.5dB steps. The digital gain control allows further attenuation (after the ADC) from -21.5dB to -103dB in 0.5dB steps. Table 12 shows how the register maps the analogue and digital gains.

LAG/RAG[7:0]	ATTENUATION LEVEL (AT OUTPUT)	ANALOGUE PGA	DIGITAL ATTENUATION
00(hex)	-∞ dB (mute)	-21dB	Digital mute
01(hex)	-103dB	-21dB	-82dB
:	:	:	:
A4(hex)	-21.5dB	-21dB	-0.5dB
A5(hex)	-21dB	-21dB	0dB
:	:	:	:
CF(hex)	0dB	0dB	0dB
:	:	:	:
FE(hex)	+23.5dB	+23.5dB	0dB
FF(hex)	+24dB	+24dB	0dB

Table 12 Analogue and Digital Gain Mapping for ADC

In addition a zero cross detect circuit is provided for the input PGA. When ZCLA/ZCRA is set with a write, the gain will update only when the input signal approaches zero (midrail). This minimises audible clicks and 'zipper' noise as the gain values change.

A timeout clock is also provided which will generate an update after a minimum of 131072 master clocks (= ~10.5ms with a master clock of 12.288MHz). The timeout clock may be disabled by setting TOD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) 0000111 Timeout Clock Disable	3	TOD	0	Analogue PGA Zero Cross Detect Timeout Disable 0 : Timeout enabled 1: Timeout disabled

Left and right inputs may also be independently muted. The LRBOTH control bit allows the user to write the same attenuation value to both left and right volume control registers, saving on software writes. The ADC volume and mute also applies to the bypass signal path.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) 0001110 Attenuation ADCL	7:0	LAG[7:0]	11001111 (0dB)	Attenuation Data for Left Channel ADC Gain in 0.5dB steps. See Table 12.
	8	ZCLA	0	Left Channel ADC Zero Cross Enable: 0: Zero cross disabled 1: Zero cross enabled
R15 (0Fh) 0001111 Attenuation ADCR	7:0	RAG[7:0]	11001111 (0dB)	Attenuation data for right channel ADC gain in 0.5dB steps. See Table 12.
	8	ZCRA	0	Right Channel ADC Zero Cross Enable: 0: Zero cross disabled 1: Zero cross enabled
R21 (15h) 0010101 ADC Input Mux	0	MUTERA	0	Mute for Right Channel ADC 0: Mute Off 1: Mute on
	1	MUTELA	0	Mute for Left Channel ADC 0: Mute Off 1: Mute on
	8	LRBOTH	0	Right Channel Input PGA Controlled by Left Channel Register 0: Right channel uses RAG and MUTERA 1: Right channel uses LAG and MUTELA

ADC/DAC SYNCHRONIZATION

The WM8591 has a range of features which can be configured to enhance the performance of the ADC and DAC when operated simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) ADC Interface Control	6	ADCMCLKINV	0	ADCMCLK Polarity: 0: non-inverted 1: inverted
	7	DACSYNCEN	0	Enable the DAC Synchronizer: 0: Disabled 1: Enabled
R28 (1Ch) 0011100 ADC/DAC Synchronization	0	ADCSYNCEN	0	Enable the ADC Synchronizer: 0: Disabled 1: Enabled
	4	ADCMCLK2DAC	0	Set both ADC and DAC to use ADCMCLK: 0: DAC uses DACMCLK 1: DAC uses ADCMCLK
	5	ADCMCLKX2	0	Allows DAC synchronizer to synchronize to ADC operating at 2x DAC rate: 0: Disabled 1: Enabled
	6	DACMCLKINV	0	DACMCLK Polarity: 0: non-inverted 1: inverted
	7	DACMCLKX2	0	Allows ADC synchronizer to synchronize to DAC operating at 2x ADC rate: 0: Disabled 1: Enabled
	8	DACMCLK2ADC	0	Set both DAC and ADC to use DACMCLK: 0: ADC uses ADCMCLK 1: ADC uses DACMCLK

LIMITER / AUTOMATIC LEVEL CONTROL (ALC)

The WM8591 has an automatic pga gain control circuit, which can function as a peak limiter or as an automatic level control (ALC). In peak limiter mode, a digital peak detector detects when the input signal goes above a predefined level and will ramp the pga gain down to prevent the signal becoming too large for the input range of the ADC. When the signal returns to a level below the threshold, the pga gain is slowly returned to its starting level. The peak limiter cannot increase the pga gain above its static level.

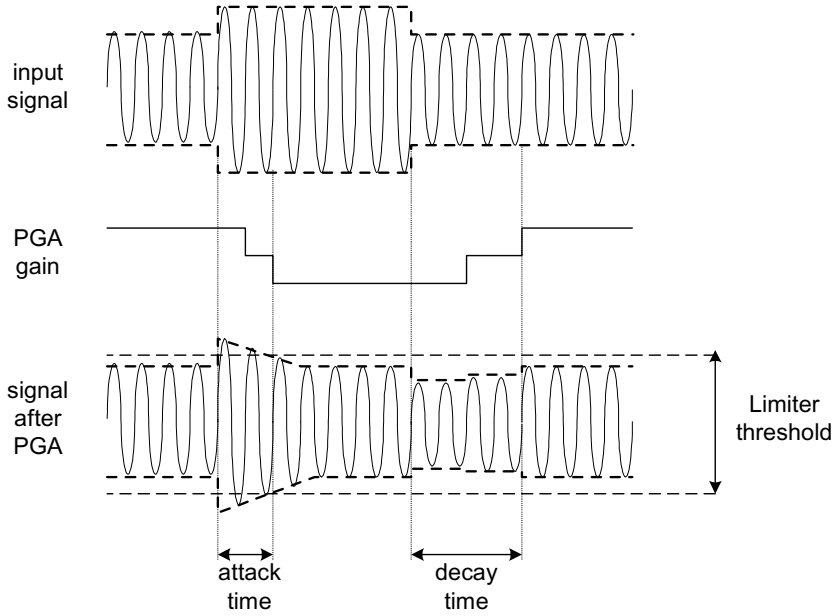


Figure 21 Limiter Operation

In ALC mode, the circuit aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

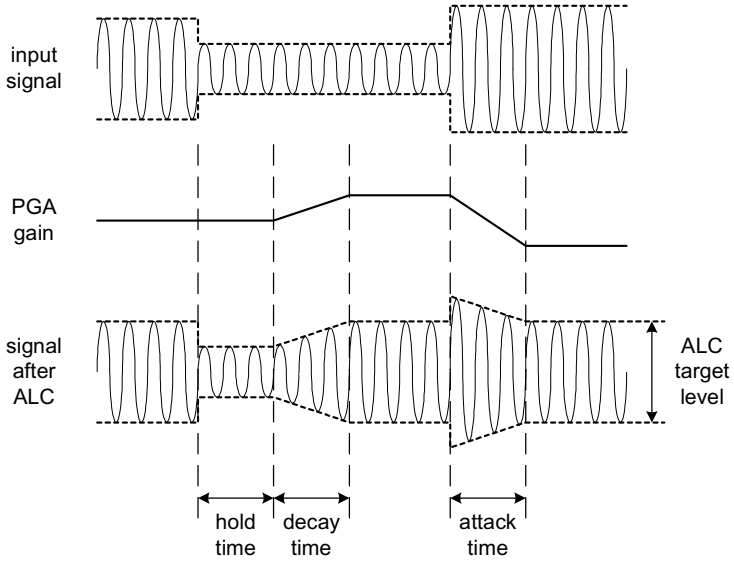


Figure 22 ALC Operation

The gain control circuit is enabled by setting the LCMODE control bit. The user can select between Limiter mode and three different ALC modes using the LCSEL control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) 0010001 ALC Control 2	8	LCMODE	1	ALC/Limiter Select 0 = ALC Mode 1 = Limiter Mode
R16 (10h) 0010000 ALC Control 1	8:7	LCSEL	11	LC Function Select 00 = Disabled 01 = Right channel only 10 = Left channel only 11 = Stereo

Both the ALC and Limiter functions can operate in stereo or single channel modes. In stereo mode, the ALC/Limiter operates on both PGAs. In single channel mode, only one PGA is controlled by the ALC/Limiter mechanism, while the other channel runs independently with its PGA gain set through the control register.

When enabled, the threshold for the limiter or target level for the ALC is programmed using the LCT control bits. This allows the threshold/target level to be programmed between 0dB and -22.5dB in 1.5dB steps. Note that for the ALC, target levels of 0dB and -1.5dB give a threshold of -3dB. This is because the ALC can give erroneous operation if the target level is set too high.

When disabled, the last gain level programmed by the ALC/Limiter will remain stored in the input PGAs. The desired fixed gain level must then be programmed manually via registers R14 and R15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) 0010000 ALC Control 1	3:0	LCT[3:0]	1110 (-1.5dB)	Limiter Threshold/ALC Target Level in 1.5dB Steps: 0000: -22.5dB FS 0001: -21dB FS … 1101: -3dB FS 1110: -1.5dB FS 1111: 0dB FS

ATTACK AND DECAY TIMES

The limiter and ALC have different attack and decay times which determine their operation. However, the attack and decay times are defined slightly differently for the limiter and for the ALC. DCY and ATK control the decay and attack times, respectively.

Decay time (Gain Ramp-Up). When in ALC mode, this is defined as the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –21dB up to +20 dB). When in limiter mode, it is defined as the time it takes for the gain to ramp up by 6dB.

The decay time can be programmed in power-of-two (2^n) steps. For the ALC this gives times from 33.6ms, 67.2ms, 134.4ms etc. to 34.41s. For the limiter this gives times from 1.2ms, 2.4ms etc., up to 1.2288s.

Attack time (Gain Ramp-Down) When in ALC mode, this is defined as the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from +20dB down to -21dB gain). When in limiter mode, it is defined as the time it takes for the gain to ramp down by 6dB.

The attack time can be programmed in power-of-two (2^n) steps, from 8.4ms, 16.8ms, 33.6ms etc. to 8.6s for the ALC and from 250us, 500us, etc. up to 256ms.

The time it takes for the recording level to return to its target value or static gain value therefore depends on both the attack/decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack/decay time.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R18 (12h) 0010010 ALC Control 3	3:0	ATK[3:0]	0010	LC Attack (Gain Ramp-down) Time	
				ALC mode 0000: 8.4ms 0001: 16.8ms 0010: 33.6ms… (time doubles with every step) 1010 or higher: 8.6s	Limiter Mode 0000: 250us 0001: 500us… 0010: 1ms (time doubles with every step) 1010 or higher: 256ms
	7:4	DCY [3:0]	1001	LC Decay (Gain Ramp-up) Time	
				ALC mode 0000: 33.5ms 0001: 67.2ms 0010: 134.4ms ….(time doubles for every step) 1001: 17.15s 1010 or higher: 34.3s	Limiter mode 0000: 1.2ms 0001: 2.4ms 0010: 4.8ms ….(time doubles for every step) 1001: 614.4ms 1010 or higher: 1.2288s

ZERO CROSS

The PGA has a zero cross detector to prevent gain changes introducing noise to the signal. In ALC mode the register bit ALCZC allows this to be turned off if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) 0010001 ALC Control 2	7	ALCZC	1 (enabled)	PGA Zero Cross Enable: 0 : disabled 1: enabled

MAXIMUM GAIN (ALC ONLY) AND MAXIMUM ATTENUATION

To prevent low level signals being amplified too much by the ALC, the MAXGAIN register sets the upper limit for the gain. This prevents low level noise being over-amplified. The MAXGAIN register has no effect on the limiter operation.

The MAXATTEN register sets a limit for the amount of attenuation below the static gain level that the limiter can apply. The MAXATTEN register has no effect in ALC mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R16 (10h) 0010000 ALC Control 1	6:4	MAXGAIN	111 (+24dB)	Set Maximum Gain for the PGA (ALC only): 111 : +24dB 110 : +20dB …..(-4dB steps) 010 : +4dB 001 : 0dB 000 : 0dB	
R20 (14h) 0010100 Limiter Control	3:0	MAXATTEN	0110 (-6dB)	Maximum Attenuation of PGA (Limiter only)	
				Limiter (attenuation below static)	
				0000 to 0011	-3dB
				0100	-4dB
				….	(-1dB steps)
				1110	-14dB
				1111	-15dB

When disabled, the last gain level programmed by the ALC/Limiter will remain stored in the input PGAs. The desired fixed gain level must then be programmed manually via registers R14 and R15.

SOFTWARE REGISTER RESET

Writing any value to register 0010111 will cause a register reset, resetting all register bits to their default values.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8591 can be configured using the Control Interface. All unused bits should be set to '0'.

REGISTER	B 15	B 14	B 13	B 12	B 11	B 10	B 9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT (HEX)
R3 (03h)	0	0	0	0	0	1	1	UPDATED	LDA[7:0]								0FF
R4 (04h)	0	0	0	0	1	0	0	UPDATED	RDA[7:0]								0FF
R5 (05h)	0	0	0	0	1	0	1	UPDATED	MDA[7:0]								0FF
R6 (06h)	0	0	0	0	1	1	0	0	0	0	0	0	0	0	PHASE[1:0]		000
R7 (07h)	0	0	0	0	1	1	1	0	PL[3:0]				TOD	IZD	ATC	DZCEN	090
R9 (09h)	0	0	0	1	0	0	1	0	0	0	0	ZFLAG POL	DMUTE	DZFM [1:0]		DEEMPH	004
R10 (0Ah)	0	0	0	1	0	1	0	DACOSR	0	0	DACWL[1:0]		DACBCP	DACLRP	DACFMT[1:0]		022
R11 (0Bh)	0	0	0	1	0	1	1	ADCHPD	DACSYNCEN	ADCMCLKINV	ADCWL[1:0]		ADCBCP	ADCLRP	ADCFMT[1:0]		022
R12 (0Ch)	0	0	0	1	1	0	0	ADCMS	DACMS	DACRATE[2:0]			ADCOSR	ADCRATE[2:0]			122
R13 (Odh)	0	0	0	1	1	0	1	0	0	0	0	0	0	DACPD	ADCPD	PDWN	000
R14 (0Eh)	0	0	0	1	1	1	0	ZCLA	LAG[7:0]								0CF
R15 (0Fh)	0	0	0	1	1	1	1	ZCRA	RAG[7:0]								0CF
R16 (10h)	0	0	1	0	0	0	0	LCSEL[1:0]		MAXGAIN[2:0]			LCT[3:0]				1FE
R17 (11h)	0	0	1	0	0	0	1	LCMODE	ALCZC	0	0	0	0	0	0	0	180
R18 (12h)	0	0	1	0	0	1	1	0	DCY[3:0]				ATK[3:0]				092
R20 (14h)	0	0	1	0	1	0	0	0	0	0	0	0	MAXATTEN[3:0]				006
R21 (15h)	0	0	1	0	1	0	1	LRBOTH	0	0	0	0	0	0	MUTELA	MUTERA	000
R23 (17h)	0	0	1	0	1	1	1	SOFTWARE RESET									not reset
R28 (1Ch)	0	0	1	1	1	0	0	DACMCLK 2ADC	DACMCLK X2	DACMCLK INV	ADCMCLK X2	ADCMCLK 2DAC	BCLK_RATE		0	ADCSYNCEN	000

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="2">R3 (03h)
0000011
Digital Attenuation DACL</td><td>7:0</td><td>LDA[7:0]</td><td>11111111
(0dB)</td><td>Digital Attenuation Data for Left Channel DACL in 0.5dB Steps</td></tr>
<tr><td>8</td><td>UPDATED</td><td>Not latched</td><td>Controls Simultaneous Update of all Attenuation Latches:
0: Store LDA1 in intermediate latch (no change to output)
1: Store LDA1 and update attenuation on all channels</td></tr>
<tr><td rowspan="2">R4 (04h)
0000100
Digital Attenuation DACR</td><td>7:0</td><td>RDA[6:0]</td><td>11111111
(0dB)</td><td>Digital Attenuation Data for Right Channel DACR in 0.5dB Steps</td></tr>
<tr><td>8</td><td>UPDATED</td><td>Not latched</td><td>Controls Simultaneous Update of all Attenuation Latches:
0: Store RDA1 in intermediate latch (no change to output)
1: Store RDA1 and update attenuation on all channels</td></tr>
<tr><td rowspan="2">R5 (05h)
0000101
Master Digital Attenuation (All Channels)</td><td>7:0</td><td>MDA[7:0]</td><td>11111111
(0dB)</td><td>Digital Attenuation Data for all DAC Channels in 0.5dB Steps</td></tr>
<tr><td>8</td><td>UPDATED</td><td>Not latched</td><td>Controls Simultaneous Update of all Attenuation Latches:
0: Store gain in intermediate latch (no change to output)
1: Store gain and update attenuation on all channels</td></tr>
<tr><td>R6 (06h)
0000110
Phase Swaps</td><td>1:0</td><td>PHASE</td><td>00</td><td>Controls Phase of DAC Outputs (LEFT, RIGHT Channel):
0: Sets non inverted output phase
1: inverts phase of DAC output</td></tr>
<tr><td rowspan="5">R7 (07h)
0000111
DAC Control</td><td>0</td><td>DZCEN</td><td>0</td><td>DAC Digital Volume Zero Cross Enable:
0: Zero Cross detect disabled
1: Zero Cross detect enabled</td></tr>
<tr><td>1</td><td>ATC</td><td>0</td><td>Attenuator Control:
0: All DACs use attenuations as programmed
1: Right DAC uses left DAC attenuations</td></tr>
<tr><td>2</td><td>IZD</td><td>0</td><td>Infinite Zero Detection Circuit Control and Automute Control:
0: Infinite zero detect automute disabled
1: Infinite zero detect automute enabled</td></tr>
<tr><td>3</td><td>TOD</td><td>0</td><td>DAC and ADC Analogue Zero Cross Detect Timeout Disable:
0 : Timeout enabled
1: Timeout disabled</td></tr>
<tr><td>7:4</td><td>PL[3:0]</td><td>1001</td><td>DAC Output Control
<table>
<tr><th>PL[3:0]</th><th>Left Output</th><th>Right Output</th><th>PL[3:0]</th><th>Left Output</th><th>Right Output</th></tr>
<tr><td>0000</td><td>Mute</td><td>Mute</td><td>1000</td><td>Mute</td><td>Right</td></tr>
<tr><td>0001</td><td>Left</td><td>Mute</td><td>1001</td><td>Left</td><td>Right</td></tr>
<tr><td>0010</td><td>Right</td><td>Mute</td><td>1010</td><td>Right</td><td>Right</td></tr>
<tr><td>0011</td><td>(L+R)/2</td><td>Mute</td><td>1011</td><td>(L+R)/2</td><td>Right</td></tr>
<tr><td>0100</td><td>Mute</td><td>Left</td><td>1100</td><td>Mute</td><td>(L+R)/2</td></tr>
<tr><td>0101</td><td>Left</td><td>Left</td><td>1101</td><td>Left</td><td>(L+R)/2</td></tr>
<tr><td>0110</td><td>Right</td><td>Left</td><td>1110</td><td>Right</td><td>(L+R)/2</td></tr>
<tr><td>0111</td><td>(L+R)/2</td><td>Left</td><td>1111</td><td>(L+R)/2</td><td>(L+R)/2</td></tr>
</table></td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) 0001001 DAC Control	0	DEEMPH	0	De-emphasis Mode Select: 0 : Normal mode 1: De-emphasis mode
	2:1	DZFM	00	DZFM / ZFLAG1 / ZFLAG2 00 / Disabled / Disabled 01 / Left channels zero / Right channels zero 10 / Both channels zero / Both channels zero 11 / Either channel zero / Either channel zero
	3	DMUTE	0	DAC Channel Soft Mute Enables: 0: Mute disabled 1: Mute enabled
	4	ZFLAGPOL	0	ZFLAG polarity ZFLAGPOL / ZFLAGL / ZFLAGR 0 / Pin pulls low to indicate zero condition, high impedance otherwise 1 / Pin is high impedance when zero condition detected, pulls low otherwise
R10 (0Ah) 0001010 DAC Interface Control	1:0	DACFMT[1:0]	01	DAC Interface Format Select: 00: Right justified mode 01: Left justified mode 10: I^2S mode 11: DSP mode
	2	DACLRP	0	DACLRC Polarity or DSP Early/Late Mode Select Left Justified / Right Justified / I^2S: 0: Standard DACLRC Polarity 1: Inverted DACLRC Polarity DSP Mode: 0: Mode A 1: Mode B
	3	DACBCP	0	DAC BITCLK Polarity: 0: Normal – DIN and DACLRC sampled on rising edge of DACBCLK 1: Inverted - DIN and DACLRC sampled on falling edge of DACBCLK
	5:4	DACWL[1:0]	10	DAC Input Word Length: 00: 16-bit Mode 01: 20-bit Mode 10: 24-bit Mode 11: 32-bit Mode (not supported in right justified mode)
	8	DACOSR	0	DAC Oversample Rate Select: 0: 128x oversampling 1: 64x oversapmling
R11 (0Bh) 0001011 ADC Interface Control	1:0	ADCFMT[1:0]	01	ADC Interface Format Select: 00: Right justified Mode 01: Left justified Mode 10: I^2S Mode 11: DSP Mode
	2	ADCLRP	0	ADCLRC Polarity or DSP Early/Late Mode Select Left Justified / Right Justified / I^2S: 0: Standard ADCLRC polarity 1: Inverted ADCLRC polarity DSP Mode: 0: Mode A 1: Mode B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	ADCBCP	0	ADC BITCLK Polarity: 0: Normal – ADCLRC sampled on rising edge of ADCBCLK; DOUT changes on falling edge of ADCBCLK 1: Inverted - ADCLRC sampled on falling edge of ADCBCLK; DOUT changes on rising edge of ADCBCLK
	5:4	ADCWL[1:0]	10	ADC Input Word Length: 00: 16-bit mode 01: 20-bit mode 10: 24-bit mode 11: 32-bit mode (not supported in right justified mode)
	6	ADCMCLKINV	0	ADCMCLK Polarity: 0: non-inverted 1: inverted
	7	DACSYNCEN	0	Enable the DAC Synchronizer: 0: Disabled 1: Enabled
	8	ADCHPD	0	ADC High Pass Filter Powerdown: 0: HP Filter Enabled 1: HP Filter Disabled
R12 (0Ch) 0001100 Master Mode Control	2:0	ADCRATE[2:0]	010	Master Mode ADCMCLK:ADCLRC Ratio Select: 010: 256fs 011: 384fs 100: 512fs 101: 768fs
	3	ADCOSR	0	ADC Oversample Rate Select: 0: 128x oversampling 1: 64x oversampling
	6:4	DACRATE[2:0]	010	Master Mode DACMCLK:DACLRC Ratio Select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs 101: 768fs
	7	DACMS	0	DAC Master/Slave Interface Mode Select: 0: Slave Mode – DACLRC and DACBCLK are inputs 1: Master Mode –DACLRC and DACBCLK are outputs
	8	ADCMS	1	ADC Master/Slave Interface Mode Select: 0: Slave Mode – ADCLRC and ADCBCLK are inputs 1: Master Mode – ADCLRC and ADCBCLK are outputs
R13 (0Dh) 0001101 PWR Down Control	0	PDWN	0	Chip Powerdown Control (works in tandem with ADCPD and DACPD): 0: All circuits running, outputs are active 1: All circuits in power save mode, outputs muted
	1	ADCPD	0	ADC Powerdown: 0: ADC enabled 1: ADC disabled
	2	DACPD	0	DAC Powerdown: 0: DAC enabled 1: DAC disabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 (0Eh) 0001110 Attenuation ADCL	7:0	LAG[7:0]	11001111 (0dB)	Attenuation Data for Left Channel ADC Gain in 0.5dB Steps: 00000000 : digital mute 00000001 : -103dB …….. 11001111 : 0dB …… 11111110 : +23.5dB 11111111 : +24dB
	8	ZCLA	0	Left ADC Zero Cross Enable: 0: Zero cross disabled 1: Zero cross enabled
R15 (0Fh) 0001111 Attenuation ADCR	7:0	RAG[7:0]	11001111 (0dB)	Attenuation Data for Right Channel ADC Gain in 0.5dB Steps: 00000000 : digital mute 00000001 : -103dB …….. 11001111 : 0dB …… 11111110 : +23.5dB 11111111 : +24dB
	8	ZCRA	0	Right ADC Zero Cross Enable: 0: Zero cross disabled 1: Zero cross enabled
R16 (10h) 0010000 ALC Control 1	3:0	LCT[3:0]	1110 (-1.5dB)	Limiter Threshold/ALC Target Level in 1.5dB Steps: 0000: -22.5dB FS 0001: -21dB FS … 1101: -3dB FS 1110: -1.5dB FS 1111: 0dB FS
	6:4	MAXGAIN[2:0]	111 (+24dB)	Set Maximum Gain of PGA: 111 : +24dB 110 : +20dB ….(-4dB steps) 010 : +4dB 001 : 0dB 000 : 0dB
	8:7	LCSEL[1:0]	11 (Stereo)	LC Function Select 00 = Disabled 01 = Right channel only 10 = Left channel only 11 = Stereo
R17 (11h) 0010001 ALC Control 2	7	ALCZC	1 (zero cross on)	ALC Uses Zero Cross Detection Circuit.
	8	LCMODE	1	ALC/Limiter Select: 0 = ALC Mode 1 = Limiter Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R18 (12h) 0011000 ALC Control 3	3:0	ATK[3:0]	0010 (33.6ms/ 1ms)	ALC/Limiter Attack (gain ramp-down) Time	
				ALC Mode: 0000: 8.4ms 0001: 16.8ms 0010: 33.6ms… (time doubles with every step) 1010 or higher: 8.6s	Limiter Mode: 0000: 250us 0001: 500us… 0010: 1ms (time doubles with every step) 1010 or higher: 256ms
	7:4	DCY[3:0]	1001 (17.15s/ 614.4ms)	ALC/Limiter Decay (gain ramp up) Time	
				ALC Mode: 0000: 33.5ms 0001: 67.2ms 0010: 134.4ms ….(time doubles for every step) 1001: 17.15s 1010 or higher: 34.3s	Limiter Mode: 0000: 1.2ms 0001: 2.4ms 0010: 4.8ms ….(time doubles for every step) 1001: 614.4ms 1010 or higher: 1.2288s
R20 (14h) 0010100 Limiter Control	3:0	MAXATTEN [3:0]	0110 (-6dB)	Maximum Attenuation of PGA (Limiter only)	
				Limiter (attenuation below static)	
				0000 to 0011	-3dB
				0100	-4dB
				….	(-1dB steps)
				1110	-14dB
				1111	-15dB
R21 (15h) 0010101 ADC Mux Control	0	MUTERA	0	Mute for Right Channel ADC: 0: Mute off 1: Mute on	
	1	MUTELA	0	Mute for Left Channel ADC: 0: Mute off 1: Mute on	
	8	LRBOTH	0	Right Channel Input PGA Controlled by Left Channel Register: 0: Right channel uses RAG and MUTERA 1: Right channel uses LAG and MUTELA	
R23 (17h) 0010111 Software Reset	[8:0]	RESET	Not reset	Writing any value to this register will apply a reset to the device registers.	
R28 (1Ch) 0011100 ADC/DAC Synchronization	0	ADCSYNCEN	0	Enable the ADC Synchronizer: 0: Disabled 1: Enabled	
	3:2	BCLK_RATE	00	Set ADCBCLK and DACBCLK output rate in Master Mode: 00: BCLK = MCLK/4 (MCLK in DSP Mode) 01: BCLK = MCLK/4 (MCLK in DSP Mode) 10: BCLK = 64fs 11: BCLK = 128fs	
	4	ADCMCLK2DAC	0	Set both ADC and DAC to use ADCMCLK: 0: DAC uses DACMCLK 1: DAC uses ADCMCLK	
	5	ADCMCLKX2	0	Allows DAC synchronizer to synchronize to ADC operating at 2x DAC rate: 0: Disabled 1: Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	DACMCLKINV	0	DACMCLK Polarity: 0: non-inverted 1: inverted
	7	DACMCLKX2	0	Allows ADC synchronizer to synchronize to DAC operating at 2x ADC rate: 0: Disabled 1: Enabled
	8	DACMCLK2ADC	0	Set both DAC and ADC to use DACMCLK: 0: ADC uses ADCMCLK 1: ADC uses DACMCLK

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	±0.01 dB	0		0.4535fs	
	-6dB		0.5fs		
Passband ripple				±0.01	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-65			dB
Group Delay			22		fs
DAC Filter					
Passband	±0.05 dB			0.454fs	
	-3dB		0.487 fs		
Passband ripple	f < 0.444fs			±0.05	dB
Stopband		0.555fs			
Stopband Attenuation	f > 0.555fs	-60			dB
Group Delay			19		fs

Table 13 Digital Filter Characteristics

DAC FILTER RESPONSES

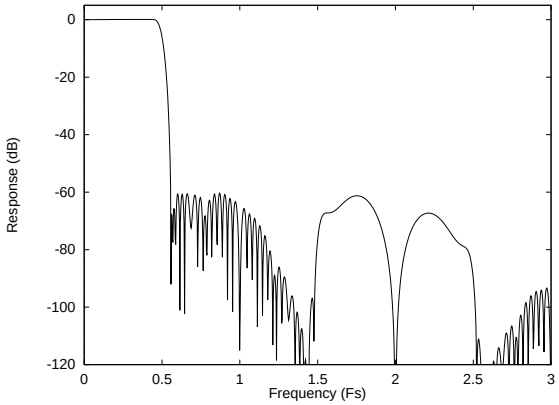


Figure 23 DAC Digital Filter Frequency Response -44.1, 48 and 96kHz

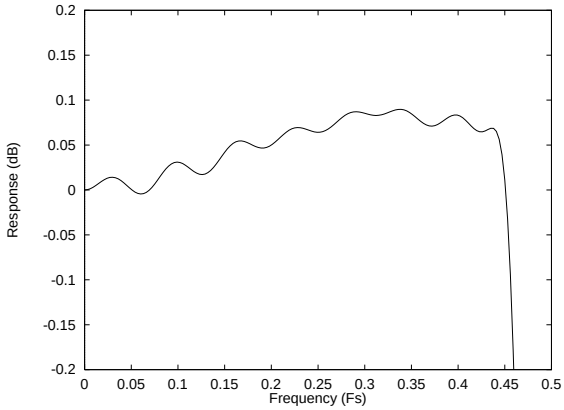


Figure 24 DAC Digital Filter Ripple -44.1, 48 and 96kHz

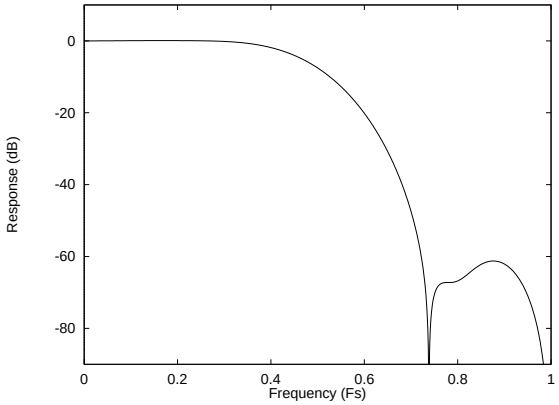


Figure 25 DAC Digital Filter Frequency Response (with DACOSR = 1) -192kHz

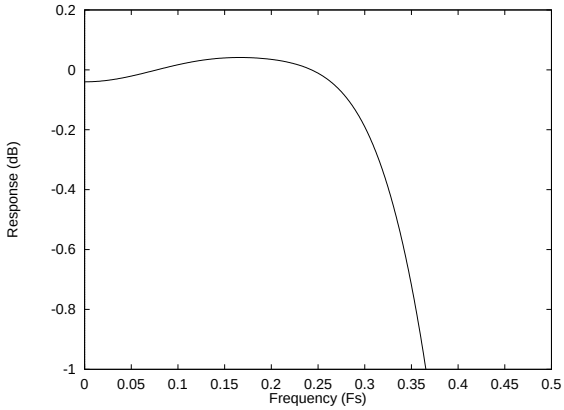


Figure 26 DAC Digital Filter Ripple (with DACOSR = 1) -192kHz

ADC FILTER RESPONSES

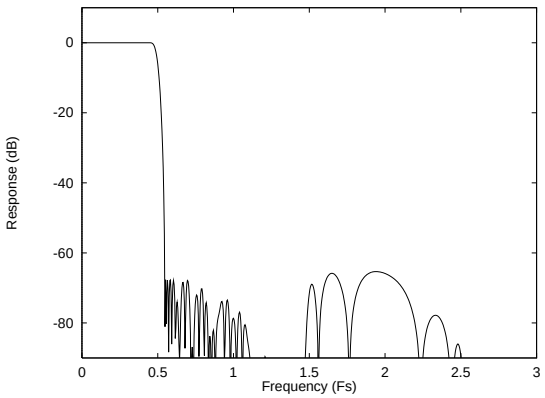


Figure 27 ADC Digital Filter Frequency Response

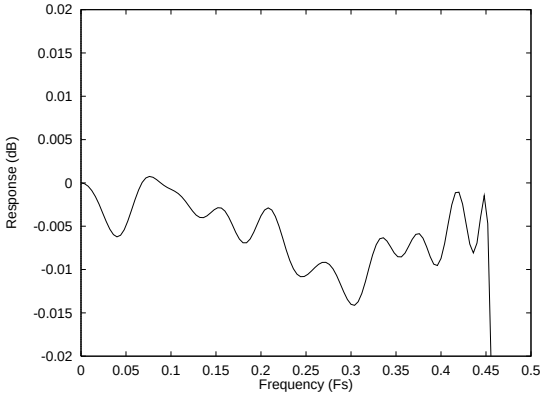


Figure 28 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8591 has a selectable digital highpass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

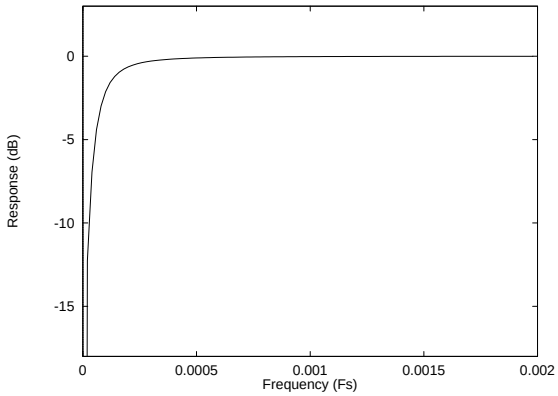


Figure 29 ADC Highpass Filter Response

DIGITAL DE-EMPHASIS CHARACTERISTICS

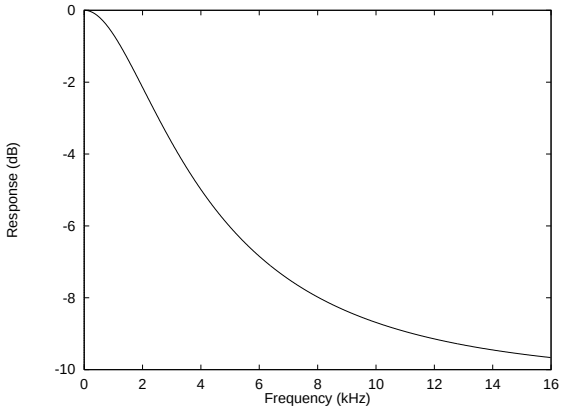


Figure 30 De-Emphasis Frequency Response (32kHz)

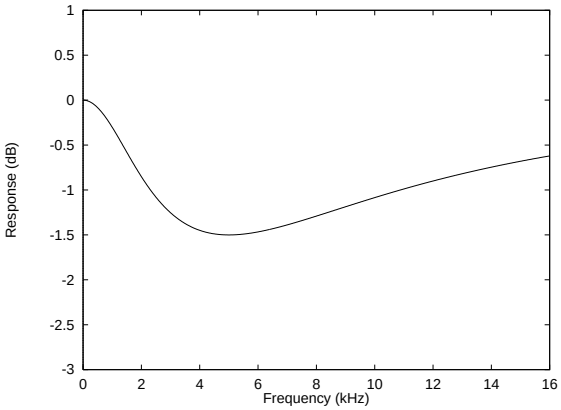


Figure 31 De-Emphasis Error (32kHz)

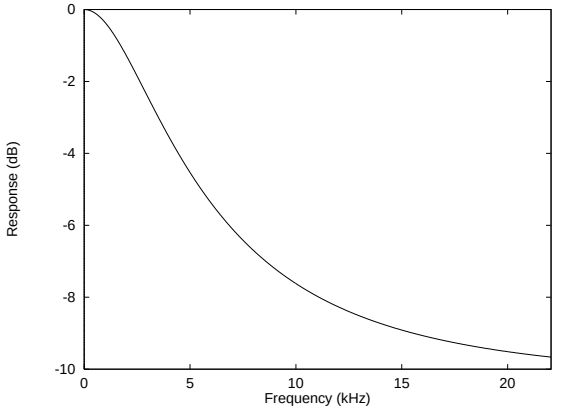


Figure 32 De-Emphasis Frequency Response (44.1kHz)

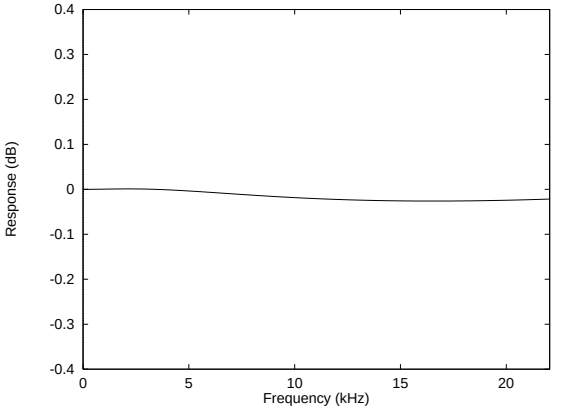


Figure 33 De-Emphasis Error (44.1kHz)

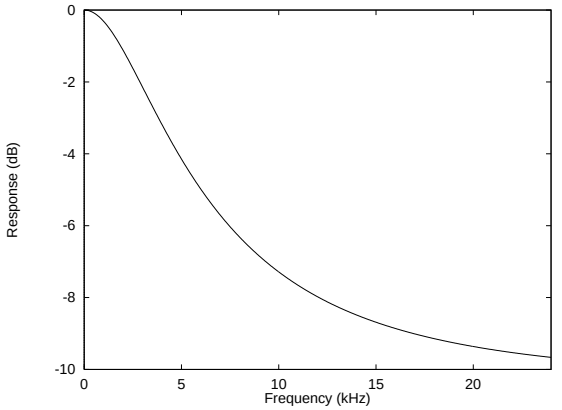


Figure 34 De-Emphasis Frequency Response (48kHz)

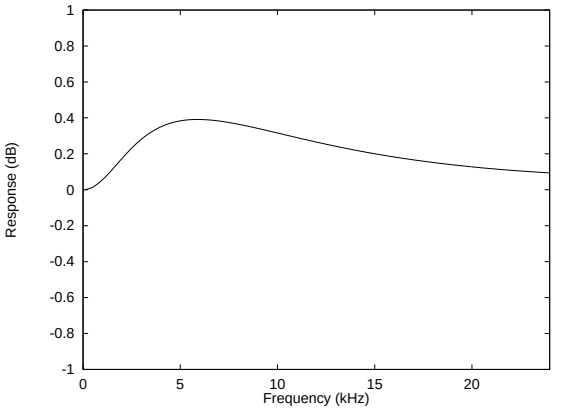


Figure 35 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

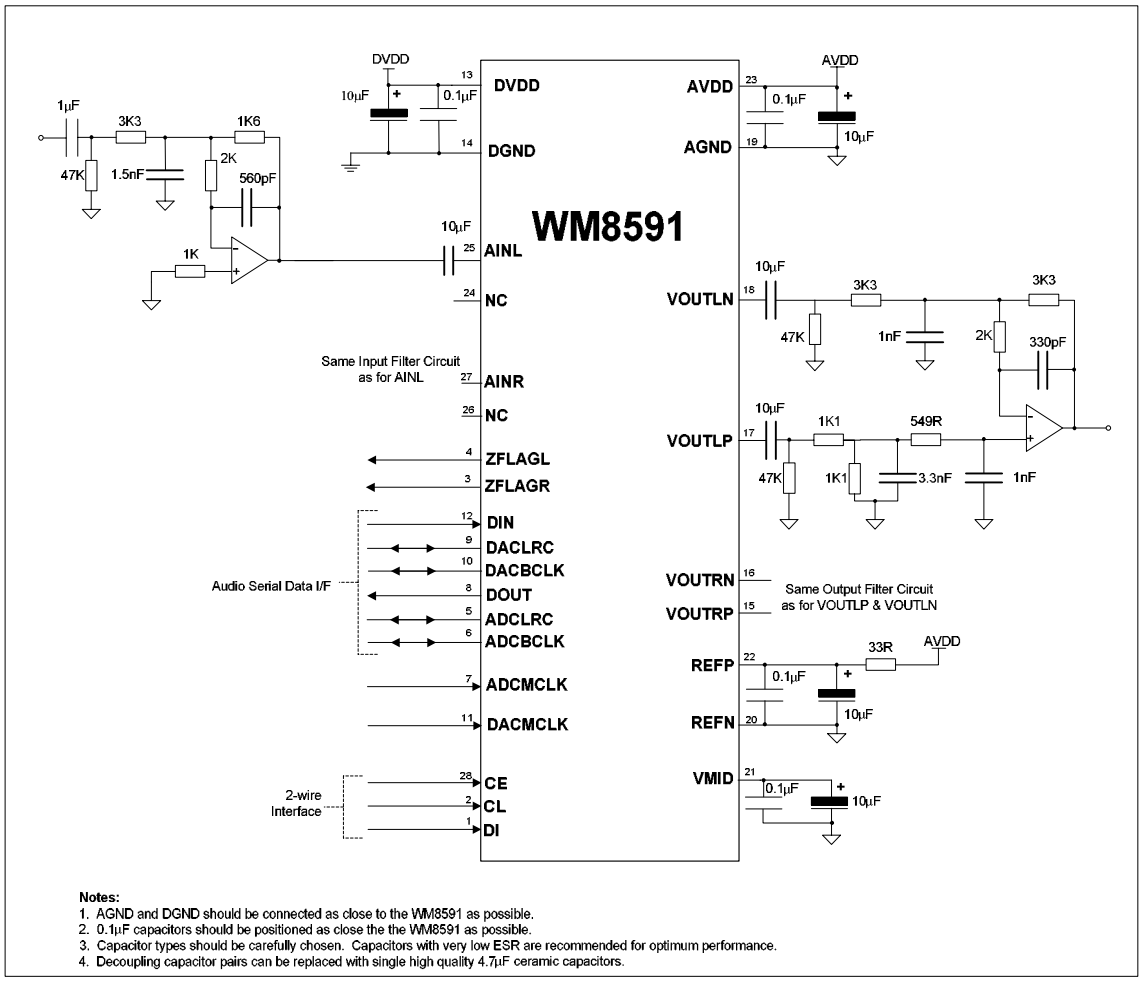


Figure 36 Recommended External Components

USE OF ADC/DAC SYNCHRONIZER

When operating the ADC and DAC simultaneously, the ADC/DAC synchronizer should be configured to optimise internal clock phasing and device performance. The synchronizer is controlled by registers R11 and R28 and recommended settings are described in Table 14.

In order for the clock synchronizer to operate, DAC_MCLK and ADC_MCLK must be phase locked with coincident clock edges.

CONFIGURATION				REGISTER SETTINGS					
DAC fs (kHz)	DAC MCLK RATE	ADC fs (kHz)	ADC MCLK RATE	ADCMCLKINV	ADCSYNCEN	ADCMCLK2DAC	DACMCLKINV	DACMCLKX2	DACMCLK2ADC
48	768fs	48	384fs	1	1	1*	0	0	0
96	384fs	48	384fs	1	1	1*	0	0	0
32	1152fs	48	384fs	0	0	0	0	0	1**
44.1	768fs	48	384fs	0	0	0	0	0	0
48	256fs	48	256fs	0	1	1*	1	0	0
48	512fs	48	256fs	0	1	0	1	1	0
48	512fs	48	256fs	0	1	1*	1	0	0
96	256fs	48	256fs	0	1	1*	1	0	0
32	768fs	48	256fs	0	0	0	0	0	0

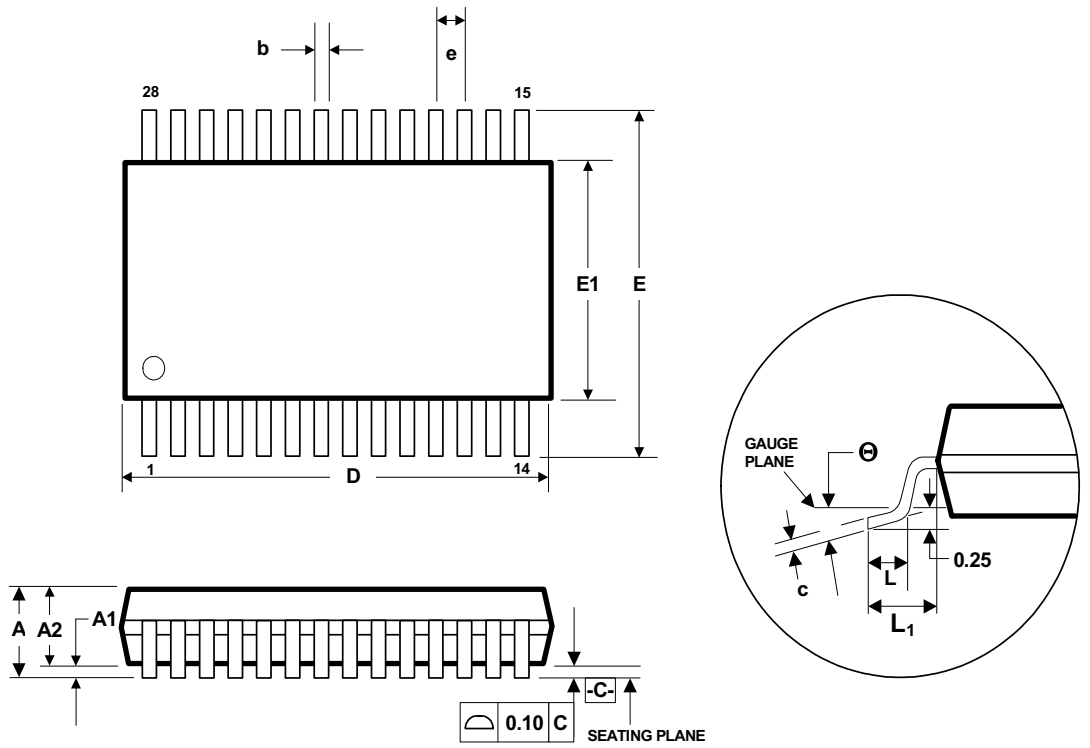
Table 14 Synchronizer Configurations

* In those modes where ADCMCLK2DAC is set, the DAC is driven by the clock signal applied to the ADC_MCLK pin. If the DAC is operated in Master mode, the DACRATE bits (R12 [6:4]) must be set to match the ADC_MCLK rate.

** In those modes where DACMCLK2ADC is set, the ADC is driven by the clock signal applied to the DAC_MCLK pin. If the ADC is operated in Master mode, the ADCRATE bits (R12 [2:0]) must be set to match the DAC_MCLK rate.

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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