Winbond
Mobile Keyboard and
Embedded Controller

W83L951DG
W83L951FG

Date: August/2006 Revision: 1.00

W83L951DG/W83L951FG Data Sheet Revision History

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1	n.a.	8/7/2006	1.0	1.0	First Release
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Winbond Electronics Corp.

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1. GENERAL DESCRIPTION

The Winbond mobile keyboard and embedded controller W83L951DG/FG architecture consists of a Turbo-8051 core logic controller and surrounded by various components, 2K+256 bytes of RAM, 64K on-chip FLASH, LPC host interface, 13 general purpose I/O port with 24 external interrupt source, 4 timers, 1 serial port, 2 SMBus interface for master mode, 3 PS/2 port, 2 PWM channels with 8-bits and 2 PWM channels with 16-bits, 2 D-A and 8 A-D converters, 1 Consumer Infrared Communications Receiver, 2 Fan Tachometer , 1 Real Time Clock Generator, and Matrix Interface. The part number with an affix of “G” is the Lead-free package product.

2. PRODUCT FEATURES

- Core logic

  8-bit Turbo 8052 Microprocessor Code based, Speed up to 24MHz

  256 bytes Internal RAM

  64K bytes Embedded Programmable Flash Memory

  2K bytes External SRAM

- Host interface

  Software Optional with LPC Interface

  Primary Programmable I/O Address Communication Port in LPC Mode

  Support SERIRQ in LPC Interface

  Support Hardware Fast Gate A20 and KBRST

  Support Port 92h

- SMBus

  Support 2 SMBus Interface support Master Mode.

- Timers

  Support Four Timer Signal with Three Pre-scalars

  Timer 1 and 2 Shard the Same Pre-scalar and are Free-Running Only.

  Timer X and Y Have Individual Pre-scalar and Support up to Four Control Modes, Free Running, Pulse Output, Event Counter and Pulse Width Measurement

- PWM

  Support Four PWM Channels

  PWM 0 and 1 are 8-bits and Programmable Frequency from 62Hz to 7.5 KHz

  PWM 2 and 3 are 16-bits and Programmable Frequency from 6Hz to 3MHz

- Fan Tachometer

  Support two Fan Tachometer Inputs

- A/D Converter

  Firmware Programmable Optional with 10-bite or 8-bit Resolution

  Support Eight Channels

- D/A Converter
  8-bit Resolution
  Support Two Channels

- PS2
  Support Three Hardware PS2 Channels
  Optional PS2 Clock Inhibit by Hardware or Firmware

- Keyboard Controller
  Support 16*8 Keyboard Matrix-scan, Expanding to 18*8 and 20*8

- GPIO
  Support 104 Useful GPIO Pins Totally and Bit–addressable to Facility Firmware Coding

- FLASH
  Support External On-Board 64K Flash via Matrix Interface (GP0, 1, 3)

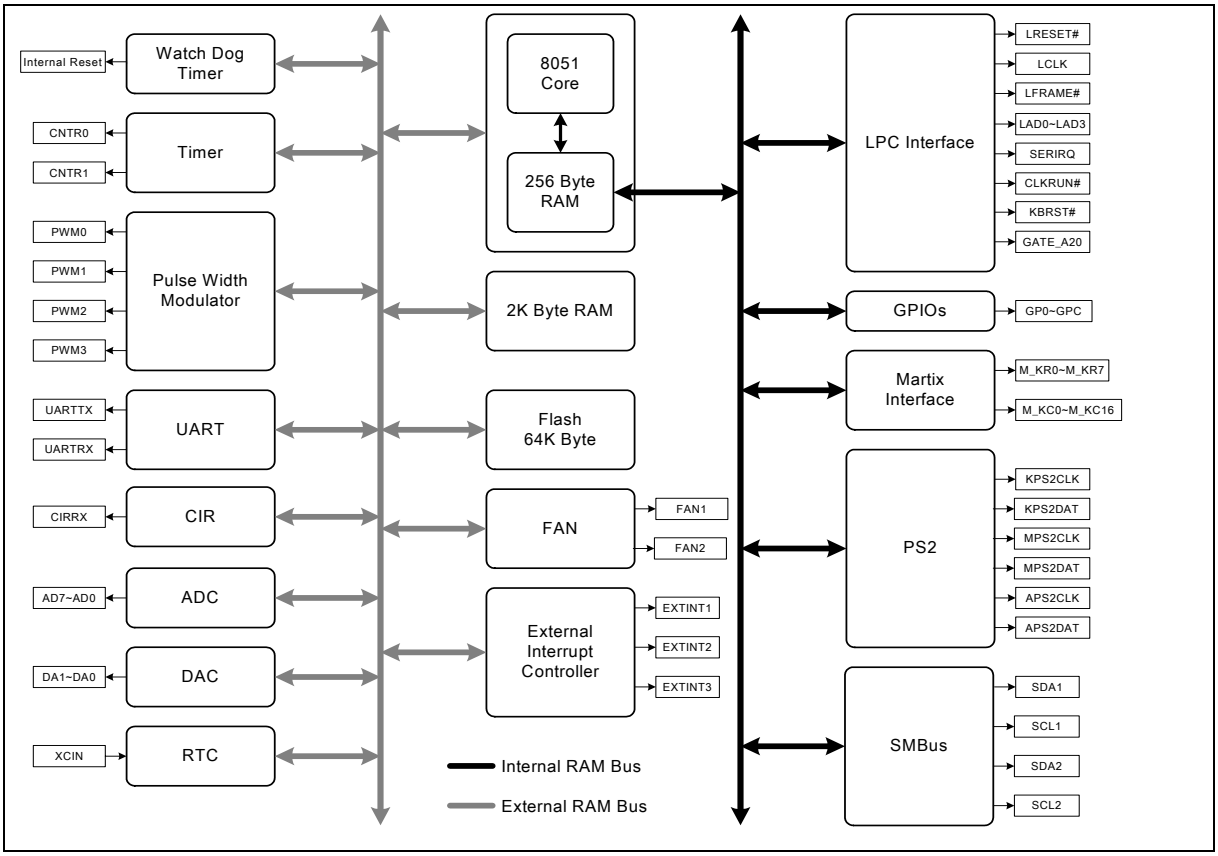
- CIR
  Support Decoding for the NEC Consumer IR Remote Control Format

- RTC
  Real Time Clock Generator with 32.768 KHz Input

- ACPI
  Support ACPI Appliance
  Secondary Programmable I/O Address Communication Port in LPC Mode

- Package
  -Pin QFP and 128-Pin LQFP Leadfree Package Options, in compliance with the RoHS (Restriction on Hazardous Substances)

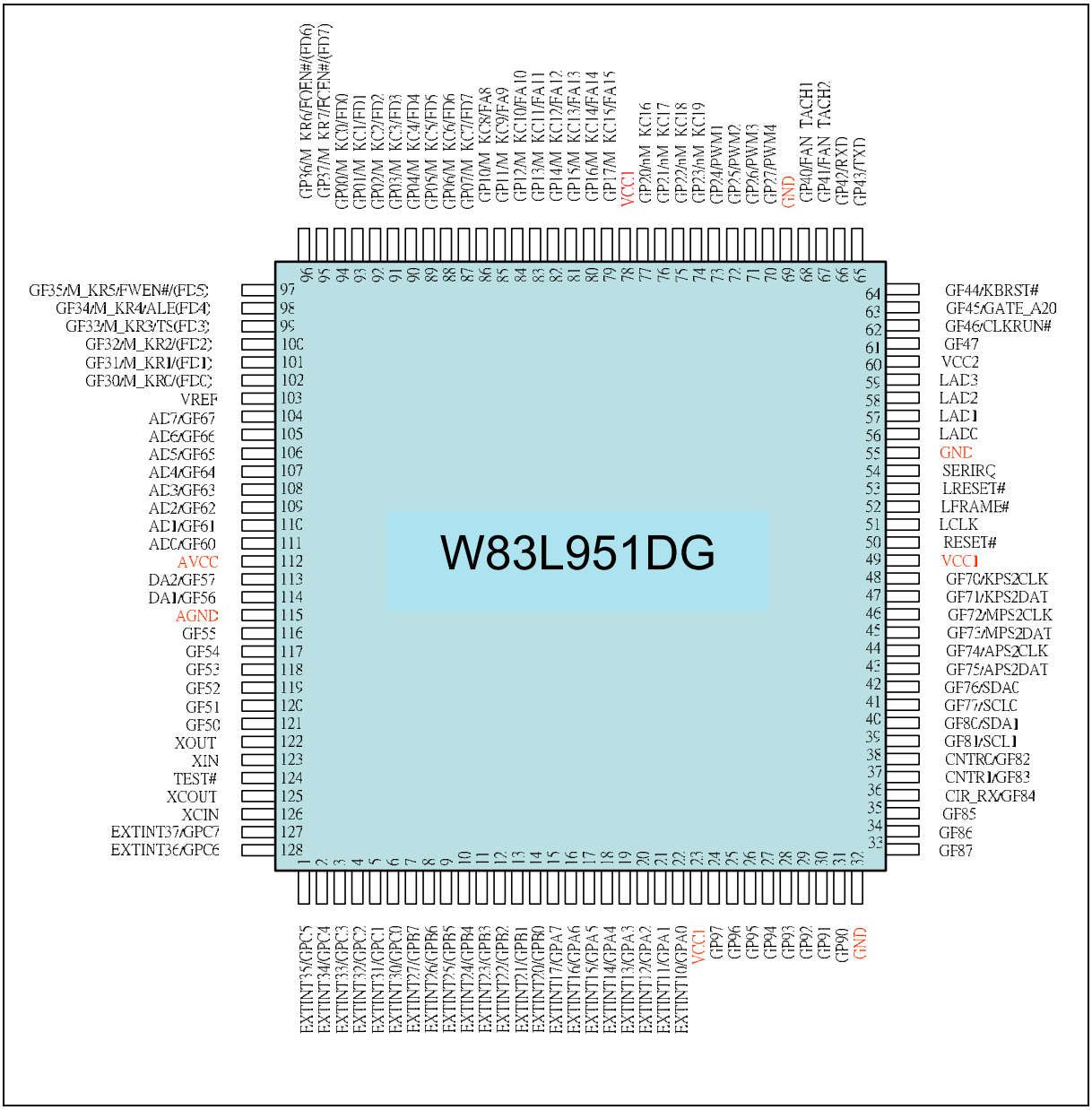
3. BLOCK DIAGRAM



Note: This Block Diagram should not used for pin count.

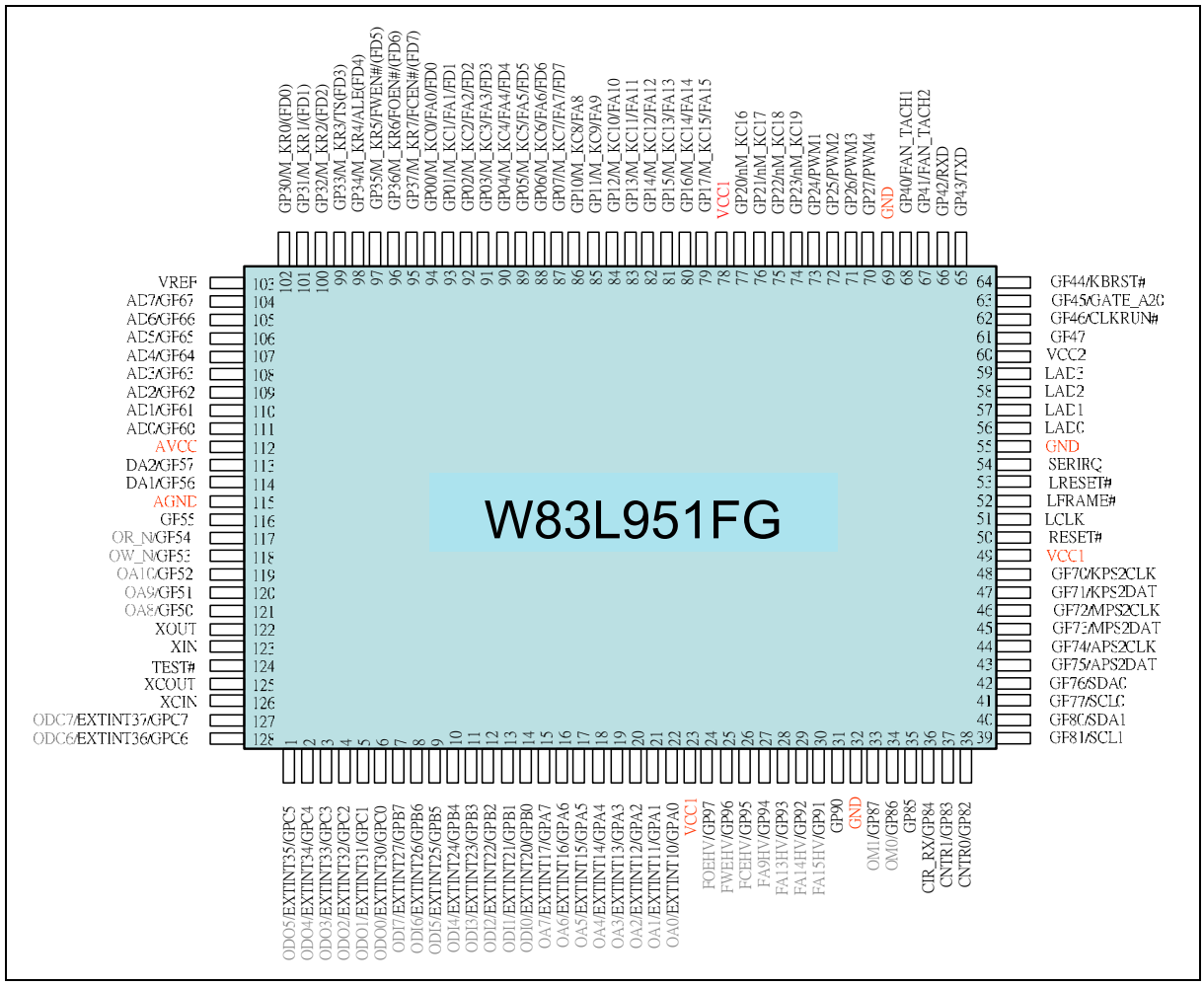
4. PIN CONFIGURATION FOR W83L951DG/W83L951FG

128-Pin Low Profile Quad Flat Pack (LQFP)



Note: The Pin Configuration is only for 128-pin LQFP Package.

128-Pin Quad Flat Pack (QFP)



Note: The Pin Configuration is only for 128-pin QFP Package.

5. PIN DESCRIPTION

Table 5-1 Pin Type Description

TYPE	DESCRIPTION
I/O_{12tsm}	Bi-directional pin, TTL level, Schmitt-trigger input, selectable 250uA/12mA sink capability, 12mA select source capability
I/O_{12tsai}	Bi-directional pin, TTL level, Schmitt-trigger input, Analog Input, 12mA source-sink capability
I/O_{12tsao}	Bi-directional pin, TTL level, Schmitt-trigger input, Analog Output, 12mA source-sink capability
I/O_{16tsh}	Bi-directional pin, TTL level, Schmitt-trigger input, 5V Tolerant, 16mA source-sink capability
I/O_{24ts}	Bi-directional pin, Schmitt-trigger input, 24mA source-sink capability
I_{ts}	TTL level, Schmitt-trigger input
I_c, O_c	Clock Input, Clock Out
I_{vdd}	Voltage Input
I_{vss}	Ground Input

Note: t – TTL level, s – Schmitt-trigger, m – matrix keyboard, ai – analog input, ao – analog output, h – 5V Tolerant, c – clock.

5.1 Pin configuration table

Table 5-2 Pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GPC5 EXTINT35	1	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC4 EXTINT34	2	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC3 EXTINT33	3	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC2 EXTINT32	4	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC1 EXTINT31	5	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC0 EXTINT30	6	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB7 EXTINT27	7	I/O16tsh	General Purpose I/O Function External Interrupt Input

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GPB6 EXTINT26	8	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB5 EXTINT25	9	I/O16tsh	General Purpose I/O Function External Interrupt Input
SYMBOL	PIN	I/O	FUNCTION
GPB4 EXTINT24	10	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB3 EXTINT23	11	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB2 EXTINT22	12	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB1 EXTINT21	13	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB0 EXTINT20	14	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA7 EXTINT17	15	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA6 EXTINT16	16	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA5 EXTINT15	17	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA4 EXTINT14	18	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA3 EXTINT13	19	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA2 EXTINT12	20	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA1 EXTINT11	21	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA0 EXTINT10	22	I/O16tsh	General Purpose I/O Function External Interrupt Input
VCC1	23	Ivdd	Normal Power Input, +3.3V
GP97	24	I/O16tsh	General Purpose I/O Function

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP96	25	I/O16tsh	General Purpose I/O Function
GP95	26	I/O16tsh	General Purpose I/O Function
GP94	27	I/O16tsh	General Purpose I/O Function
GP93	28	I/O16tsh	General Purpose I/O Function
GP92	29	I/O16tsh	General Purpose I/O Function
GP91	30	I/O16tsh	General Purpose I/O Function
GP90	31	I/O16tsh	General Purpose I/O Function
GND	32	Ivss	Normal GND
GP87	33	I/O16tsh	General Purpose I/O Function
GP86	34	I/O16tsh	General Purpose I/O Function
GP85	35	I/O16tsh	General Purpose I/O Function
GP84 CIR_RX	36	I/O16tsh	General Purpose I/O Function Consumer Infrared Communication Receiver Function
GP83 CNTR1	37	I/O16tsh	General Purpose I/O Function Timer Y Signal
GP82 CNTR0	38	I/O16tsh	General Purpose I/O Function Timer X Signal
GP81 SCL2	39	I/O16tsh	General Purpose I/O Function SMBus 2 Clock Signal
SYMBOL	PIN	I/O	FUNCTION
GP80 SDA2	40	I/O16tsh	General Purpose I/O Function SMBus 2 Data Signal
GP77 SCL1	41	I/O16tsh	General Purpose I/O Function SMBus 1 Clock Signal
GP76 SDA1	42	I/O16tsh	General Purpose I/O Function SMBus 1 Data Signal
GP75 APS2_DAT	43	I/O16tsh	General Purpose I/O Function Auxiliary PS2 Data Signal
GP74 APS2_CLK	44	I/O16tsh	General Purpose I/O Function Auxiliary PS2 Clock Signal
GP73 MPS2_DAT	45	I/O16tsh	General Purpose I/O Function Mouse PS2 Data Signal

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP72 MPS2_CLK	46	I/O16tsh	General Purpose I/O Function Mouse PS2 Clock Signal
GP71 KPS2_DAT	47	I/O16tsh	General Purpose I/O Function Keyboard PS2 Data Signal
GP70 KPS2_CLK	48	I/O16tsh	General Purpose I/O Function Keyboard PS2 Clock Signal
VCC1	49	Ivdd	Normal Power Input, +3.3V
RESET#	50	I_{ts}	System Reset.
LCLK	51	Its	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	Its	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	Its	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O24ts	Serial IRQ input/Output.
GND	55	Ivss	Normal GND
LAD0	56	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LPWRSTS	60	Its	Power status. Indicates current power status of LPC interface.
GP47	61	I/O16tsh	General Purpose I/O Function
GP46 CLKRUN#	62	I/O16tsh	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O16tsh	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O16tsh	General Purpose I/O Function CPU reset output

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP43 TXD	65	I/O16tsh	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O16tsh	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O16tsh	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O16tsh	General Purpose I/O Function Fan tachometer 0
SYMBOL	PIN	I/O	FUNCTION
GND	69	Ivss	Normal GND
GP27 PWM3	70	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP24 PWM0	73	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
VCC1	78	Ivdd	Normal Power Input, +3.3V
GP17 KC15 FA15	79	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP16 KC14 FA14	80	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP15 KC13 FA13	81	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP14 KC12 FA12	82	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP13 KC11 FA11	83	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP12 KC10 FA10	84	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP11 KC9 FA9	85	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP10 KC8 FA8	86	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP07 KC7 FA7/FD7	87	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP06 KC6 FA6/FD6	88	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
SYMBOL	PIN	I/O	FUNCTION
GP05 KC5 FA5/FD5	89	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP04 KC4 FA4/FD4	90	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP03 KC3 FA3/FD3	91	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP02 KC2 FA2/FD2	92	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP01 KC1 FA1/FD1	93	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP00 KC0 FA0/FD0	94	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP37 KR7 CE#	95	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash chip select enable
GP36 KR6 OE#	96	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash output enable
GP35 KR5 WE#	97	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash write enable
GP34 KR4 ALE	98	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Address latch enable
GP33 KR3	99	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input
GP32 KR2	100	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP31 KR1	101	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input
GP30 KR0	102	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input
VREF	103	Ivdd	Analog Reference Voltage Input
GP67 AD7	104	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP66 AD6	105	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP65 AD5	106	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP64 AD4	107	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
SYMBOL	PIN	I/O	FUNCTION
GP63 AD3	108	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP62 AD2	109	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP61 AD1	110	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP60 AD0	111	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
AVCC	112	Ivdd	Analog Power Input, +3.3V
GP57 DA2	113	I/O12tsai	General Purpose I/O Function DA Converter Output
GP56 DA1	114	I/O12tsai	General Purpose I/O Function DA Converter Output
AGND	115	Ivss	Analog GND
GP55	116	I/O16tsh	General Purpose I/O Function
GP54	117	I/O16tsh	General Purpose I/O Function
GP53	118	I/O16tsh	General Purpose I/O Function
GP52	119	I/O16tsh	General Purpose I/O Function

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP51	120	I/O16tsh	General Purpose I/O Function
GP50	121	I/O16tsh	General Purpose I/O Function
XOUT	122	Oc	24MHz/12MHz System Clock Output
XIN	123	Ic	24MHz/12MHz System Clock Input
TEST#	124	I_{ts}	Test pin to provide different operation.
XCOUT	125	Oc	32.768 KHz Clock Output
XCIN	126	Ic	32.768 KHz Clock Input
GPC7 EXTINT37	127	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC6 EXTINT36	128	I/O16tsh	General Purpose I/O Function External Interrupt Input

5.2 RESET# & TEST# Part

Table 5-3 RESET# & TEST# pin configuration table

SYMBOL	PIN	I/O	FUNCTION
RESET#	50	I_{ts}	System Reset.
TEST#	124	I_{ts}	Test pin to provide different operation.

In W83L951DG/FG, RESET# Pin and TEST# Pin decide the status of W83L951DG/FG to provide 4 operations.

TEST#	RESET#	CHIP CURRENT STATUS
0	0	Internal Flash Access Interface Enable
0	1	Reserved
1	0	Normal Reset
1	1	Normal Operation

5.3 LPC Interface Part

LPC Interface is formed by LAD0~LAD3, SERIRQ, LRESET#, LFRAME#, LCLK and VCC2. These pins are defined by LPC interface Spec except VCC2. Below are descriptions about all LPC pins:

Table 5-4 LPC interface pin configuration table

SYMBOL	PIN	I/O	FUNCTION
LCLK	51	I_{ts}	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	I_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	I_{ts}	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O_{24ts}	Serial IRQ input/Output.
LAD0	56	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.

Note: Other pins about LPC interface, CLKRUN#: Please see “GP4” part.VCC2: Please see “power & clock” part.

5.4 GPIO0 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO0 and GPIOD0 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and other functions are disabled.

Table 5-5 GPIO0 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP07 KC7 FA7/FD7	87	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP06 KC6 FA6/FD6	88	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP05 KC5 FA5/FD5	89	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP04 KC4 FA4/FD4	90	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP03 KC3 FA3/FD3	91	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP02 KC2 FA2/FD2	92	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP01 KC1 FA1/FD1	93	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP00 KC0 FA0/FD0	94	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data

5.5 GPIO1 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO1 and GPIOD1 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and other functions are disabled.

Table 5-6 GPIO1 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP17 KC15 FA15	79	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP16 KC14 FA14	80	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP15 KC13 FA13	81	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP14 KC12 FA12	82	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP13 KC11 FA11	83	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP12 KC10 FA10	84	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP11 KC9 FA9	85	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP10 KC8 FA8	86	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

5.6 GPIO2 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO2 and GPIOD2 register to determine 8 input/output.

Pulse Width Modulator Output

Use Pulse Width Modulator Registers to control 4 Pulse Width Modulator Output.

Keyboard Matrix Column Output

Change the value of chip control 2 register bit 3 (Keyboard Scan Function Enable) to enable {GP0, GP1, GP20~23} keyboard scan function and GP3 key wakeup interrupt function.

Table 5-7 GPIO2 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP27 PWM3	70	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP24 PWM0	73	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output

5.7 GPIO3 Part

This part contains General Purpose I/O function, external flash interface, and keyboard matrix row input. Default function is General Purpose I/O function.

General Purpose I/O Function

Change the value of GPIO 3 data register (GPIO3) and GPIO 3 direction register (GPIOD3) to determine 8 input/output.

Keyboard Matrix Row Input

Change the value of chip control 2 register bit 3 (Keyboard Scan Function Enable) to enable GP3 key wakeup interrupt function.

Note: GPIO3 must be set as input when this function is enabled

The sample frequency about KEY Interrupt Mode is a system cycle, trigger for ' Low ' of input of GP3 and only take a sample once (unless input of GP3 return 'High', then enter 'low'). If signal debounce, then interrupt may request again.

Internal Flash Access Interface

GPIO30~33: Reserved (Must assign low)

Table 5-8 GPIO3 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP37 KR7 CE#	95	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash chip select enable
GP36 KR6 OE#	96	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash output enable
GP35 KR5 WE#	97	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash write enable
GP34 KR4 ALE	98	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Address latch enable
GP33 KR3	99	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP32 KR2	100	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP31 KR1	101	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP30 KR0	102	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input

5.8 GPIO4 Part

General Purpose I/O Function

Change the value of GPIO 4 data register (GPIO4) and GPIO 4 direction register (GPIOD4) to determine 8 input/output.

Universal Asynchronous Serial I/O Function

Change the value of chip control 1 register bit 3 (UART Function Enable) to enable Universal Asynchronous Serial I/O Function.

Hardware Keyboard Reset Function

Change the value of keyboard control register bit4 (Port 92 Enable) and bit3 (Hardware Keyboard Reset Control Enable) to enable Hardware Keyboard Reset Function.

Hardware Gate A20 Function

Change the value of keyboard control register bit4 (Port 92 Enable) and bit2 (Hardware Gate A20 Control Enable) to enable Hardware Gate A20 Function.

Table 5-9 GPIO4 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP47	61	I/O_{16tsh}	General Purpose I/O Function
GP46 CLKRUN#	62	I/O_{16tsh}	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O_{16tsh}	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O_{16tsh}	General Purpose I/O Function CPU reset output
GP43 TXD	65	I/O_{16tsh}	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O_{16tsh}	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 0

5.9 GPIO5 Part

General Purpose I/O Function

Change the value of GPIO 5 data register (GPIO5) and GPIO 5 direction register (GPIOD3) to determine 8 input/output.

D/A Converter Function

Change the value of chip control 2 register bit 7 (D/A 2 Function Enable) and Bit 6 (D/A 1 Function Enable) to enable D/A Converter Function.

Table 5-10 GPIO5 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP57 DA2	113	I/O_{12tsai}	General Purpose I/O Function DA2 Converter Output
GP56 DA1	114	I/O_{12tsai}	General Purpose I/O Function DA1 Converter Output
GP55	116	I/O_{16tsh}	General Purpose I/O Function
GP54	117	I/O_{16tsh}	General Purpose I/O Function
GP53	118	I/O_{16tsh}	General Purpose I/O Function
GP52	119	I/O_{16tsh}	General Purpose I/O Function
GP51	120	I/O_{16tsh}	General Purpose I/O Function
GP50	121	I/O_{16tsh}	General Purpose I/O Function

5.10 GPIO6 Part

General Purpose I/O Function

Change the value of GPIO 6 data register (GPIO6) and GPIO 6 direction register (GPIOD6) to determine 8 input/output.

A/D Converter Function

Change the value of chip control 2 register bit 5 (A/D Function Enable) to enable A/D Converter Function.

Table 5-11 GPIO6 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP67 AD7	104	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP66 AD6	105	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP65 AD5	106	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP64 AD4	107	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP63 AD3	108	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP62 AD2	109	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP61 AD1	110	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal
GP60 AD0	111	I/O_{12tsao}	General Purpose I/O Function A/D Converter Input Signal

5.11 GPIO7 Part

General Purpose I/O Function

Change the value of GPIO 7 data register (GPIO7) and GPIO 7 direction register (GPIOD7) to determine 8 input/output.

Keyboard PS2 Function Enable Function

Change the value of chip control 3 register bit 2 (Keyboard PS2 Function Enable) to enable Keyboard PS2 Function Enable Function.

Mouse PS2 Function Enable Function

Change the value of chip control 3 register bit 3 (Mouse PS2 Function Enable) to enable Mouse PS2 Function Enable Function.

Auxiliary PS2 Function Enable Function

Change the value of chip control 3 register bit 4 (Auxiliary PS2 Function Enable) to enable Auxiliary PS2 Function Enable Function.

SMBUS 1 Function

Change the value of chip control 3 register bit 0 (SMBUS 1 Function Enable) to enable SMBUS 1 Function.

Table 5-12 GPIO7 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP77 SCL1	41	I/O_{16tsh}	General Purpose I/O Function SMBus 1 Clock Signal
GP76 SDA1	42	I/O_{16tsh}	General Purpose I/O Function SMBus 1 Data Signal
GP75 APS2_DAT	43	I/O_{16tsh}	General Purpose I/O Function Auxiliary PS2 Data Signal
GP74 APS2_CLK	44	I/O_{16tsh}	General Purpose I/O Function Auxiliary PS2 Clock Signal
GP73 MPS2_DAT	45	I/O_{16tsh}	General Purpose I/O Function Mouse PS2 Data Signal
GP72 MPS2_CLK	46	I/O_{16tsh}	General Purpose I/O Function Mouse PS2 Clock Signal
GP71 KPS2_DAT	47	I/O_{16tsh}	General Purpose I/O Function Keyboard PS2 Data Signal
GP70 KPS2_CLK	48	I/O_{16tsh}	General Purpose I/O Function Keyboard PS2 Clock Signal

5.12 GPIO8 Part

General Purpose I/O Function

Change the value of GPIO 8 data register (GPIO8) and GPIO 8 direction register (GPIOD8) to determine 8 input/output.

Consumer Infrared Communications Receiver Function

Change the value of chip control 3 register bit 5 (CIR Function Enable) to enable Consumer Infrared Communications Receiver Function.

Wave Measurement Function

Change the value of timer X/Y mode register bit 5-4 and bit 1-0 to enable Wave Measurement Function.

SMBUS 2 Function

Change the value of chip control 2 register bit 1 (SMBUS 2 Function Enable) to enable SMBUS 2 Function.

Table 5-13 GPIO8 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP87	33	I/O_{16tsh}	General Purpose I/O Function
GP86	34	I/O_{16tsh}	General Purpose I/O Function
GP85	35	I/O_{16tsh}	General Purpose I/O Function
GP84 CIR_RX	36	I/O_{16tsh}	General Purpose I/O Function Consumer Infrared Communication Receiver Function
GP83 CNTR1	37	I/O_{16tsh}	General Purpose I/O Function Timer Y Signal
GP82 CNTR0	38	I/O_{16tsh}	General Purpose I/O Function Timer X Signal
GP81 SCL2	39	I/O_{16tsh}	General Purpose I/O Function SMBus 2 Clock Signal
GP80 SDA2	40	I/O_{16tsh}	General Purpose I/O Function SMBus 2 Data Signal

5.13 GPIO9 Part

General Purpose I/O Function

Change the value of GPIO 9 data register (GPIO9) and GPIO 9 direction register (GPIOD9) to determine 8 input/output.

Table 5-14 GPIO9 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP97	24	I/O_{16tsh}	General Purpose I/O Function
GP96	25	I/O_{16tsh}	General Purpose I/O Function
GP95	26	I/O_{16tsh}	General Purpose I/O Function
GP94	27	I/O_{16tsh}	General Purpose I/O Function
GP93	28	I/O_{16tsh}	General Purpose I/O Function
GP92	29	I/O_{16tsh}	General Purpose I/O Function
GP91	30	I/O_{16tsh}	General Purpose I/O Function
GP90	31	I/O_{16tsh}	General Purpose I/O Function

5.14 GPIOA Part

General Purpose I/O Function

Change the value of GPIO A data register (GPIOA) and GPIO A direction register (GPIODA) to determine 8 input/output.

External Interrupt Source Input Function

Change the value of external interrupt enable 1 register to determine External Interrupt.

Table 5-15 GPIOA pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GPA7 EXTINT17	15	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA6 EXTINT16	16	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA5 EXTINT15	17	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA4 EXTINT14	18	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA3 EXTINT13	19	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA2 EXTINT12	20	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA1 EXTINT11	21	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPA0 EXTINT10	22	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

5.15 GPIOB Part

General Purpose I/O Function

Change the value of GPIO B data register (GPIOB) and GPIO B direction register (GPIODB) to determine 8 input/output.

External Interrupt Source Input Function

Change the value of external interrupt enable 2 register to determine External Interrupt.

Table 5-16 GPIOB pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GPB7 EXTINT27	7	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB6 EXTINT26	8	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB5 EXTINT25	9	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB4 EXTINT24	10	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB3 EXTINT23	11	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB2 EXTINT22	12	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB1 EXTINT21	13	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPB0 EXTINT20	14	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

5.16 GPIOC Part

General Purpose I/O Function

Change the value of GPIO C data register (GPIOC) and GPIO C direction register (GPIODC) to determine 8 input/output.

External Interrupt Source Input Function

Change the value of external interrupt enable 3 register to determine External Interrupt.

Table 5-17 GPIOC pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GPC7 EXTINT37	127	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC6 EXTINT36	128	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC5 EXTINT35	1	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC4 EXTINT34	2	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC3 EXTINT33	3	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC2 EXTINT32	4	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC1 EXTINT31	5	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input
GPC0 EXTINT30	6	I/O_{16tsh}	General Purpose I/O Function External Interrupt Input

5.17 Power & Clock Part

Table 5-18 Power & clock pin configuration table

SYMBOL	PIN	I/O	FUNCTION
XOUT	122	O_c	24MHz/12MHz System Clock Output
XIN	123	I_c	24MHz/12MHz System Clock Input
XCOUT	125	O_c	32.768 KHz Clock Output
XCIN	126	I_c	32.768 KHz Clock Input
VCC1	23 49 78	I_{vdd}	Normal Power Input, +3.3V
VCC2	60	I_{ts}	Power status. Indicates current power status of LPC interface.
GND	32 55 69	I_{vss}	Normal GND
AVCC	112	I_{vdd}	Analog Power Input, +3.3V
AGND	115	I_{vss}	Analog GND
VREF	103	I_{vdd}	Analog Reference Voltage Input

6. FUNCTIONAL DESCRIPTION

In W83L951DG/FG, memory organization and data type are based on Turbo 51 core controller. Register sets of various function blocks are finished by accessing Special Function Register (SFR).

According to the difference of accessing approaches, SFR are divided into Address Mapping and External RAM Address Mapping.

Internal RAM Address Mapping:

It means to use direct addressing to access 128 bytes from internal RAM address 80H to 0FFH. Function blocks that use Internal RAM Address Mapping are listed below:

Table 6-1 Reset Source Table

NAME	RESET SOURCE
8051 Core	System Reset.
Internal Interrupt Controller	System Reset
PS2 Device Interface	System Reset + PS2 Reset
Low Pin Count Interface Controller	System Reset + LPC Power Fail + LPC Reset
SMBus 1	System Reset + SMBUS1 Reset
SMBus 2	System Reset + SMBUS2Reset
GPIO Controller	System Reset.

Table 6-2 Internal RAM Address Mapping Table

Base on 00h	Index							
Offset	**0**	**1**	**2**	**3**	**4**		**6**	**7**
80	+GP0	SP	DPL1	DPH1	DPL2	DPH2	ID	VERSION
88	+GP1	CHIPCTRL1	CHIPCTRL2	CHIPCTRL3	DPSEL	INTEN	MMEN	
90	+GP2	KBCCON	LPCCON	DBB0STS	DBB0	DBB0ADDH	DBB0ADDL	SIRQ0
98	+GP3	DBB1STS	DBB1	DBB1ADDH	DBB1ADDL	SIRQ1		
A0	+GP4	KPS2DATA	KPS2CON	KPS2STS	MPS2DATA	MPS2CON	MPS2STS	PS2HSEN
A8	+GP5	APS2DATA	APS2CON	APS2STS				
B0	+GP6	S1CR	S1IREQ	S1IE	S1FIFOCON	S1MFIFO	S1MCON	S1MSTS
B8	+GP7	S1MFIFOSTS	S1SFIFO	S1SCON	S1SSTS	S1SFIFOSTS		
C0	+GP8	S2CR	S2IREQ	S2IE	S2FIFOCON	S2MFIFO	S2MCON	S2MSTS
C8	+GP9	S2MFIFOSTS	S2SFIFO	S2SCON	S2SSTS	S2SFIFOSTS		
D0	+PSW	GPD0	GPD1	GPD2	GPD3	GPD4	GPD5	GPD6
D8	+GPA	GPD7	GPD8	GPD9	GPDA	GPDB	GPDC	
E0	+ACC	IE1	IE2	IE3	IE4			
E8	+GPB	IREQ1	IREQ2	IREQ3	IREQ4			
F0	+B	IP1	IP2	IP3	IP4			
F8	+GPC	FCON	FADDH	FADDL	FDATA			
Index + 8	8	9	A	B	C		E	F

Read Only Reserved + a bit addressable register

External RAM Address Mapping:

It means to use MOVX to access 256 bytes from external RAM addressing FF00H~FFFFH.

Function blocks that use External RAM Address Mapping are listed below:

Table 6-3 Reset Source Table

NAME	RESET SOURCE
Watch Dog Block	System Reset + WDT Reset
Timer Block	System Reset
PWM1/2/3/4 Block	System Reset + PWM1/2/3/4 Reset
Serial I/O Block	System Reset + SIO Reset
CIR Block	System Reset + CIR Reset
AD Convert Block	System Reset + AD Reset
DA Convert Block	System Reset + DA Reset
External Interrupt Block	System Reset + System Reset.
FAN Block	System Reset + FAN Reset
RTC Block	System Reset + RTC Reset

Table 6-4 External RAM Address Mapping Table

Base FF00h	**Index**							
Offset	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
00h	WDTCON	WDTSTS						
08h								
10h	PRE1	T1	PRE2	T2				
18h	TM	PREX	TX	PREY	TY			
20h	PWMCON	PWM1P	PWM1H	PWM2P	PWM2H	PWM3PL	PWM3PH	PWM3HL
28h	PWM3HH	PWM4PL	PWM4PH	PWM4HL	PWM4HH			
30h	UARTCON	UARTSTS	BRGH	BRGL	UARTBUF			
38h								
40h	CIR	BRD	CIRFIFO					
48h								
50h	AD1	AD2	DA1	DA2				
58h								
60h	FAN1	FAN2						
68h								
70H	RTCSEC	RTCSECAL	RTCMIN	RTCMINAL	RTCHR	RTCHRAL		
78H								
80H	EIE1	EIE2	EIE3	EIREQ1	EIREQ2	EIREQ3		
88H	EINTT1	EINTT2	EINTT3	EINTT4				
Index +	8	9	A	B	C	D	E	F

Read Only Reserved

6.1 Turbo 8051 Core Block

The Turbo 8051 is fully instruction compatible. It features a faster running and better performance. It improves the performance not just by running at high frequency but also reduces the machine cycle duration from the standard 8051 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. The Turbo 8051 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers.

In W83L951DG/FG, External Wakeup Source will only be controlled by external wakeup configure register, not be influenced by internal interrupt configuration, even relevant interrupt enable or global interrupt enable have not been set, can carry out action of wakeup chip equally.

Table 6-5 8051 Configure Register Define

8051 Configure Register (12)									
IntAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D0	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0	ACC	Accumulator [7:0]							
F0	B	B[7:0]							
81	SP	Stack Pointer [7:0]							
82	DPL1	Data Pointer 1 [7:0]							
83	DPH1	Data Pointer 1 [15:8]							
84	DPL2	Data Pointer 2 [7:0]							
85	DPH2	Data Pointer 2 [15:8]							
86	ID	Device ID Register							
87	REV	Device Revised Version Register							
8C	DPSEL								DPS
8D	INTEN								INTEN
8E	MMC								MMEN
89	CHIPCTRL1	PWM4EN	PWM3EN	PWM2EN	PWM1EN	UARTEN	ALPCEN	Clock Select	
8A	CHIPCTRL2	D/AEN2	D/AEN1	A/DEN	RTCEN	KEYEN	WDTEN	PD	IDLE
8B	CHIPCTRL3	FAN2EN	FAN1EN	CIREN	APS2	MPS2	KPS2	SM2EN	SM1EN

Table 6-6 External Wakeup Configure Register Define

POWER DOWN CONFIGURE REGISTER									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
8C	EXTWKP1	Reserved				KEY	EXTINT3	EXTINT2	EXTINT1
8D	EXTWKP2	Reserved			RTC	LPC	APS2	MPS2	KPS2

6.1.1 Register Description

6.1.1.1 Program Status Word Register (PSW) (Default Value: 0000_0000)

Bit7: Carry Flag (CY):

Set for an arithmetic operation, which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.

Bit6: Auxiliary Carry (AC):

Set when the previous operation resulted in a carry (during addition) or borrow (during subtraction) from the high order nibble.

Bit5: User Flag 0 (F0):

General-purpose flag can be set or cleared by the user by software.

Bit4~3: Register bank selects bits (RS1, RS0):

RS1	RS0	Register bank	Address Range
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Bit2: Overflow Flag (OV):

Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation or vice-versa.

Bit1: User Flag 1 (F1):

General-purpose flag that can be set or cleared by the user by software

Bit0: Parity flag (P):

Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Please refer to MCS-8051 define in detail.

6.1.1.2 Accumulator Register (ACC) (Default Value: 0000_0000)

Bit7~0: Accumulator (A)

The A or ACC register is the standard 8032 accumulator. Please refer to MCS-8051 define in detail.

6.1.1.3 B Register (B) (Default Value: 0000_0000)

Bit7~0: B

The B register is the standard 8032 accumulator. Please refer to MCS-8051 define in detail.

6.1.1.4 Stack Pointer Register (SP) (Default Value: 0000_0111)

Bit7~0: Stack Pointer

The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack. Note: The address range is 00h~FFh.

Please refer to MCS-8051 define in detail.

6.1.1.5 Data Pointer 1 High Byte Register (DPH1) (Default Value: 0000_0000)

This is the high byte of the standard 8032 16-bit data pointer.

6.1.1.6 Data Pointer 1 Low Byte Register (DPL1) (Default Value: 0000_0000)

This is the low byte of the standard 8032 16-bit data pointer.

6.1.1.7 Data Pointer 2 High Byte Register (DPH2) (Default Value: 0000_0000)

Same as Data Pointer 1 High Byte Register, it is selected by DPSEL@DPS.

6.1.1.8 Data Pointer 2 Low Byte Register (DPL1) (Default Value: 0000_0000)

Same as Data Pointer 1 High Byte Register, it is selected by DPSEL@DPS.

6.1.1.9 Device ID Register (ID) (Default Value: 0001_0010)

Device ID Number = 12h.

6.1.1.10 Revised Version Register (REV) (Default Value: 0000_0000)

Version Number = 00h

6.1.1.11 Data Pointer Select Register (DPSEL) (Default Value: 0000_0000)

Bit7~1: Reserved

Bit0: Select Data Pointer 1/2 Register (Default Value: 0)

1: Data Pointer 2 Register

0: Data Pointer 1 Register

6.1.1.12 All Interrupt Enable Register (INTEN) (Default Value: 0000_0000)

Bit7~1: Reserved

Bit0: Enable 8051 All Interrupt Procedure

1: Enable 8051 All Interrupt Procedure

0: Disable

6.1.1.13 Memory Mapping Control Register (MMC) (Default Value: 0000_0000)

Bit7~1: Reserved

Bit0: Enable Memory Mapping

1: Enable, 0000~07FFh (Address) based on Data Address Map to F800~FFFFh based on Code Address.

0: Disable

6.1.1.14 Chip Control 1 Register (CHIPCTRL1) (Default Value: 0000_0000)

Bit 7: Pulse Width Modulator 4 Function Enable

1: Enable Pulse Width Modulator 4 (GP27 GPIO Function Disable)

0: Power down Pulse Width Modulator 4

Bit 6: Pulse Width Modulator 3 Function Enable

1: Enable Pulse Width Modulator 3 (GP26 GPIO Function Disable)

0: Power down Pulse Width Modulator 3

Bit 5: Pulse Width Modulator 2 Function Enable

1: Enable Pulse Width Modulator 2 (GP25 GPIO Function Disable)

0: Power down Pulse Width Modulator 2

Bit 4: Pulse Width Modulator 1 Function Enable

1: Enable Pulse Width Modulator 1 (GP24 GPIO Function Disable)

0: Power down Pulse Width Modulator 1

Bit 3: UART Function Enable

1: Enable UART Block (GP42、GP43 GPIO Function Disable)

0: Power down UART Block

Bit 2: Advance LPC Function Enable

1: Enable CLKRUN# Function. (GP46 GPIO Function Disable)

0: Disable

Bit 1~0: System Clock Select

00: Input Clock, 01: Input Clock, 10: Input Clock/2, 11: Input Clock/4

6.1.1.15 Chip Control 2 Register (CHIPCTRL2) (Default Value: 0000_0000)

Bit 7: D/A 2 Function Enable

1: Enable DAC2 Block (GP56 GPIO Function Disable)

0: Power down DAC2 Block

Bit 6: D/A 1 Function Enable

1: Enable DAC1 Block (GP57 GPIO Function Disable)

0: Power down DAC1 Block

Bit 5: A/D Function Enable

1: Enable ADC Block (GP6 GPIO Function Disable)

0: Power down ADC Block

Bit 4: Real Time Clock Function Enable

1: Enable RTC Block

0: Power down RTC Block

Bit 3: Keyboard Scan Function Enable

1: Enable {GP0, GP1, GP20~23} Keyboard Scan Function and GP3 Key Wakeup Interrupt Function.

0: Disable

Note: To enable Keyboard Scan Function will switch {GP0, GP1, GP20~23} drive current from 12mA to 250uA.

Bit 2: Watch Dog Timer Function Enable

1: Enable WDT Block

0: Power down WDT Block

Bit 1: Whole Chip Power down Enable

1: Power down mode:

When there is no any external interrupt, Key Wake-up interrupt and LPC interrupt occurs or PS2 data line is low , W83L951DG/FG will stop external clock to enter power down mode, otherwise it will clear this bit as 0 automatically.

0: Normal Mode:

When any external interrupt or Key Wake-up interrupt occurs or PS2 data line goes low, this bit will clear this bit as 0 automatically.

Note: If whole chip power down mode and idle mode are both enabled, after leaving power down mode, W83L951DG/FG will enter idle mode to wait for internal interrupt.

Bit 0: Whole Chip Idle Enable

1: Idle Mode:

When there is no any interrupt occurs, W83L951DG/FG will enter idle mode, otherwise it will clear this bit as 0 automatically.

0: Normal Mode:

It will clear this bit as 0 when all interrupt events occur.

6.1.1.16 Chip Control 3 Register (CHIPCTRL3) (Default Value: 0000_0000)

Bit 7: FAN 2 Function Enable

1: Enable FAN1 Block (GP40 GPIO Function Disable)

0: Power down FAN1 Block

Bit 6: FAN 1 Function Enable

1: Enable FAN2 Block (GP41 GPIO Function Disable)

0: Power down FAN2 Block

Bit 5: CIR Function Enable

1: Enable CIR Block (GP84 GPIO Function Disable)

0: Power down CIR Block

Bit 4: Auxiliary PS2 Function Enable

1: Enable Auxiliary PS2 Block (GP70、GP71 GPIO Function Disable)

0: Power down Auxiliary PS2 Block (The Wakeup by APS2 is also disabled)

Bit 3: Mouse PS2 Function Enable

1: Enable Mouse PS2 Block (GP72、GP73 GPIO Function Disable)

0: Power down Mouse PS2 Block (The Wakeup by MPS2 is also disabled)

Bit 2: Keyboard PS2 Function Enable

1: Enable Keyboard PS2 Block (GP70、GP71 GPIO Function Disable)

0: Power down Keyboard PS2 Block (The Wakeup by KPS2 is also disabled)

Bit 1: SMBUS 2 Function Enable

1: Enable SMBUS2 Block (GP80、GP81 GPIO Function Disable)

0: Power down SMBUS2 Block

Bit 0: SMBUS 1 Function Enable

1: Enable SMBUS1 Block (GP76、GP77 GPIO Function Disable)

0: Power down SMBUS1 Block

6.1.1.17 External Wake-up 1 Register (EXTWKP1) (Default Value: 0000_0000)

Bit7~4: Reserved

Bit3: Enable Key Wake-up Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit2: Enable External Interrupt 3 wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit1: Enable External Interrupt 2 wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit0: Enable External Interrupt 1 wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

6.1.1.18 External Wake-up 2 Register (EXTWKP2) (Default Value: 0000_0000)

Bit7~5: Reserved

Bit4: Enable RTC Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit3: Enable LPC Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Bit2: Enable APS2 Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Auxiliary PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

Bit1: Enable MPS2 Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Mouse PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

Bit0: Enable KPS2 Interrupt wake-up W83L951DG/FG at power down mode.

1: Enable.

0: Disable.

Note: Before enabling the function, Keyboard PS2 Noise Filter Enable Bit (NFEN@PS2CON) must be set low.

6.2 Low Pin Count Interface Block

Table 6-7 Low Pin Count Interface Register Define

LOW PIN COUNT INTERFACE(LPC) & SERIAL IRQ & DATA BUFFER BLOCK(10)									
INTA DDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
91	KBCCON	Reserved			P92EN	HKBEN	HGAEN	GA20SET	GA20CLR
92	LPCCON	DBB1En	DBB0En	SIRQ11EN	SIRQ10EN	SIRQ01EN	SIRQ00EN	SIRQ1GEN	SIRQ0GEN
93	DBB0STS	UDF[3:0]				CD0	UDF	IBF0	OBF0
94	DBB0	Data Buffer 0 [7:0]							
95	DBB0ADDH	Data Buffer 0 Address High Byte							
96	DBB0ADDL	Data Buffer 0 Address Low Byte							
97	SIRQ0	OBF01 SIRQ Number				OBF00 SIRQ Number			
99	DBB1STS	UDF[3:0]				CD1	UDF	IBF1	OBF1
9A	DBB1	Data Buffer 1 [7:0]							
9B	DBB1ADDH	Data Buffer 1 Address High Byte							
9C	DBB1ADDL	Data Buffer 1 Address Low Byte							
9D	SIRQ1	OBF11 SIRQ Number				OBF10 SIRQ Number			

Gray: Only with System Reset to initial.

6.2.1 Register Description

6.2.1.1 DBB0 Status Register (DBB0STS) (Default Value: 0000_?0?0)

Bit7~4: User Define Flag

Bit3: Indicate IDBB0 Command/Data (By LRESET_N Pin to reset)

1: Command, 0: Data.

Bit2: User Define Flag

Bit1: Input Buffer Full Flag (By LRESET_N Pin to reset)

1: Full, 0: Empty

Bit0: Output Buffer Full Flag

1: Full, 0: Empty

6.2.1.2 Data Bus Buffer 0 Register (DBB0) (Default Value: 0000_0000)

Write data to output buffer, and read data from input buffer.

6.2.1.3 Data Bus Buffer 0 Address High Byte Register (DBB0ADDH) (Default Value: 0000_0000)

DBB0 address is according to {DBB0ADDH, DBB0ADDL}. Default I/O address is 0x00h.

If transmission is proceeding, address is encoded and decoded in next package.

6.2.1.4 Data Bus Buffer 0 Address Low Byte Register (DBB0ADDL) (Default Value: 0000_0000)

DBB0 address is according to {DBB0ADDH, DBB0ADDL}. Default I/O address is 0x00h.

If transmission is proceeding, address is encoded and decoded in next package.

6.2.1.5 Low Pin Count Control Register (LPCCON) (Default Value: 0000_0000)

Bit7: Data Bus Buffer 1 Enable

1: Enable (If transmission is proceeding, address is encoded and decoded in next package.)

0: Disable

Bit6: Data Bus Buffer 0 Enable

1: Enable (If transmission is proceeding, address is encoded and decoded in next package.)

0: Disable

Bit5: Serial IRQ 11 Enable

1: Enable (Start generating Serial IRQ for OBF1)

0: Disable (Stop generating Serial IRQ for OBF1)

Bit4: Serial IRQ 10 Enable

1: Enable (Start generating Serial IRQ for OBF1)

0: Disable (Stop generating Serial IRQ for OBF1)

Bit3: Serial IRQ 01 Enable

1: Enable (Start generating Serial IRQ for OBF0)

0: Disable (Stop generating Serial IRQ for OBF0)

Bit2: Serial IRQ 00 Enable

1: Enable (Start generating Serial IRQ for OBF0)

0: Disable (Stop generating Serial IRQ for OBF0)

Bit1: Serial IRQ 1 Generate Start Bit

W83L951DG/FG hardware checks this bit in every starting of Serial IRQ procedure. If this bit is high, W83L951DG/FG will generate Serial IRQ corresponding to OBF1 SIRQ Number @SIRQ. This bit clears as low automatically after W83L951DG/FG receives request and enters Serial IRQ procedure. This bit is set as high in writing this bit and data is written to Data Bus Buffer 1 Register.

This bit is to provide the method to generate Serial IRQ that is needless through writing to Data Bus Buffer 1 Register.

Bit0: Serial IRQ 0 Generate Start Bit

W83L951DG/FG hardware checks this bit in every starting of Serial IRQ procedure. If this bit is high, W83L951DG/FG will generate Serial IRQ corresponding to OBF0 SIRQ Number @SIRQ. This bit clears as low automatically after W83L951DG/FG receives request and enters Serial IRQ procedure. This bit is set as high in writing this bit and data is written to Data Bus Buffer 0 Register.

This bit is to provide the method to generate Serial IRQ that is needless through writing to Data Bus Buffer 0 Register.

6.2.1.6 Serial IRQ 0 Number (SIRQ0) (Default Value: 0000_0000)

Bit7~4: Serial IRQ 01 Number

If transmission is proceeding, IRQ number will be changed in next transmission. Set as 0000, SIRQ01 is disabled.

Bit3~0: Serial IRQ 00 Number

If transmission is proceeding, IRQ number will be changed in next transmission. Set as 0000, SIRQ00 is disabled.

6.2.1.7 Serial IRQ 1 Number (SIRQ1) (Default Value: 0000_0000)

Bit7~4: Serial IRQ 11 Number

If transmission is proceeding, IRQ number will be changed in next transmission. Set as 0000, SIRQ11 is disabled.

Bit3~0: Serial IRQ 10 Number

If transmission is proceeding, IRQ number will be changed in next transmission. Set as 0000, SIRQ10 is disabled.

6.2.1.8 Keyboard Control Register (KBCCON)(Default Value: 0000_0001)

Bit7~5: Serial IRQ Hold Counter for Serial IRQ Generate Function

000: Generate 1 cycle of Serial IRQ.

001: Generate 2 cycles of Serial IRQ.

010: Generate 3 cycles of Serial IRQ.

011: Generate 4 cycles of Serial IRQ.

100: Generate 5 cycles of Serial IRQ.

101: Generate 6 cycles of Serial IRQ.

110: Generate 7 cycles of Serial IRQ.

111: Generate 8 cycles of Serial IRQ.

Bit4: Port 92 Enable (Default Value: 0)

1: Enable W83L951DG/FG's hardware logic to receive the data written in I/O address@0092h. Bit1 and bit0 of port92 control register controls Gate A20 and KBRST pin. Gate A20 will drive high when bit1 is 1 and KBRESET pin drive {14us High → 6us Low → High} waveform when bit0 is 1. Gate A20 is default high level after LPC reset and GP44, GP45 GPIO function is disabled.

0: Disable

Bit3: Hardware Keyboard Reset Control Enable (Default Value: 0)

1: Enable W83L951DG/FG's hardware logic to set KBRESET. When the KBC receives data that follows a "FE" command, the KBRESET pin drives {14us High → 6us Low → High} waveform. And GP44 GPIO function is disabled.

0: Disable

Bit2: Hardware Gate A20 Control Enable (Default Value: 0)

1: Enable W83L951DG/FG's hardware logic to set Gate A20. When the KBC receives data that follows a "D1" command, the Gate A20 pin drives high. And GP45 GPIO function is disabled.

0: Disable

Bit1: Gate A20 Set

Set directly Gate A20 Output Register. If host is setting from LPC Interface, the request will be ignored. This belongs to software control.

Bit0: Gate A20 Clear/Gate A20 Status

Write: Clear directly Gate A20 Output Register. If host is setting from LPC Interface, the request will be ignored. This belongs to software control.

Read: Current Internal Gate A20 Status.

6.2.1.9 DBB1 Status Register (DBB1STS) (Default Value: 0000_?0?0)

Bit7~4: User Define Flag

Bit3: Indicate IDBB Command/Data (By LRESET# Pin to reset)

1: Command, 0: Data.

Bit2: User Define Flag

Bit1: Input Buffer Full Flag (By LRESET# Pin to reset)

1: Full, 0: Empty

Bit0: Output Buffer Full Flag

1: Full, 0: Empty

6.2.1.10 Data Bus Buffer 1 Register (DBB1) (Default Value: 0000_0000)

The output buffer register and the input buffer register are located at the same address. The output buffer is write-only and the input buffer is read-only.

6.2.1.11 Data Bus Buffer 1 Address High Byte Register (DBB1ADDH) (Default Value: 0000_0000)

DBB1 address is according to {DBB1ADDH, DBB1ADDL}. Default I/O address is 0x00h. If transmission is proceeding, address will be encoded and decoded in next package, not in current package.

6.2.1.12 Data Bus Buffer 1 Address Low Byte Register (DBB1ADDL) (Default Value: 0000_0000)

DBB1 address is according to {DBB1ADDH, DBB1ADDL}. Default I/O address is 0x00h. If transmission is proceeding, address will be encoded and decoded in next package, not in current package.

6.3 Personal System 2 Block

The Winbond Keyboard controller has three independent PS/2 serial ports implemented in hardware, which are directly controlled by the on chip 8051. Each of the three PS/2 serial channels uses a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has two signal lines: Clock and Data. Both signal lines are bi-directional and employ open drain. The PS2DATA, PS2CON and PS2STS is defined individually for each PS/2 channel. PS2HSEN is only one register for controlling all PS/2 device handshake action.

Table 6-8 Personal System 2(PS2) Register Define

KEYBOARD & MOUSE & AUXILIARY PS2 BLOCK(9)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A1	KPS2DATA	KPS2 Data register [7:0]							
A2	KPS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	KPS2T/R
A3	KPS2STS	KPS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY
A4	MPS2DATA	MPS2 Data register [7:0]							
A5	MPS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	MPS2T/R
A6	MPS2STS	MPS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY
A7	PS2HSEN	Reserved							HSEN
A9	APS2DATA	APS2 Data register [7:0]							
AA	APS2CON	NFEN	Inhibit	STOP		PARITY		Reserved	APS2T/R
AB	APS2STS	APS2BUSY	START_DEC	TTIMEOUT	XMIT_BUSY	FE	PE	RTIMEOUT	RDAT_RDY

Gray: Only with System Reset to initial.

6.3.1 Register Description

6.3.1.1 PS/2 Handshake Enable Register (PS2HSEN) (Default Value:: 0000_0000)

Bit 7~1: Reserved (always return 'LOW')

Bit 0: Handshake Mode Enable (HSEN)

0: The handshake mode of PS2 disables.

1: The handshake mode of PS2 enables.

When the handshake mode of PS2 is enabling, the TR bit (BIT 0) of PSCON is automatically set high when the START_DEC bit (bit 6) of PS2STS of the other channel is set.

Note:

The priority of three PS2 interface is KPS2 > MPS2 > APS2.

Whether the handshake mode of PS2 is enabling or no, the TR bit (BIT 0) of PSCON is automatically set high when the RDATA_RDY bit (bit 0) of PS2STS of this channel is set.

6.3.1.2 PS/2 T/R DATA Registers (PS2DATA) (Default Value: 1111_1111)

Transmit:

The byte written to this register, when PS2_T/R = 1 and PS2_EN = 1 and XMIT_BUSY = 0, is transmitted automatically by the PS/2 channel control logic. On successful start of this transmission, the PS2 logic will automatic set XMIT_BUSY to high. If PS2_T/R = 0 or PS2_EN = 0 or XMIT_BUSY = 1, then writes to this register are ignored.

On successful completion of this transmission or upon a Transmit Time-out condition the PS2_T/R and XMIT_BUSY bit is automatically set to low. The PS2_T/R bit must be written to a HIGH before initiating another transmission to the remote device.

Note:

Even if PS2_T/R = 1 and PS2_EN = 1 and XMIT_BUSY = 0, writing the transmit Register will hold the current transmission if RDATA_RDY is set. The automatic PS2 logic forces data to be read from the Receive Register before allowing a transmission.

An interrupt is generated on the high to low transition of XMIT_BUSY.

All bits of this register are write-only for transmit data, because you always read received data.

Receive:

When PS2_EN=1 and PS2_T/R=0, the PS2 Channel is set to automatically receive data on that channel (both the CLK and DATA lines will float waiting for the peripheral to initiate a reception by sending a start bit followed by the data bits). After a successful reception data is placed in this register and the RDATA_RDY bit is set and the CLK line is forced low by the PS2 channel logic. RDATA_RDY is cleared and the CLK line is released to hi-z following a read of this register. This automatically holds off further receive transfers until the 8051 has had a chance to get the data.

Note:

The Receive Register is initialized to 0xFF after a Timeout has occurred.

The channel can be enabled to automatically transmit data (PS2_EN=1) by setting PS2_T/R while RDATA_RDY is set, however a device (not include host) transmission can hold until the data has been read from the Receive Register.

An interrupt is generated on the low to high transition of RDATA_RDY.

If a receive timeout (REC_TIMEOUT=1) or a transmit timeout (XMIT_TIMEOUT =1) occurs the channel is busied (CLK held low) for 300us(Input clock=24MHz) or 600us(Input clock=12MHz) (Hold Time) to guarantee that the peripheral aborts. Writing to the Transmit Register will be allowed; however the data written will not be transmitted until the Hold Time expires.

In the foregoing situation, RDATA_RDY won't automatically clear.

6.3.1.3 PS/2 Control Registers (PS2CON) (Default Value:: 0000_0000)

Bit 7: NOISE FILTER ENABLE (NFEN)

0: Disable noise filter for clock line

1: Enable noise filter for clock line

Bit 6: Inhibit bit

The low to high transition of the inhibit bit will hold the clock line low for 100us(Input clock=24MHz) or 200us(Input clock=12MHz).

Bit 5-4: STOP

Bits [5:4] of the Control Register are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [5:4] =

00: Receiver expects an active high stop bit.

01: Receiver expects an active low stop bit.

10: Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).

11: Reserved.

Bit 3-2: PARITY

Bits [3:2] of the Control Register are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits [3:2] =

00: Receiver expects Odd Parity (Default Value:).

01: Receiver expects Even Parity.

10: Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).

11: Reserved.

Bit 1: PS2_EN PS2 Channel Enable

When PS2_EN=1 the PS/2 State machine is enabled allowing the channel to perform automatic reception or transmission depending on the bit value of PS2_T/R. When PS2_EN = 0, the channel's automatic PS/2 state machine is disabled.

Note:

If the PS2_EN bit is cleared prior to the rising edge of the 10th (parity bit) clock edge the receive data is discarded (RDATA_RDY remains low).

If the PS2_EN bit is cleared following the rising edge of the 10th clock signal then the receive data is saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

In the foregoing two situations, ps2 device can't differentiate host receive data success or fail, and therefore we don't recommend to use this function. It shall set to high before you start any operation of PS2.

Bit 0: PS2_T/R PS/2 Channel Transmit/Receive

This bit is only valid when PS2_EN=1 and sets the PS2 logic for automatic transmission or reception when PS2_T/R equals HIGH or LOW respectively (This bit may be modified, after unsetting PS2_EN).

When set the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation this bit must be set prior to writing to the Transmit Register; writes are blocked to the Transmit Register when this bit is not set.

Upon setting the PS2_T/R bit the channel will drive its CLK line low and then float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS2_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. KB controller drives the data line low and, within 100us, floats the clock line (externally pulled high by the pull-up resistor) to signal to the external PS/2 device that data is now available.

The PS2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Timeout error condition occurs.

Note: If the PS2_T/R bit is set while the channel is actively receiving data prior to the rising edge of the 10th (parity bit) clock edge the receive data is discarded. If this bit is not set prior to the 10th clock signal then the receive data is saved in the Receive Register.

When the PS2_T/R bit is cleared the PS/2 channel is enabled to receive data. Upon clearing this bit, whether RDATA_RDY=0 or no, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission for receiving data. But if RDATA_RDY=1, the hardware won't generate interrupt to indicate finished receive data.

If the PS2_T/R bit is set while RDATA_RDY=1 then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

6.3.1.4 PS/2 Status Registers (PS2STS) (Default Value:: 0000_0000)

Bit 7: Receiver Busy (RX_BUSY)

This bit is indicators for each of the three PS/2 Channels. When a RX_BUSY bit is set the associated channel is actively receiving PS/2 data; when a RX_BUSY bit is clear the channel is idle.

Bit 6: Start Bit Detect (START_DEC)

This bit is set on detecting start bit of receive conditions. Writing high will clear this bit.

Bit 5: Transmitter Timeout (XMIT_TIMEOUT)

This bit is set on one of 3 transmit conditions, and in addition the channel's CLK line is automatically pulled low and held for a period of 300us(Input clock=24MHz) or 600us(Input clock=12MHz) following assertion of the XMIT_TIMEOUT bit during which time the PS2_T/R is also held low:

When the transmitter bit time (time between falling edges) exceeds 300us(Input clock=24MHz) or 600us(Input clock=12MHz).

When the transmitter start bit is not received within 25ms(Input clock=24MHz) or 50ms(Input clock=12MHz) from signaling a transmit start event.

If the time from the 1st (start, falling edge) bit to the 11th (stop, falling edge) bit exceeds 2ms.

Writing high will clear this bit.

Bit 4: Transmitter Busy (XMIT_BUSY)

When high, the XMIT_BUSY bit is a status bit indicating that the PS2 channel is actively transmitting data to the PS2 peripheral device. Writing to the Transmit Register whether the channel ready to transmit will cause the XMIT_BUSY bit to assert and remain asserted until one of the following conditions occur and an Interrupt is generated..

The falling edge of the 11th CLK; upon a Transmit Timeout condition (XMIT_TIMEOUT goes high);

Upon the PS2_T/R bit being written to 0.

Upon the PS2_EN bit being written to 0.

Note: An interrupt is generated on the high to low transition of XMIT_BUSY.

Bit 3: Framing Error (FE)

When receiving data the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel has been set to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an Interrupt is generated. Writing high will clear this bit.

Bit 2: Parity Error (PE)

When receiving data the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel has been set to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an Interrupt is generated. Writing high will clear this bit.

Bit 1: Receiver Timeout (REC_TIMEOUT)

Under PS2 automatic operation, PS2_EN=1, this bit is set on one of 4 receive error conditions, and in addition the Channel's CLK line is automatically pulled low and held for a period of 300us following assertion of the REC_TIMEOUT bit:

When the receiver bit time (time between falling edges) exceeds 300us(Input clock=24MHz) or 600us(Input clock=12MHz).

If the time from the 1st (start, falling edge) bit to the 10th (stop, falling edge) bit exceeds 2ms.

On a receive parity error along with the parity error (PE) bit.

On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit. Writing high will clear this bit.

Note: An Interrupt is generated on the low to high transition of the REC_TIMEOUT bit.

Bit 0: Data Ready (RDATA_RDY)

Receive Data Ready: Under normal operating conditions, this bit is set following the falling edge of the 11th clock given successful reception of a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive timeout errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS2_EN bit is cleared following the 10th CLK edge (see the PS2_EN bit description for further details). Writing high will clear this bit.

Note: An Interrupt is generated on the low to high transition of the RDATA_RDY bit.

6.4 System Management Bus Block

W83L951DG/FG provides 2 System Management Bus (SMBus) host controllers. The SMBus host controllers is SMBUS 2.0 compatible. It also provides 32 bytes FIFO. The FIFO contains SMBus1 Master Data FIFO(8), SMBus2 Master Data FIFO(8).

Table 6-9 SMBus 1 Register Define

SMBUS 1 BLOCK(24)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
B1	SM1SCR	Reserved		Baud Rate Select			RBIM	Reserved	Reserved
B2	SM1IREQ	MSTS	MFIFORdy	MFIFOReq	MPktFinish				
B3	SM1IE	Interrupt Enable [7:0]							
B4	SM1FIFOCON	STOP	RepStart	Master Level[1:0]		ClrMFIFO	ClrSFIFO	Slave Leve[1:0]	
B5	SM1MFIFO	Master Data FIFO [7:0]							
B6	SM1MCON	MasterEn	RMS	Read Byte Count[5:0]					
B7	SM1MSTS	RxTMO	TxTMO	AlFull	AlEmty	WrErr	NACKRe	ArbFail	ClrFinish
B9	SM1MFIFOSTS	Full	Empty	FIFO Data Length[5:0]					
BA	Reserved								
BB	Reserved								
BC	Reserved								
BD	Reserved								

Table 6-10 SMBus 2 Register Define

SMBUS 2 BLOCK(24)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C1	SM2SCR	Reserved		Baud Rate Select			RBIM	Reserved	Reserved
C2	SM2IREQ	MSI	MFIFORdy	MFIFOReq	MPktFinish				
C3	SM2IE	Interrupt Enable [7:0]							
C4	SM2FIFOCON	STOP	RepStart	Master Level[1:0]		ClrMFIFO	ClrSFIFO	Slave Leve[1:0]	
C5	SM2MFIFO	Master Data FIFO [7:0]							
C6	SM2MCON	MasterEn	RMS	Read Byte Count[5:0]					
C7	SM2MSTS	RxTMO	TxTMO	AlFull	AlEmty	WrErr	NACKRec	ArbFail	ClrFinish
C9	SM2MFIFOSTS	Full	Empty	FIFO Data Length[5:0]					
CA	Reserved								
CB	Reserved								
CC	Reserved								
CD	Reserved								

Gray: Only with System Reset to initial.

6.4.1 Register Description

6.4.1.1 System Control Register (SM1/2SCR) (Default Value: 0001_10?0)

Bit 7~6: Reserved (Must Assign Low)

Bit 5~3: Baud Rate Select

Select SMBus baud rate.

Input Clock is 24MHz :

When System Clock is 24MHz:

000: 12.5 KHz, 001: 25 KHz, 010: 50 KHz, 011: 100 KHz

100: 400 KHz, 101: 800 KHz, 110: 1.2 MHz, 111: 2.4 MHz

When System Clock is 12MHz:

000: 12.5 KHz, 001: 25 KHz, 010: 50 KHz, 011: 100 KHz

100: 400 KHz, 101: 800 KHz, 110: 1.2 MHz, 111: N/A

When System Clock is 6MHz:

000: 12.5 KHz, 001: 25 KHz, 010: 50 KHz, 011: 100 KHz

100: 400 KHz, 101: 800 KHz, 110: N/A, 111: N/A

Input Clock is 12MHz

When System Clock is 12MHz:

000: 6.25 KHz, 001: 12.5 KHz, 010: 25 KHz, 011: 50 KHz

100: 200 KHz, 101: 400 KHz, 110: 600 KHz, 111: 1.2 MHz

When System Clock is 6MHz:

000: 6.25 KHz, 001: 12.5 KHz, 010: 25 KHz, 011: 50 KHz

100: 200 KHz, 101: 400 KHz, 110: 600 KHz, 111: N/A

When System Clock is 3MHz:

000: 6.25 KHz, 001: 12.5 KHz, 010: 25 KHz, 011: 50 KHz

100: 200 KHz, 101: 400 KHz, 110: N/A, 111: N/A

Bit 2: Rx Byte Interrupt Mode

Select the mode that SMBus receive data bytes to generate Master/Slave Data Ready interrupt.

0: Only First Byte and FIFO Full Byte:

Master/Slave Data Ready Interrupt only occurs in receiving first byte after Start phase or Repeat_Start phase and any byte that make FIFO enter Full state.

1: Every Byte:

Master/Slave Data Ready Interrupt occurs in every time to finish receiving one byte.

Bit 1: SMBALERT Pin Status (Reserved)

Bit 0: SMBALTER Event Control (Reserved)

Control the occurrence of SMBALTER Event

0: Disable

1: Enable.

6.4.1.2 Interrupt Register (SM1/2IREQ) (Default Value: 0000_0000)

Bit 7: Master Status

Indicate Master Status Register changed.

Bit 6: Master FIFO Data Ready Interrupt

Indicate that FIFO finishes receiving data byte when Master is under MSR (Master at Receiving) mode. About detail description, please refer Bit7@SM1/2SCR.

Bit 5: Master FIFO Data Request Interrupt

Indicate that FIFO request micro-processor provides data for transmitting to Salve when Master is under MST (Master at Transmitting) mode and empty.

Bit 4: Master Packet Finished Interrupt

Indicate that Master finishes package transmission (Include Rx and Tx).

Bit 3~0: Reserved

6.4.1.3 Interrupt Enable Register (SM1/2IE) (Default Value: 0000_0000)

All Bits:

1: Enable Interrupt.

The content of Interrupt Register via OR operation will convert into Microprocessor Internal Interrupt Source.

0: Disable Interrupt.

Disable convert into Microprocessor Internal Interrupt, but relative interrupt flag will still be produced.

6.4.1.4 FIFO Control Register (SM1/2FIFOCON) (Default Value: 0000_0000)

Bit 7: STOP Tag Flag (Only for Master)

Indicate that writing byte is the last byte.

Bit 6: Repeat_Start Tag Flag (Only for Master)

Indicate that writing byte is Repeat_Start Byte.

Bit 5~4: Master FIFO Threshold Level Select

00: AE – 2, AF – 6, 01: AE - 3, AF – 5

10: AE – 4, AF – 4, 11: Disable

Note: AE is Almost Empty Flag, AF is Almost Full Flag.

Bit 3: Clear Master FIFO

Clear Master FIFO. Master will stop transfer immediately and generate Stop phase. After SMBus finishes the action, SMBus responds to micro-processor via FIFO Clear Finished Event in Master Status Register.

Bit 2~0: Reserved

6.4.1.5 Master Data FIFO Register (SM1/2MFIFO) (Default Value: 0000_0000)

This FIFO register stores the data from Master.

Only allow writing in MST mode, and only allowed to read in MSR mode. Default is MST mode and transforming is through Data_Ready_Interrupt.

6.4.1.6 Master Control Register (SM1/2MCON) (Default Value: 0100_0000)

Bit 7: Master Enable

Bit 6: Read Mode Select

1: Host Read One Byte Hold Mode.

Master holds bus (drive SCL low) after finishing receiving every byte.

0: Host Read Continue Mode.

Master finishes {Receiving Package -> Stop Phase -> Release Bus} automatically according to read byte count.

Note: If Read Byte Count initial value is 1, Master will ignore criterion of "Host Read One Byte Hold Mode".

Bit 5~0: Read Byte Count

Indicate Read Byte Count. The allowed maximum is 64 bytes block read.

Filled Value	Actual Value
0	64
1~63	1~63

6.4.1.7 Master Status Register (SM1/2MSTS) (Default Value: 0000_0000)

Bit 7: Master Rx Timeout Event

Indicate Master generates RX_TIMEOUT (When Master FIFO is full, SCL drive low to generate timeout). After the Master generates Stop Phase, will be back to initial state and clear FIFO.

Note: If timeout is not generated by the Master, the response will occur in FIFO Clear Finished Event in Master Status Register.

Bit 6: Master Tx Timeout Event

Indicate Master generates TX_TIMEOUT (When Master FIFO is empty, SCL drive low to generate timeout). After Master generates Stop Phase, will be back to initial state and clear FIFO.

Note: If timeout is not generated by Master, the response is in FIFO Clear Finished Event in Master Status Register.

Bit 5: Master Almost Full Event

Indicate that Master generate Almost Full Event. It occurs only up to Almost Full level.

Bit 4: Master Almost Empty Event

Indicate that Master generate Almost Empty Event. It occurs only down to Almost Empty level.

Bit 3: Master FIFO Data Write Error Event

Indicate that Microprocessor writes to Master FIFO, Master FIFO is full or Read Mode.

Bit 2: NACK Received Event

Indicate that Master receives NACK. After generating Stop Phase, Master will be back to initial state and clear FIFO.

Note: Wait for the response of Clear Finished Event in Master Status Register to start next transfer.

Bit 1: Bus Arbitration Failed Event

Indicate that bus arbitration failed. Master will be back to initial state and clear FIFO.

Bit 0: FIFO Clear Finished Event

Indicate that Master finishes the request to clear FIFO.

Note: When Micro Processors has not proposed Master FIFO Clear Request but produces, it indicates the remote device to drive SCL low to generate timeout.

6.4.1.8 Master FIFO Status Register (SM1/2MFIFOSTS) (Default Value: 0100_0000)

Bit 7: Full Flag

Bit 6: Empty Flag

Bit 5~4: Reserved

Bit 3~0: FIFO Data Length

6.5 Internal Interrupt Controller Block

W83L951DG/FG Interrupts occur by 28 sources, 27 external and 25 internal interrupt.

About Interrupt Control, each interrupt is controlled and corresponding to a bit in Interrupt Enable Register (IE1/2/3/4), the Interrupt Priority Control Register (IP1/2/3/4) and the Interrupt Request Register (IREQ1/2/3/4).

An interrupt occurs if the corresponding Interrupt Request occurs and enable bits is HIGH. When several interrupts occur at the same time, the interrupts are received according to priority setting. If interrupts are setting to same priority, then it is decided by hardware internal checking rule.

After Interrupt of EXTINT1, EXTINT2, EXTINT3, SMBUS1, SMBUS2, FAN1 and FAN2 is produced, can't be interrupt by other Interrupt source, so should set as High Propriety.

Table 6-11 Internal Interrupt Controller Register Define

INTERRUPT BLOCK(17)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
E1	IE1	TimerY	TimerX	Timer2	Timer1	OBE1	IBF1	OBE0	IBF0
E2	IE2	CNTR1	CNTR0	ADC	RTC	KEY-WP	EXINT3	EXTINT2	EXTINT1
E3	IE3	FAN2	FAN1	CIR	APS2	MPS2	KPS2	SMBUS2	SMBUS1
E4	IE4	R	R	R	R	R	R	UARTRX	UARTTX
E9	IREQ1	TimerY	TimerX	Timer2	Timer1	OBE1	IBF1	OBE0	IBF0
EA	IREQ2	CNTR1	CNTR0	ADC	RTC	KEY-WP	EXINT3	EXTINT2	EXTINT1
EB	IREQ3	FAN2	FAN1	CIR	APS2	MPS2	KPS2	SMBUS2	SMBUS1
EC	IREQ4	R	R	R	R	R	R	UARTRX	UARTTX
F1	IPRO1	TimerY	TimerX	Timer2	Timer1	OBE1	IBF1	OBE0	IBF0
F2	IPRO2	CNTR1	CNTR0	ADC	RTC	KEY-WP	EXINT3	EXTINT2	EXTINT1
F3	IPRO3	FAN2	FAN1	CIR	APS2	MPS2	KPS2	SMBUS2	SMBUS1
F4	IPRO4	R	R	R	R	R	R	UARTRX	UARTTX

Table 6-12 Internal Interrupt Vector & Trigger Type Table

SOURCE	VECTOR ADDRESS	TRIGGER TYPE
Non-mask Interrupt	0x0003	Edge Trigger
LPC Power Fail Interrupt	0x000b	Edge Trigger
Input Buffer 0 Full Interrupt	0x0013	Edge Trigger
Output Buffer 0 Empty Interrupt	0x001b	Edge Trigger
Input Buffer 1 Full Interrupt	0x0023	Edge Trigger
Output Buffer 1 Empty Interrupt	0x002b	Edge Trigger
Timer 1 Interrupt	0x0033	Edge Trigger
Timer 2 Interrupt	0x003b	Edge Trigger
Timer X Interrupt	0x0043	Edge Trigger
Timer Y Interrupt	0x004b	Edge Trigger
External Interrupt Group 1	0x0053	Level Trigger
External Interrupt Group 2	0x005b	Level Trigger
External Interrupt Group 3	0x0063	Level Trigger
Key Interrupt	0x006b	Edge Trigger
Real Time Clock Alarm Interrupt	0x0073	Edge Trigger
ADC Interrupt	0x007b	Edge Trigger
CNTR0 Interrupt	0x0083	Edge Trigger
CNTR1 Interrupt	0x008b	Edge Trigger
SMBUS 1 Interrupt	0x0093	Level Trigger
SMBUS 2 Interrupt	0x009b	Level Trigger
Keyboard PS2 Interrupt	0x00a3	Edge Trigger
Mouse PS2 Interrupt	0x00ab	Edge Trigger
Auxiliary PS2 Interrupt	0x00b3	Edge Trigger
CIR Interrupt	0x00bb	Edge Trigger
FAN 1 Interrupt	0x00c3	Level Trigger
FAN 2 Interrupt	0x00cb	Level Trigger
UART Tx Interrupt	0x00d3	Edge Trigger
UART Rx Interrupt	0x00db	Edge Trigger
Reserved	0x00e3	N/A
Reserved	0x00eb	N/A
Reserved	0x00f3	N/A
Reserved	0x00fb	N/A

6.5.1 Register Description

6.5.1.1 Interrupt Enable 1 Register (IE1) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor that Interrupt will be produced, and write down in Interrupt Request 1 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor that Interrupt will be produced, but write down in Interrupt Request 1 Register.

6.5.1.2 Interrupt Enable 2 Register (IE2) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor that Interrupt will be produced, and write down in Interrupt Request 2 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor that Interrupt will be produced, but write down in Interrupt Request 2 Register.

6.5.1.3 Interrupt Enable 3 Register (IE3) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor that Interrupt will be produced, and write down in Interrupt Request 3 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor that Interrupt will be produced, but write down in Interrupt Request 3 Register.

6.5.1.4 Interrupt Enable 4 Register (IE4) (Default Value: 0000_0000)

1: Enable. It produces Interrupt Request to Micro-Processor that Interrupt will be produced, and write down in Interrupt Request 4 Register.

0: Disable. It does not produce Interrupt Request to Micro-Processor that Interrupt will be produced, but write down in Interrupt Request 4 Register.

6.5.1.5 Interrupt Request 1 Register (IREQ1) (Default Value: 0000_0000)

Read:

1: Requested

0: No Requested

Write:

1: Clear

0: No Change

6.5.1.6 Interrupt Request 2 Register (IREQ2) (Default Value: 0000_0000)

Read:

1: Requested

0: No Requested

Write:

1: Clear

0: No Change

6.5.1.7 Interrupt Request 3 Register (IREQ3) (Default Value: 0000_0000)

Read:

1: Requested

0: No Requested

Write:

1: Clear

0: No Change

6.5.1.8 Interrupt Request 4 Register (IREQ4) (Default Value: 0000_0000)

Read:

1: Requested

0: No Requested

Write:

1: Clear

0: No Change

6.5.1.9 Interrupt Priority 1 Register (IPRO1) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

6.5.1.10 Interrupt Priority 2 Register (IPRO2) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

6.5.1.11 Interrupt Priority 3 Register (IPRO3) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

6.5.1.12 Interrupt Priority 4 Register (IPRO4) (Default Value: 0000_0000)

1: High Priority

0: Low Priority

6.6 GPIOs Block

W83L951DG/FG provides 13 GPIO blocks, and every GPIO block has 8 GPIO that can set individually. I/O Pad has three states by data register and direction register setting. Input register always reads current pad status.

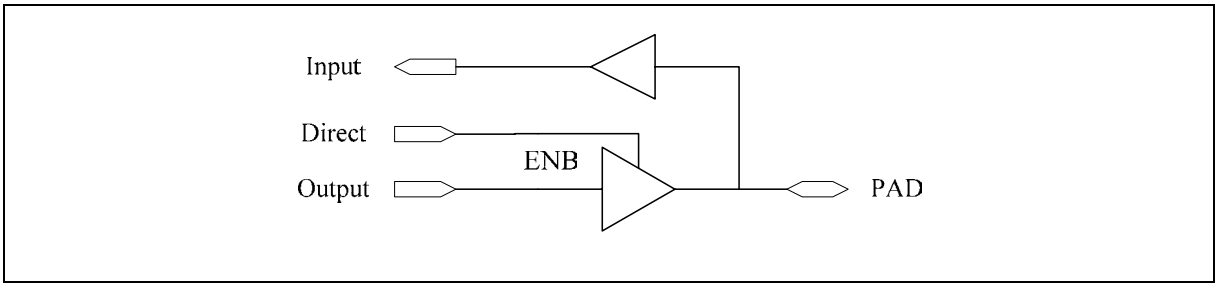


Figure 6-1 GPIO Block Diagram

Table 6-13 GPIOs Type Setup Define

TYPE	OUTPUT REGISTER(WRITE)	DIRECTION REGISTER
Input	Don't Care	0
Output	Output Data	1
Open-Drain	0	Output Data'

Table 6-14.GPIOs Control Register Define

GPIO BLOCK(26)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
80	GPIO0	GPIO 0 Input/Output Register[7:0]							
88	GPIO1	GPIO 1 Input/Output Register[7:0]							
90	GPIO2	GPIO 2 Input/Output Register[7:0]							
98	GPIO3	GPIO 3 Input/Output Register[7:0]							
A0	GPIO4	GPIO 4 Input/Output Register[7:0]							
A8	GPIO5	GPIO 5 Input/Output Register[7:0]							
B0	GPIO6	GPIO 6 Input/Output Register[7:0]							
B8	GPIO7	GPIO 7 Input/Output Register[7:0]							
C0	GPIO8	GPIO 8 Input/Output Register[7:0]							
C8	GPIO9	GPIO 9 Input/Output Register[7:0]							
D8	GPIOA	GPIO A Input/Output Register[7:0]							
E8	GPIOB	GPIO B Input/Output Register[7:0]							
F8	GPIOC	GPIO C Input/Output Register[7:0]							

Continued.

GPIO BLOCK(26)									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D1	GPIOD0	GPIO 0 Direction Register[7:0]							
D2	GPIOD1	GPIO 1 Direction Register[7:0]							
D3	GPIOD2	GPIO 2 Direction Register[7:0]							
D4	GPIOD3	GPIO 3 Direction Register[7:0]							
D5	GPIOD4	GPIO 4 Direction Register[7:0]							
D6	GPIOD5	GPIO 5 Direction Register[7:0]							
D7	GPIOD6	GPIO 6 Direction Register[7:0]							
D9	GPIOD7	GPIO 7 Direction Register[7:0]							
DA	GPIOD8	GPIO 8 Direction Register[7:0]							
DB	GPIOD9	GPIO 9 Direction Register[7:0]							
DC	GPIODA	GPIO A Direction Register[7:0]							
DD	GPIODB	GPIO B Direction Register[7:0]							
DE	GPIODC	GPIO C Direction Register[7:0]							

6.6.1 GPIO Data Register Description

6.6.1.1 GPIO 0 Input/Output Register (GPIO0) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result.
For example "CPL Bit" Instruction
Read Pin Status into temp Register.
Invert temp register.
Write Result to Output Data Register according for bit address, and not influence the value of other bit.

6.6.1.2 GPIO 1 Input/Output Register (GPIO1) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.3 GPIO 2 Input/Output Register (GPIO2) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.4 GPIO 3 Input/Output Register (GPIO3) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.5 GPIO 4 Input/Output Register (GPIO4) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.6 GPIO 5 Input/Output Register (GPIO5) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.7 GPIO 6 Input/Output Register (GPIO6) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.8 GPIO 7 Input/Output Register (GPIO7) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.9 GPIO 8 Input/Output Register (GPIO8) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.10 GPIO 9 Input/Output Register (GPIO9) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.11 GPIO A Input/Output Register (GPIOA) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.12 GPIO B Input/Output Register (GPIOB) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.1.13 GPIO C Input/Output Register (GPIOC) (Default Value: 0000_0000)

Write:

Output data register

Read:

GPIO pin status whether GPIO function is active or not.

Note: bit command and byte command have same result

6.6.2 GPIO Direction Register Description

6.6.2.1 GPIO 0 Direction Register (GPIOD0) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.2 GPIO 1 Direction Register (GPIOD1) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.3 GPIO 2 Direction Register (GPIOD2) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.4 GPIO 3 Direction Register (GPIOD3) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.5 GPIO 4 Direction Register (GPIOD4) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.6 GPIO 5 Direction Register (GPIOD5) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.7 GPIO 6 Direction Register (GPIOD6) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.8 GPIO 7 Direction Register (GPIOD7) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.9 GPIO 8 Direction Register (GPIOD8) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.10 GPIO 9 Direction Register (GPIOD9) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.11 GPIO A Direction Register (GPIODA) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.12 GPIO B Direction Register (GPIODB) (Default Value: 0000_0000)

1: Output,

0: Input.

6.6.2.13 GPIO C Direction Register (GPIODC) (Default Value: 0000_0000)

1: Output,

0: Input.

6.7 Watch Dog Block

The watchdog timer gives a mean of returning to the reset state when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit timer L and an 8-bit timer H. At reset or writing to the watchdog timer control register WDTCON [7] (START), each watchdog timer H and L is set to 0FFh.

About Watchdog timer H count size selection, we can use Bit 5 of the watchdog timer control register (SIZE) permits selecting a watchdog timer H count source. When this bit is set to LOW, the count source becomes the underflow signal of watchdog timer L.

Table 6-15.Watch Dog Register Define

WATCH DOG BLOCK(1)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	WDTCON	START	INTTYPE	SIZE	Clock Prescale Number[4:0]				
01	WDTSTS	Reserved							+WDT

Gray: Only with System Reset (Pin Reset + WDT Reset) to Initial.

+: Only with Pin Reset to Initial

6.7.1 Register Description

6.7.1.1 Watch Dog Control Register (WDTCON) (Default Value: 0000_0000)

Reset with Power Reset & Pin Reset.

Bit 7: Start

1: Start / Reload

0: Stop

This Bit permits enable/disable the watchdog timer. Write LOW to this bit, the watchdog timer is stopped. Write HIGH to this bit will reload the watchdog timer (watchdog timer H and L is set to 0FFh) even this bit is already be HIGH. After written HIGH, the watchdog timer is running. Once this timer is timed-out the chip is reset. Also the watchdog timer is stopped to prevent the next time-out.

Bit 6: Interrupt Type

1: NMI

0: Hardware reset

Bit 5: Size

Select the counter size. The counter starts from low to overflow. Then generate interrupt or hardware reset.

1: One Byte Counter. $\text{WDT Timeout Limit} \approx 256/\text{Count Frequency}$.

0: Two Byte Counter. $\text{WDT Timeout Limit} \approx 65536/\text{Count Frequency}$.

Bit 4~0: Clock Prescale Number

Input clock=24MHz : Count frequency is 1MHz / 2(Clock Prescale Number +1).

Input clock=12MHz : Count frequency is 1MHz / 4(Clock Prescale Number +1).

6.7.1.2 Watch Dog Status Register (WDTSTS) (Default Value: 0000_0000)

Reset with Power Reset.

Bit 7~1: Reserved

Bit 0: WDT Reset Finished

1: Finished, 0: No Happened.

6.8 Timer Block

The Keyboard controller has four timers: timer X, timer Y, timer 1, and timer 2. The division ratio of each timer or pre-scalar is given by 1/n + 1, where n is the value in the corresponding timer or pre-scalar latch. All timers are count down. When the timer reaches "00H", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer is underflow, the corresponding interrupt request bit is set to 1.

In Timer 1 and Timer 2, the count source of pre-scalar 1/2 is the oscillator frequency divided by 16. The output of pre-scalar 1/2 is counted for both timer 1 and 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y can works in one of four operating modes by setting the timer XY mode register.

Table 6-16.Timer Register Define

TIMER BLOCK(9)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10	PRE1	TM1ST	Prescale 1 [6:0]						
11	T1	Timer 1 [7:0]							
12	PRE2	TM2ST	Prescale 2 [6:0]						
13	T2	Timer 2 [7:0]							
18	TM	TMYST	CNTR1	TMYMODE		TMXST	CNTR0	TMXMODE	
19	PREX	Prescale X [7:0]							
1A	TX	Timer X[7:0]							
1B	PREY	Prescale Y [7:0]							
1C	TY	Timer Y [7:0]							

6.8.1 Register Description

6.8.1.1 Clock Prescale Number of Timer 1 (PRE1) (Default Value: 0111_1111)

Bit 7: Timer 1 Start Bit

Write: Start Timer 1 counter.

1: Enable (Prescale Counter Reload & Start, but Timer 1 Data Keep)

0: Disable

Read: Always Read ‘LOW’.

Bit 6~0: Clock Prescale Number

Write: Prescale Counter Reload.

Read: Current Prescale Counter Value

6.8.1.2 Timer 1 Register (T1) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer 1 Counter Reload.

Read: Current Timer 1 Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

6.8.1.3 Clock Prescale Number of Timer 2 (PRE2) (Default Value: 0111_1111)

Bit 7: Timer 2 Start Bit

1: Start (Prescale Counter Reload & Start, but Timer 2 Data Keep)

0: Stop

Bit 6~0: Clock Prescale Number

Write: Prescale Counter Reload.

6.8.1.4 Timer 2 Register (T2) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer 2 Reload.

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

6.8.1.5 Timer X/Y Mode Register (TM) (Default Value: 0000_0000)

Bit 7: Timer Y Start Bit

Start internal Time Y counter and

1: Enable (Prescale Y & Timer Y Data Keep after Stop)

0: Disable

Bit 6: CNTR1 active edge selection bit

0: Interrupt at falling edge Count at rising edge in event counter mode.

1: Interrupt at rising edge Count at falling edge in event counter mode.

Bit 5-4: Timer Y operating bit

00: Timer mode

The Timer Y can select the count by XIN/16.

01: Pulse output mode (Disable GP83 Function, Pin Direct Force “Output”)

Timer Y counts XIN/16. Whenever the contents of the timer reach “00H”, the signal output from the CNTR1 pin is inverted. If the CNTR1 active edge selection bit is 0, the pin is “H” after initial. If it is 1, the pin is ‘L’ after initial. When using a timer in this mode, set the corresponding direction register of port GP83 to output mode.

10: Event count mode (Disable GP83 Function, Pin Direct Force “Input”)

Operating on event counter mode is the almost same as in timer mode, except that the timer counts signals input through the CNTR1. When the CNTR1 active edge selection bit is 0, the rising edge on the CNTR1 pin is counted. When the CNTR1 active edge selection bit is 1, the falling edge on the CNTR1 pin is counted.

11: Pulse width measurement mode (Disable GP83 Function, Direct Force “Input”)

If the CNTR1 active edge selection bit is 0, the timer counts XIN/16 while the CNTR1 pin is H. If the CNTR1 active edge selection bit is 1, the timer counts while the CNTR1 pin is ‘L’.

Bit 3: Timer X Start Bit

1: Enable (Prescale X & Timer X Data Keep)

0: Disable

Bit 2: CNTR0 active edge selection bit

0: Interrupt at falling edge Count at rising edge in event counter mode.

1: Interrupt at rising edge Count at falling edge in event counter mode.

Bit 1-0: Timer X operating bit

00: Timer mode

The Timer X only counts XIN/16.

01: Pulse output mode (Disable GP82 Function, Direct Force “Output”)

Timer X counts XIN/16. Whenever the contents of the timer reach “00H”, the signal output from the CNTR0 pin is inverted. If the CNTR0 active edge selection bit is 0, the pin is “H” after initial. If it is 1, the pin is ‘L’ after initial. When using a timer in this mode, set the corresponding direction register of port GP82 to output mode.

10: Event count mode (Disable GP82 Function, Direct Force “Input”)

Operating on event counter mode is the almost same as in timer mode, except that the timer counts signals input through the CNTR0. When the CNTR0 active edge selection bit is 0, the rising edge on the CNTR0 pin is counted. When the CNTR0 active edge selection bit is 1, the falling edge on the CNTR0 pin is counted.

11: Pulse width measurement mode (Disable GP82 Function, Direct Force “Input”)

If the CNTR0 active edge selection bit is 0, the timer counts XIN/16 while the CNTR0 pin is H. If the CNTR0 active edge selection bit is 1, the timer counts while the CNTR0 pin is ‘L’.

> *Note: The count can be stopped by setting a “0” to the timer X (or timer Y) count start bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.*

6.8.1.6 Clock Prescale Number of Timer X (PREX) (Default Value: 1111_1111)

Bit 7~0: Clock Prescale Number

Write: Prescale Counter Reload.

Read: Current Prescale Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

6.8.1.7 Timer X Register (TX) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer X Reload.

Read: Current Timer X Counter Value

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

6.8.1.8 Clock Prescale Number of Timer Y (PREY) (Default Value: 1111_1111)

Bit 7~0: Clock Prescale Number

Write: Prescale Counter Reload.

Note: In writing, due to the effect of internal frequency XIN/16, 0~16 system clock error occurs in first prescale period width.

Read: Current Prescale Counter Value

6.8.1.9 Timer Y Register (TY) (Default Value: 1111_1111)

Bit 7~0:

Write: Timer Y Reload.

Read: Current Timer X Counter Value

6.9 Pulse Width Modulator Block

W83L 951D provides 4 Pulse Width Modulator Output.

8-bit PWM has two: PWM1 and PWM2. The fixed resolution is about 64us(Input clock=24MHz) or 128us(Input clock=12MHz).

16-bit PWM has two: PWM3 and PWM4. The minimum resolution can be selected by frequency select in PWM Control Register.

Table 6-17.Pulse Width Modulator Register Define

PULSE WIDTH MEASURER BLOCK(13)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
20	PWMCON	Reserved	PWM4 Freq. Select			Reserved	PWM3 Freq. Select		
21	PWM1P	PWM 1 Period Register [7:0]							
22	PWM1H	PWM 1 High Level Register [7:0]							
23	PWM2P	PWM 2 Period Register [7:0]							
24	PWM2H	PWM 2 High Level Register [7:0]							
25	PWM3PL	PWM 3 Period Register [7:0]							
26	PWM3PH	PWM 3 Period Register [15:8]							
27	PWM3HL	PWM 3 High Level Register [7:0]							
28	PWM3HH	PWM 3 High Level Register [15:8]							
29	PWM4PL	PWM 4 Period Register [7:0]							
2A	PWM4PH	PWM 4 Period Register [15:8]							
2B	PWM4HL	PWM 4 High Level Register [7:0]							
2C	PWM4HH	PWM 4 High Level Register [15:8]							

Gray: Only with System Reset to initial.

Note:

If {PWM High Level Register} = 0, the output keeps in low level.

If {PWM High Level Register} >= {PWM Period Register} ,the PWM1/PWM2 output will keep in high level with 1us low pulse , PWM3/PWM4 output will keep in high level without pulse.

If PWM1/PWM2 is {PWM Period Level Register} > {PWM High Level Register} >0, then

Period Width: 64 × {PWM Period Level Register} + 4units.

Low Width : 64 × ({PWM Period Level Register} − {PWM High Level Register}) + 1unit.

High Width : 64 × {PWM High Level Register} + 3 units.

The unit is 1us in PWM1/PWM2.

PWM 3/PWM4 is {PWM Period Level Register} > {PWM High Level Register} >0, then

Period Width: {PWM Period Level Register} + 4units.

Low Width : {PWM Period Level Register} — {PWM High Level Register} + 1unit.

High Width : {PWM High Level Register} + 3units.

The unit is 1/F in PWM 3/PWM4. And F is defined in PWM Control Register.

PWM 1/PWM2/PWM3/PWM4 is default low.

6.9.1 Register Description

6.9.1.1 PWM Control Register (PWMCON) (Default Value: 0000_0000)

Bit 7: Reserved

Bit 6~4: PWM 4 Frequency Select

Input clock=24MHz :

111: Reserved, 110: 375 KHz, 101: 750 KHz, 100: 1.5 MHz.

011: 3 MHz, 010: 6 MHz, 001: 12 MHz, 000: 24 MHz.

Input clock=12MHz :

111: Reserved, 110: Reserved, 101: 375 KHz, 100: 750KHz.

011: 1.5 MHz, 010: 3 MHz, 001: 6 MHz, 000: 12 MHz.

Bit 3: Reserved

Bit 2~0: PWM 3 Frequency Select

Input clock=24MHz :

111: Reserved, 110: 375 KHz, 101: 750 KHz, 100: 1.5 MHz.

011: 3 MHz, 010: 6 MHz, 001: 12 MHz, 000: 24 MHz.

Input clock=12MHz :

111: Reserved, 110: Reserved, 101: 375 KHz, 100: 750KHz.

011: 1.5 MHz, 010: 3 MHz, 001: 6 MHz, 000: 12 MHz.

6.9.1.2 PWM 1 Period Register (PWM1P) (Default Value: 0000_0000)

Use the 8-bit register to control width of a full period output.

6.9.1.3 PWM 2 Period Register (PWM2P) (Default Value: 0000_0000)

Use the 8-bit register to control width of a full period output.

6.9.1.4 PWM 3 Period Register (PWM3PH, PWM3PL) (Default Value: 0000h)

Use the 16-bit register to control width of a full period output.

6.9.1.5 PWM 4 Period Register (PWM4PH, PWM4PL) (Default Value: 0000h)

Use the 16-bit register to control width of a full period output.

6.9.1.6 PWM 1 High Level Register (PWM1H) (Default Value: 0000_0000)

PWM1H is defined as high signal width for PWM1 output. It is an 8-bit register.

6.9.1.7 PWM 2 High Level Register (PWM2H) (Default Value: 0000_0000)

PWM2H is defined as high signal width for PWM2 output. It is an 8-bit register.

6.9.1.8 PWM 3 High Level Register (PWM3HH, PWM3HL) (Default Value: 0000_0000)

(PWM3HH, PWM3HL) is defined as high signal width for PWM3 output. It is a 16-bit register.

6.9.1.9 PWM 4 High Level Register (PWM4HH, PWM4HL) (Default Value: 0000_0000)

(PWM4HH, PWM4HL) is defined as high signal width for PWM4 output. It is a 16-bit register.

6.10 UART Block

W83L951DG/FG supports one Universal asynchronous serial I/O mode (UART) .Eight serial data transfer formats can be selected, for vary selection of Stop bit, Parity, Parity check, Data length, and the transfer formats used by a transmitter and receiver must be identical.

The transmitter and receiver shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register. The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a byte while the next byte is being received.

Table 6-18.UART Register Define

UART Block(5)									
ExtAddr	Name	7	6	5	4	3	2	1	0
30	UARTCON	TxEn	TS	RxEn	PARE	PARS	STPS	CHAS	Reserved
31	UARTSTS	ParErr	FrameErr	OverErr	Reserved			RxBFull	TxBFull
32	BRGH	Baud Rate Generator High Byte[7:0]							
33	BRGL	Baud Rate Generator Low Byte[7:0]							
34	UARTBUF	UART Transmit / Receive Buffer[7:0]							

Gray: Only with System Reset to initial.

6.10.1 Register Description

6.10.1.1 UART Control Register (UARTCON) (Default Value: 0000_0000)

Bit 7: Transmit enable bit (TE)

0: Transmit disabled. 1: Transmit enable.

Bit 6: Transmit Speed up bit (TS) (Reserved)

0: Disable.

1: Enable.

Bit 5: Receive enable bit (RE)

0: Receive disable. 1: Receive enable.

Bit 4: Parity enable bit (PARE).

0: Parity Bit disable. 1: Parity Bit enable.

Bit 3: Parity selection bit (PARS).

0: Odd parity. 1: Even parity.

Bit 2: Stop bit length selection bit (STPS)

0: 1 stop bit. 1: 2 stop bits.

Bit 1: Character length selection bit (CHAS) .

0: 8 bits 1: 7 bits.

Bit 0: User Define Register

6.10.1.2 UART Status Register (UARTSTS) (Default Value: 0000_0000)

Bit 7: Parity Error Status for Packet at Receive Buffer (PE)

Read: 0 - No error, 1 - Parity error

Bit 6: Framing Error Status for Packet at Receive Buffer (FE)

Read: 0 - No error, 1 - Framing error

Bit 5: Overrun Error Interrupt (OE)

For UART Rx Interrupt, users need to write this bit to clear.

Read:

0 - No error

1 - Overrun error

Write:

0 - No Chang

1 - Clear

Bit 4~2: No use (return 'L' when read)

Bit 1: Receive Buffer Full Status Flag (RBF)

Receive Buffer Full generates the interrupt. Read buffer can clear the flag.

0: Buffer empty

1: Buffer full

Bit 0: Transmit Buffer Full Status Flag (TBF)

Transmit Buffer Empty generates the interrupt. Write buffer can clear the flag. And next byte is allowed to write into the buffer.

0: Buffer empty

1: Buffer full

6.10.1.3 Baud Rate Generator High/Low Byte Register (BRGH/BRGL) (Default Value: 0000_0000_0000_0000)

Input clock=24MHz :

Baud Rate Period Width = (N+1) / 3MHz.

And N = {BRGH, BRGL}

Input clock=12MHz :

Baud Rate Period Width = 2(N+1) / 3MHz.

And N = {BRGH, BRGL}

6.10.1.4 UART Transmit / Receive Buffer (UARTBUF) (Default Value: 0000_0000)

Read: Receive Buffer

Write: Transmit Buffer

6.11 Consumer Infrared Communications Receiver Block

The CIrCC implements hardware-level decoding for the NEC Consumer IR Remote Control format. The hardware decoder may be used to generate a wake-up event or to send parts of the received message frame to the FIFO. The No Care Custom Code (NCCC), No Care Data Code (NCDC), PME Wake and Frame bits of the Consumer IR Control register configure the hardware decoder.

About NEC Consumer IR Format, the NEC Consumer IR Remote Control format specifies a 38 kHz carrier, 13ms of sync framing, and 32 bits of pulse-position modulated (PPM) message data. The message data includes an 8 bit Custom Code field, an 8 bit Custom Code' field, an 8 bit Data Code field, and an 8 bit Data Code' field. A single frame of the NEC PPM Consumer Remote Control signal is shown in Figure 14-1.

The Custom Code fields in this protocol uniquely address message frames for specific devices. The Custom Code fields can be used as a 16 bit address or as an 8 bit address followed by the bit-wise complement of the Custom Code field Custom Code. The Data Code field is an 8 bit command code, Data Code' is the bit-wise complement of Data Code.

Note: The CIrCC hardware can decode NEC protocol framing (sync pulse, 32 bit PPM message data) at any data rate, depending on the programmed Bit Rate Divider (BRD).

Table 6-19.Consumer Infrared Communications Receiver Register Define

CIR BLOCK(3)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
40	CIRCON	DFE	SFE	REP	FINISH	DM	SM	RM	RXINV
41	CIRBRD	Baud Rate Divider[7:0]							
42	CIRDATA1	CIR Receive Data 1[7:0]							
43	CIRDATA2	CIR Receive Data 2[7:0]							
44	CIRDATA3	CIR Receive Data 3[7:0]							
45	CIRDATA4	CIR Receive Data 4[7:0]							

Gray: Only with System Reset to initial.

6.11.1 Register Description

6.11.1.1 CIR Configure Register (CIRCON) (Default Value: 0000_0000)

Bit 7: Data Frame Error Status Flag (Write 'HIGH' to Clear)

When Data Frame Error flag occurs, CIR Interrupt is generated. Write the bit can clear Data Frame Error Flag.

Read:

0 - No error

1 - Data frame Error

Write:

0 - No Change

1 - Clear

Bit 6: Start Frame Error Status Flag (Write 'HIGH' to Clear)

When Start Frame Error flag occurs, CIR Interrupt is generated. Write the bit can clear Start Frame Error Flag.

Read:

0 - No error

1 – Start Frame Error

Write:

0 - No Change

1 - Clear

Bit 5: Repeat Status Flag (Write 'HIGH' to Clear)

When Repeat Flag occurs, CIR Interrupt is generated. Write the bit can clear Repeat Flag.

Read:

0 - No happened

1 – Repeat Packet Received.

Write:

0 - No Change

1 - Clear

Bit 4: Finish Status Flag (Write 'HIGH' to Clear)

When Finish Flag occurs, CIR Interrupt is generated. Write the bit can clear Finish Flag.

Read:

0 - No happened

1 – Packet Received is finish.

Write:

0 - No Chang

1 - Clear

Bit 3: Data Frame Error Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 2: Start Frame Error Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 1: Repeat Interrupt Mask Enable

0 – Enable.

1 – Disable.

Bit 0: Rx Signal Invert Enable

Enable CIR Rx signal Convert Function

0 – Enable.

1 – Disable.

6.11.1.2 Baud Rate Divider (CIRBRD) (Default Value: 0101_0101)

Input clock=24MHz :

The Transmit and Receive Bit Rate Divider register is used to extract a serial NRZ data stream for the CIrCC SCE. The divider is eight bits wide. The input clock to the Bit Rate Divider is 100 KHz (Carrier Frequency Divider input clock 16). The relationship between the Bit Rate Divider (BRD) and the Bit Rate (Fb) is as follows:

BRD = (.1MHz/Fb) – 1

For example, program the Bit Rate Divider with 55 ('37'Hex) for a .562ms Remote Control bit cell like for the NEC remote control frame format: Fb = 1.786 KHz. This is ~.5% accuracy. Table 9 contains representative BRD vs. BitRate relationships. The Bit Rate range is 100 KHz to 390.625Hz.

Input clock=12MHz :

The Transmit and Receive Bit Rate Divider register is used to extract a serial NRZ data stream for the CIrCC SCE. The divider is eight bits wide. The input clock to the Bit Rate Divider is 50 KHz (Carrier Frequency Divider input clock 16). The relationship between the Bit Rate Divider (BRD) and the Bit Rate (Fb) is as follows:

BRD = (.05MHz/Fb) – 1

For example, program the Bit Rate Divider with 55 ('37'Hex) for a .562ms Remote Control bit cell like for the NEC remote control frame format: Fb = 0.893 KHz. This is ~.5% accuracy. Table 9 contains representative BRD vs. BitRate relationships. The Bit Rate range is 50 KHz to 190Hz.

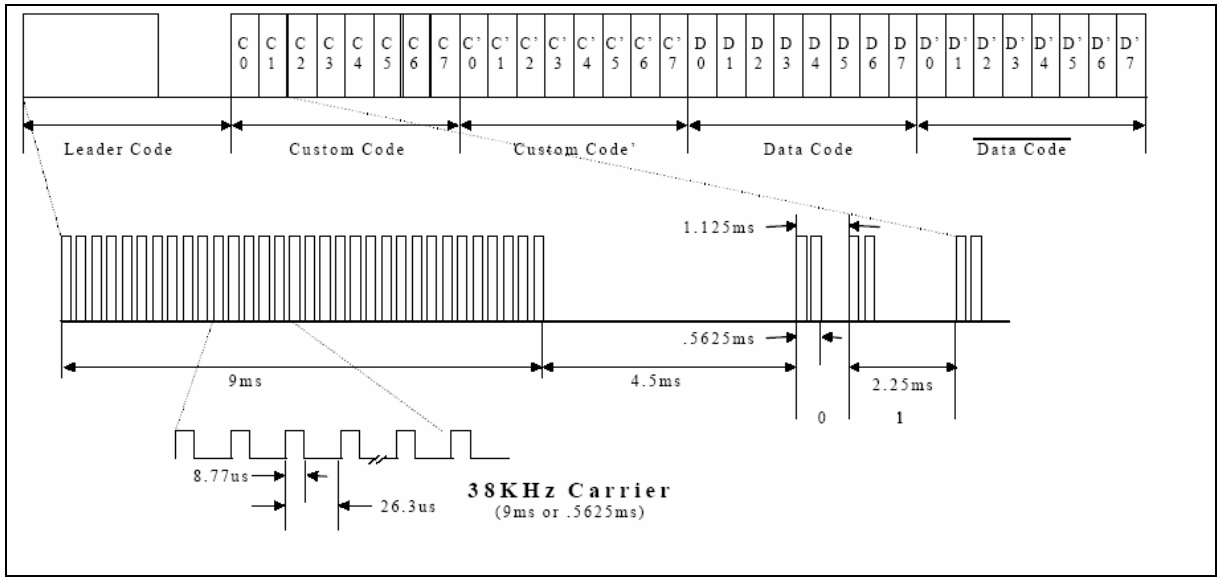


Figure 6-2.NEC CIR Frame Format

Table 6-20.Bit Rate Divider (BRD) V.S Bit Rate (Fb)

INPUT CLOCK=12MHZ							
BRD	**FB (KHZ)**	**BRD**	**FB (KHZ)**	**BRD**	**FB (KHZ)**	**BRD**	**FB (KHZ)**
003	12.5	067	0.7355	131	0.379	195	0.255
007	6.25	071	0.6945	135	0.3675	199	0.25
011	4.1665	075	0.658	139	0.357	203	0.245
015	3.125	079	0.625	143	0.347	207	0.2405
019	2.5	083	0.595	147	0.338	211	0.236
023	2.0835	087	0.568	151	0.329	215	0.2315
027	1.7855	091	0.5435	155	0.3205	219	0.2275
031	1.5625	095	0.521	159	0.3125	223	0.223
035	1.389	099	0.5	163	0.305	227	0.2195
039	1.25	103	0.481	167	0.2975	231	0.2155
043	1.1365	107	0.463	171	0.2905	235	0.212
047	1.0415	111	0.4465	175	0.284	239	0.2085
051	0.9615	115	0.431	179	0.278	243	0.205
055	0.893	119	0.4165	183	0.2715	247	0.2015
059	0.8335	123	0.403	187	0.266	251	0.1985
063	12.5	127	0.781	191	0.521	255	0.19

Continued.

INPUT CLOCK=24MHZ							
BRD	**FB (KHZ)**	**BRD**	**FB (KHZ)**	**BRD**	**FB (KHZ)**	**BRD**	**FB (KHZ)**
BRD	Fb (kHz)	BRD	Fb (kHz)	BRD	Fb (kHz)	BRD	Fb (kHz)
003	25.000	067	1.471	131	0.758	195	0.510
007	12.500	071	1.389	135	0.735	199	0.500
011	8.333	075	1.316	139	0.714	203	0.490
015	6.250	079	1.250	143	0.694	207	0.481
019	5.000	083	1.190	147	0.676	211	0.472
023	4.167	087	1.136	151	0.658	215	0.463
027	3.571	091	1.087	155	0.641	219	0.455
031	3.125	095	1.042	159	0.625	223	0.446
035	2.778	099	1.000	163	0.610	227	0.439
039	2.500	103	0.962	167	0.595	231	0.431
043	2.273	107	0.926	171	0.581	235	0.424
047	2.083	111	0.893	175	0.568	239	0.417
051	1.923	115	0.862	179	0.556	243	0.410
055	1.786	119	0.833	183	0.543	247	0.403
059	1.667	123	0.806	187	0.532	251	0.397
063	1.563	127	0.781	191	0.521	255	0.391

6.11.1.3 CIR Receive Data 1(CIRDATA1) (Default Value: 0000_0000)

Read: CIR 1st Received Data Buffer

6.11.1.4 CIR Receive Data 1/2/3/4(CIRDATA1/2/3/4) (Default Value: 0000_0000)

Read: CIR 2nd Received Data Buffer

6.11.1.5 CIR Receive Data 1/2/3/4(CIRDATA1/2/3/4) (Default Value: 0000_0000)

Read: CIR 3rd Received Data Buffer

6.11.1.6 CIR Receive Data 1/2/3/4(CIRDATA1/2/3/4) (Default Value: 0000_0000)

Read: CIR 4th Received Data Buffer

6.12 A/D Converter Block

W83L951DG/FG provides 8 A/D inputs. Analog input pin is selected in A/D Converter Register 0. The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

Table 6-21 A/D Convert Register Define

A/D CONVERT BLOCK(4)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
50	AD1	ADCST	Analog Input Select			ADCC	Reserved	Analog [1:0]	
51	AD2	Analog [9:2]							
54	PADMODE	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Gray: Only with System Reset to initial.

6.12.1 Register Description

A/D converter is 10-bit converter. The V_{REF} is Input of VREF pin.

The formula: A/D converter result= (Analog [9:0] / 1024) × V_{REF}

6.12.1.1 A/D Converter Register 1 (AD1) (Default Value: 0000_00??)

Bit 7: ADC Start Bit

1: Start (Only one time)

0: No change.

When A/D Conversion Complete Status Bit is high, write 1 to this bit to start A/D convert. And ADC Start Bit keeps low until hardware receives this request and can receive next request. And ADC Start Bit changes from low to high at the time.

Bit 6~4: Analog Input Pin Select

000: GP60, 001: GP61, 010: GP62, 011: GP63,

100: GP64, 101: GP65, 110: GP66, 111: GP67.

Bit 3: A/D Conversion Complete Status Bit (Read Only)

0: Conversion in progress.

1: Conversion completed.

Bit 2: Reserved

Bit 1~0: A/D Converter Result [1:0]

A/D converter result bit1 is LSB.

When A/D Conversion Complete Status Bit is high, A/D Converter Result is valid.

6.12.1.2 A/D Converter Register 2 (AD2) (Default Value: ????_????)

Bit 7~0: A/D Converter Result [9:2]

A/D Converter Result bit 9 is MSB.

When A/D Conversion Complete Status Bit is high, A/D Converter Result is valid.

6.12.1.3 Pad Mode Register (PADMODE) (Default Value: 0000_0000)

Bit 7~0: Pad mode select

0: Normal Mode

1: AD Mode

6.13 D/A Converter Block

The keyboard controller has two internal D-A converters (DA2 and DA1) with 8-bit resolution. The result of D-A conversion is output to the DA2 or DA1 pin.

Table 6-22.D/A Converter Register Define

A/D CONVERT BLOCK(4)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
52	DA1	D/A 1 Convert Register [7:0]							
53	DA2	D/A 2 Convert Register [7:0]							

Note:

Gray: Only with System Reset to initial.

6.13.1 Register Description

6.13.1.1 D-A conversion register 1(DA1) (Default Value: 0000_0000)

$$V_{GP57} = V_{REF} \times (N/256)$$

VREF is the reference voltage.

6.13.1.2 D-A conversion register 2(DA2) (Default Value: 0000_0000)

$$V_{GP56} = V_{REF} \times (N/256)$$

VREF is the reference voltage.

6.14 Fan Tachometer Block

Fan Tachometer Block provides two groups of Fan Tachometer, can be by GP40, GP41 inputs the wave form and calculates automatically that corresponding Count of cycle of rotational speed is counted. When real RPM is lower than setting value, interrupt request will occur.

Table 6-23.Fan Tachometer Register Define

FAN BLOCK(2)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	FAN1	Fan 1 Count[7:0]							
01	FAN2	Fan 2 Count[7:0]							

Note:

Gray: Only with System Reset to initial.

6.14.1 Register Description

6.14.1.1 FAN 1/2 Count/Limit Register (FAN1/2) (Default Value: ????_????)

Read:

Input clock=24MHz :

Current Count. RPM = (60 × 1 × 10e6) / (2 × Count × 256) = 117187.5/Count

Input clock=12MHz :

Current Count. RPM = (60 × 1 × 10e6) / (4 × Count × 256) = 58593/Count.

Write:

Set Count of tolerance of minimum RPM. When real RPM is lower than setting value, interrupt request will occur. The relation between RPM and Count is as follows:

Input clock=24MHz :

RPM = (60 × 1 × 10e6) / (2 × Count × 256) = 117187.5/Count.

Count = 117187.5/RPM.

Input clock=12MHz :

RPM = (60 × 1 × 10e6) / (4 × Count × 256) = 58593/Count.

Count= 58593/RPM.

6.15 Real Time Clock Generator Block

Base on 32.768KHz, Real Time Clock Generator Block finishes counts which include seconds, minutes, and hours automatically. It also provides alarm function.

When {RTCHR, RTCMIN, RTCSEC} and {RTCHRAL, RTCMINAL, RTCSECAL} are equal, interrupt will occur to Microprocessor automatically.

Table 6-24.Real Time Clock Generator Register Define

REAL TIME CLOCK BLOCK(6)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
70	RTCSEC	RTC Seconds Register[7:0]							
71	RTCSECAL	RTC Seconds Alarm Register[7:0]							
72	RTCMIN	RTC Minutes Register[7:0]							
73	RTCMINAL	RTC Minutes Alarm Register[7:0]							
74	RTCHR	RTC Hours Register[7:0]							
75	RTCHRAL	RTC Hours Alarm Register[7:0]							

Note:

Gray: Only with System Reset to initial.

RTCSEC, RTCMIN, RTCHR should initial after local reset.

6.15.1 Register Description

6.15.1.1 RTC Second Register (RTCSEC) (Default Value: 0000_0000)

Read: Indicate RTC second value at present.

Write: Set RTC second value at present.

6.15.1.2 RTC Second Alarm Register (RTCSECAL) (Default Value: 0000_0000)

Read: Indicate RTC second alarm at present.

Write: Set RTC second alarm value at present.

6.15.1.3 RTC Minute Register (RTCMIN) (Default Value: 0000_0000)

Read: Indicate RTC minute value at present.

Write: Set RTC minute value at present.

6.15.1.4 RTC Minute Alarm Register (RTCMINAL) (Default Value: 0000_0000)

Read: Indicate RTC minute alarm value at present.

Write: Set RTC minute alarm value at present.

6.15.1.5 RTC Hour Register (RTCHR) (Default Value: 0000_0000)

Read: Indicate RTC hour value at present.

Write: Set RTC hour value at present.

6.15.1.6 RTC Hour Alarm Register (RTCHRAL) (Default Value: 0000_0000)

Read: Indicate RTC hour alarm minute value at present.

Write: Set RTC hour alarm value at present.

6.16 External Interrupt Control Block

About External Interrupt, in W83L951DG/FG, External Interrupt Group1 (EXTINT1[7:0]), External Interrupt Group2 (EXTINT2[7:0]) and External Interrupt Group3 (EXTINT3[7:0]) interrupt source pins are same as GPA[7:0], GPB[7:0] and GPC[7:0].

Table 6-25.External Interrupt Control Register Define

INTERRUPT BLOCK(17)									
EXTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
80	EXTINTE1	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10
81	EXTINTE2	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
82	EXTINTE3	INT37	INT36	INT35	INT34	INT33	INT32	INT31	INT30
83	EXTINTREQ1	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10
84	EXTINTREQ2	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
85	EXTINTREQ3	INT37	INT36	INT35	INT34	INT33	INT32	INT31	INT30
88	EXTINTT1	INT17	INT16	INT15	INT14	INT13	INT12	INT11	INT10
89	EXTINTT2	INT27	INT26	INT25	INT24	INT23	INT22	INT21	INT20
8A	EXTINTT3	INT33		INT32		INT31		INT30	
8B	EXTINTT4	INT37		INT36		INT35		INT34	

Note: All register initial after system reset.

6.16.1 Register Description

6.16.1.1 External Interrupt Enable 1/2/3 Register (EXTINTE1/2/3) (Default Value: 0000_0000)

1: Enable.

In enable state, external interrupt source will cause external interrupt request to generate the interrupt to Microprocessor.

0: Disable.

6.16.1.2 External Interrupt Request 1/2/3 Register (EXTINTREQ1/2/3) (Default Value: 0000_0000)

Bit7~0: External Interrupt Request

Read: 1: Requested, 0: No Requested.

Write: 1: Clear Request, 0: No Change

6.16.1.3 External Interrupt Trigger Select 1 Register (EXTINTT1) (Default Value: 0000_0000)

Bit 7~0:INT17~10 Trigger Type

Indicate the trigger type of External Interrupt 17~10.

1: Rising Edge

0: Falling Edge.

6.16.1.4 External Interrupt Trigger Select 2 Register (EXTINTT2) (Default Value: 0000_0000)

Bit 7~0:INT27~20 Trigger Type

Indicate the trigger type of External Interrupt 27~20.

1: Rising Edge

0: Falling Edge.

6.16.1.5 External Interrupt Trigger Select 3 Register (EXTINTT3) (Default Value: 0000_0000)

Bit 7~6:INT33 Trigger Type

Indicate the trigger type of External Interrupt 33.

1x: Rising Edge& Falling Edge,

01: Rising Edge,

00: Falling Edge

Bit 5~4:INT32 Trigger Type

Indicate the trigger type of External Interrupt 32.

1x: Rising Edge& Falling Edge,

01: Rising Edge,

00: Falling Edge

Bit 3~2:INT31 Trigger Type

Indicate the trigger type of External Interrupt 31.

1x: Rising Edge& Falling Edge,

01: Rising Edge,

00: Falling Edge

Bit 1~0:INT30 Trigger Type

Indicate the trigger type of External Interrupt 30.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

6.16.1.6 External Interrupt Trigger Select 4 Register (EXTINTT4) (Default Value: 0000_0000)

Bit 7~6:INT37 Trigger Type

Indicate the trigger type of External Interrupt 37.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

Bit 5~4:INT36 Trigger Type

Indicate the trigger type of External Interrupt 36.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

Bit 3~2:INT35 Trigger Type

Indicate the trigger type of External Interrupt 35.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

Bit 1~0:INT34 Trigger Type

Indicate the trigger type of External Interrupt 34.

1x: Rising Edge& Falling Edge,

01: Rising Edge

00: Falling Edge

6.17 Flash Memory

The W83L951DG/FG has a 64KByte, 3.3-volt only CMOS flash memory. The byte-wide (× 8) data appears on DQ7–DQ0. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is not required. The unique cell architecture of the Flash results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

6.17.1 External Programming Mode

The context of flash in Winbond Keyboard controller is empty by default. At the first use, you must program the flash by external writer device. For programming the flash by external device, the Winbond Keyboard controller must enter the flash-programming mode by TEST# Pin is connected to GND. RESET# Pin is connected to GND. FA [7:0] and FD [7:0] port is combined to GP07 to GP00. FA [7:0] is latched by the ALE (GP34).

In External Programming Mode, W83L951DG/FG protects Internal Flash data, so W83L951DG/FG will close “Read Command”. Under this condition, users must run “Erase Command” to use “Read Command”.

6.17.2 Internal Programming Mode

In W83L951DG/FG, in addition to access internal flash by outside, it provides to access SFR by Microprocessor. When Enable Memory Bit of Memory Mapping Control Register is high, and PC is F800~FFFFh, Microprocessor can access Internal Flash by SFR.

Table 6-26.Internal Programming Flash Register Define

INTERNAL PROGRAMMING FLASH									
INTADDR	**NAME**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F9	FCON	CEB	OEB	WEB	Reserved				EXCHANG_GP
FA	FADDH	A[15:8]							
FB	FADDL	A[7:0]							
FC	FDATA	DQ[7:0]							

6.17.2.1 Flash Control Register (FCON) (Default Value: 0000_0000)

6.17.2.2 Bit7: Flash Chip Select Enable (CEB)

Like CE# Pin. Refer to next section for further details.

Bit6: Flash Output Enable (OEB)

Like OE# Pin. Refer to next section for further details.

Bit5: Flash Write Enable (WEB)

Like WE# Pin. Refer to next section for further details.

Bit4~Bit1: Reserved

Bit0: Exchange GPIOA/B/C to GPIO1/0/3 Function (Reserved)

6.17.2.3 Flash Address High Byte Register (FADDH) (Default Value: 0000_0000)

Address [15:8] Input, Like A [15:8] Pin. Refer to next section for further details.

6.17.2.4 Flash Address Low Byte Register (FADDL) (Default Value: 0000_0000)

Address [7:0] Input, Like A [7:0] Pin. Refer to next section for further details.

6.17.2.5 Flash Data Register (FDATA) (Default Value: 0000_0000)

Write: Data Input

Read: Data Output

Like DQ [7:0] Pin. Refer to next section for further details.

6.17.3 Device Bus Operation

6.17.3.1 Read Mode

The read operation of the Internal Flash is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

6.17.3.2 Write Mode

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing #WE to logic low state, while #CE is at logic low state and #OE is at logic high state. Addresses are latched on the falling edge of #WE or #CE, whichever happens later; while data is latched on the rising edge of #WE or #CE, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

6.17.3.3 Output Disable Mode

With the #OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

6.17.3.4 Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on #OE, #CE, or #WE will not initiate a write cycle.

6.17.4 Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. "Command Definitions" defines the valid register command sequences.

6.17.4.1 Read Command

The device will automatically power-up in the read state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. The device will automatically returns to read state after completing an Embedded Program or Embedded Erase algorithm.

Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

6.17.4.2 Byte Program Command

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two "unlock" write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the embedded program algorithm. Addresses are latched on the falling edge of #CE or #WE, whichever happens later and the data is latched on the rising edge of #CE or #WE, whichever happens first. The rising edge of #CE or #WE (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see "Hardware Sequence Flags"). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for Data Polling operations. Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to program 0 back to 1, the toggle bit will stop toggling. Only erase operations can convert "0"s to "1"s.

Refer to the Programming Command Flow Chart using typical command strings and bus operations.

6.17.4.3 Chip Erase Command

Chip erase is a six-bus-cycle operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles are asserted, followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically erase and verify the entire memory for an all one data pattern. The erase is performed sequentially on each sectors at the same time (see "Feature"). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last #WE pulse in the command sequence and terminates when the data on DQ7 is "1" at which time the device returns to read the mode.

Refer to the Erase Command Flow Chart using typical command strings and bus operations.

6.17.5 Write Operation Status

6.17.5.1 DQ7: Data Polling

The W39L040 device features Data Polling as a method to indicate to the host that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7.

During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output.

Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce

a "1" at the DQ7 output. For chip erase, the Data Polling is valid after the rising edge of the sixth pulse in the six #WE write pulse sequences. For sector erase, the Data Polling is valid after the last rising edge of the sector erase #WE pulse. Data Polling must be performed at sector addresses within any of the sectors being erased. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable (#OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte′s valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see "Command Definitions").

6.17.5.2 DQ6: Toggle Bit

The Flash also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (#OE toggling) data from the device at any address will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth #WE pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth #WE pulse in the six write pulse sequence. For sector/page erase, the Toggle Bit is valid after the last rising edge of the sector/page erase #WE pulse. The Toggle Bit is active during the sector/page erase time-out.

Either #CE or #OE toggling will cause DQ6 to toggle.

6.17.6 Table of Operating Modes

Table 6-27.Device Bus Operations

MODE	#CE	#OE	#WE	A0	A1	DQ0~DQ7
Read	VIL	VIL	VIH	A0	A1	Dout
Write	VIL	VIH	VIL	A0	A1	Din
Standby	VIH	X	X	X	X	High Z
Output Disable	VIL	VIH	VIH	X	X	High Z

Table 6-28.Command Define

COMMAND DESCRIPTION	NO. OF CYCLE	1ST	2ND	3RD	4TH	5TH	6TH
		ADDR,DATA					
Read	1	Ain, Dout					
Byte Program	4	5555,AA	2AAA,55	5555,A0	Ain, Din		
Chip Erase	6	5555,AA	2AAA,55	5555,80	5555,AA	2AAA,55	5555,10
Page Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	PA 50
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit 1	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit 2	1	XXXX F0					

Notes:

1. Address Format: A14 ~ A0(Hex); Data Format: DQ7 ~ DQ0(Hex) .
2. Either one the two Product ID Exit commands can be used.
3. PA: Page Address = FXXXh to 0XXXh for page 15 to page 0.

6.17.7 Embedded Algorithm

6.17.7.1 Embedded Programming Algorithm

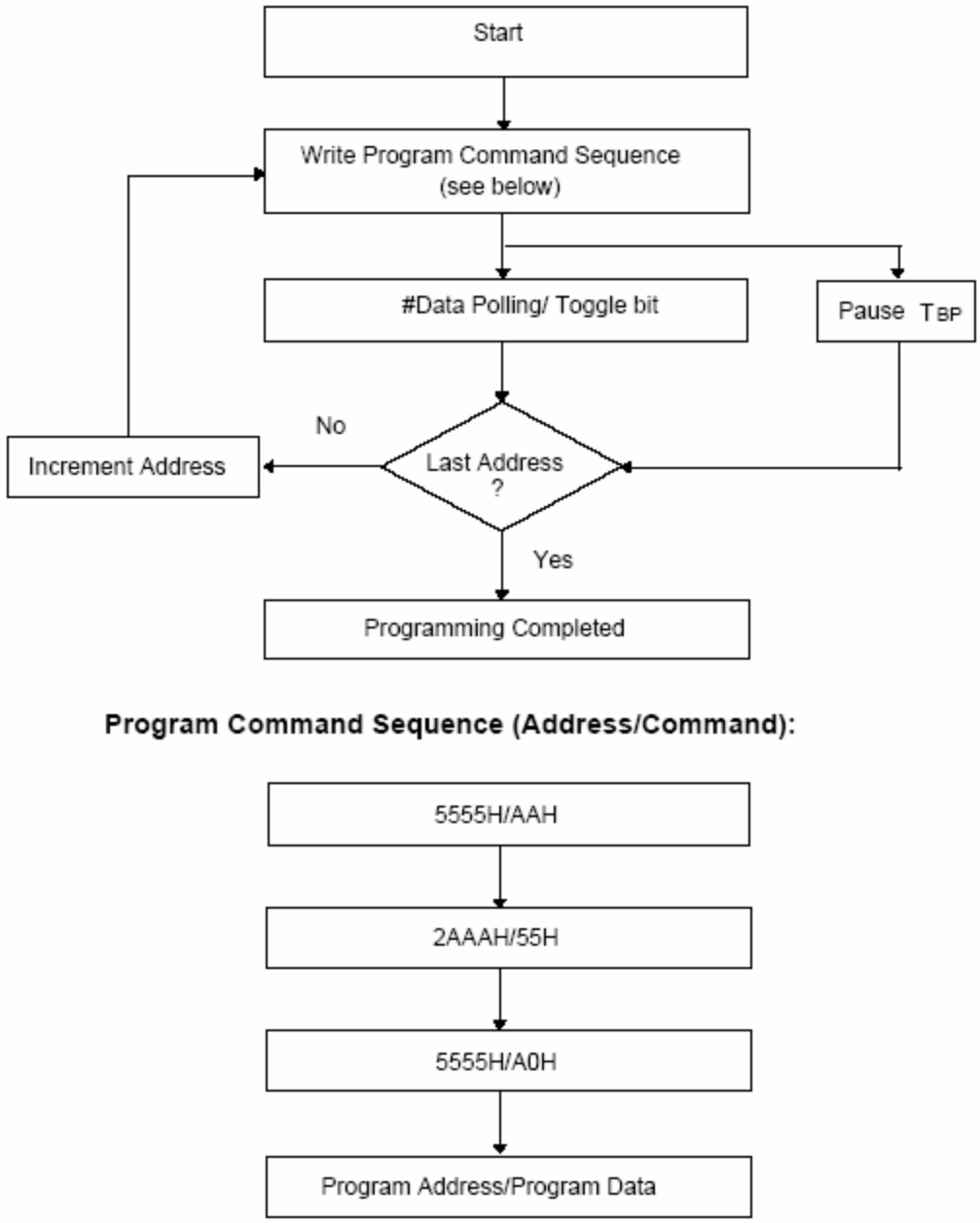


Figure 6-3.Embedded Programming Algorithm State Diagram

6.17.7.2 Embedded Erase Algorithm

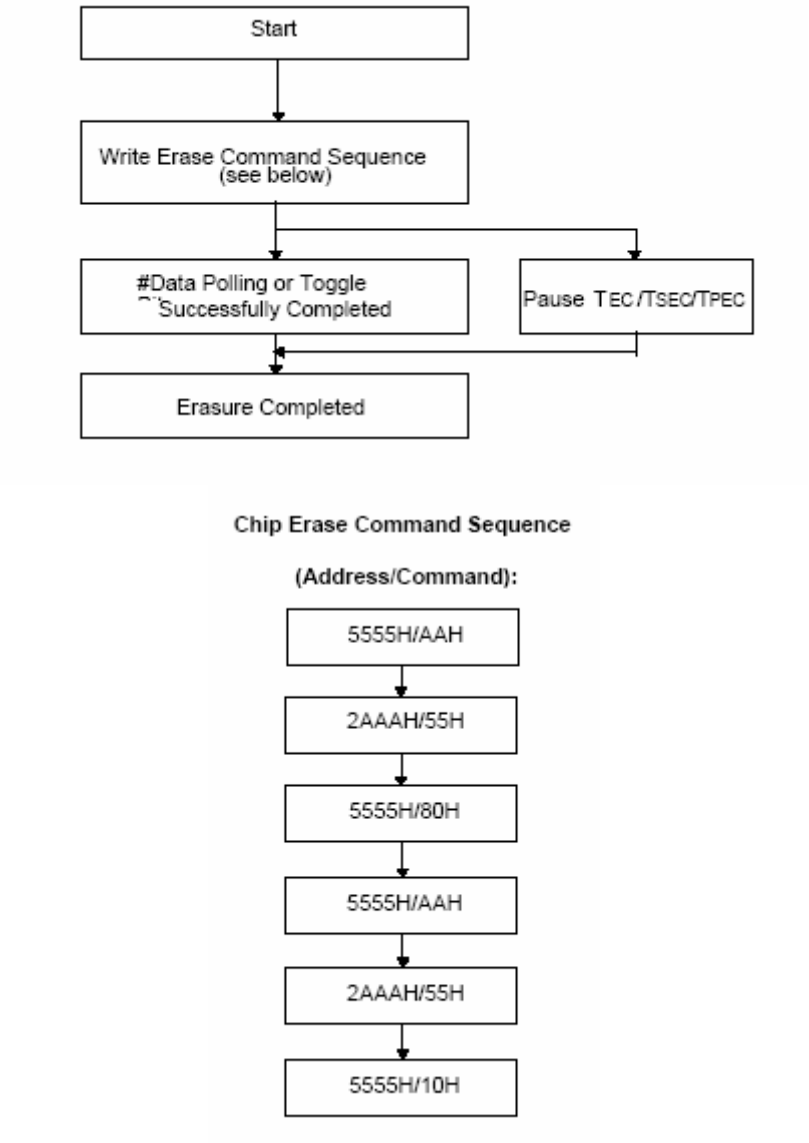


Figure 6-4.Embedded Erase Algorithm State Diagram

6.17.7.3 Embedded #Data Polling Algorithm

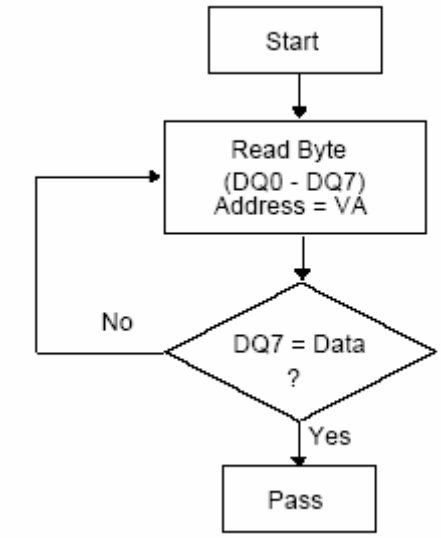


Figure 6-5.Embedded #Data Polling Algorithm State Diagram

Note: VA = Byte Address for programming

= Any Group Address during chip erase

6.17.7.4 Embedded Toggle Bit Algorithm

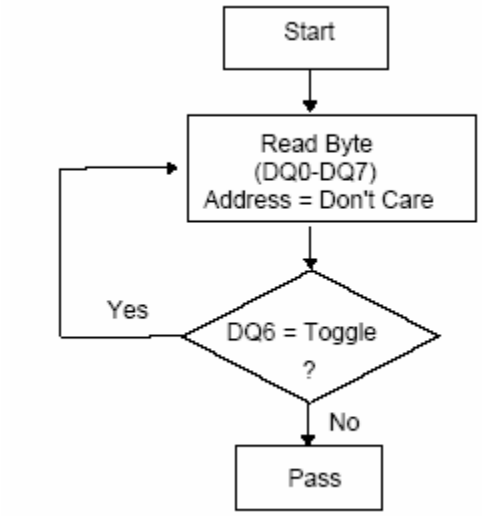


Figure 6-6.Embedded Toggle Bit Algorithm State Diagram

6.17.8 Timing Parameters

Table 6-29.Read Cycle Timing Parameters Table

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	TRC	90	-	ns
Chip Enable Access Time	TCE	-	90	ns
Address Access Time	TAA	-	90	ns
Output Enable Access Time	TOE	-	45	ns
#CE Low to Active Output	TCLZ	0	-	ns
#OE Low to Active Output	TOLZ	0	-	ns
#CE High to High-Z Output	TCHZ	-	25	ns
#OE High to High-Z Output	TOHZ	-	25	ns
Output Hold from Address Change	TOH	0	-	ns

Note: (VDD = 3.3V ±0.3V, VSS = 0V, TA = 0 to 70° C or -40 to 85° C)

Table 6-30.Write Cycle Timing Parameters Table

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	40	-	-	nS
#WE and #CE Setup Time	TCS	0	-	-	nS
#WE and #CE Hold Time	TCH	0	-	-	nS
#OE High Setup Time	TOES	0	-	-	nS
#OE High Hold Time	TOEH	0	-	-	nS
#CE Pulse Width	TCP	100	-	-	nS
#WE Pulse Width	TWP	100	-	-	nS
#WE High Width	TWPH	100	-	-	nS
Data Setup Time	TDS	40	-	-	nS
Data Hold Time	TDH	10	-	-	nS
Byte Programming Time	TBP	-	35	50	μS
Chip Erase Cycle Time	TEC	-	50	100	mS
Sector/Page Erase Cycle Time	TEP	-	12.5	25	mS

Table 6-31.Power-up Timing Parameters Table

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	μS
Power-up to Write Operation	TPU. WRITE	5	mS

6.17.9 Timing Waveforms

The Timing Waveforms don't contain ALE(GP34 and TS(GP33). If using External Mode to access, TS pin must keep low. And use ALE(GP34) to do Low Address Byte(GP0) latch. ALE is high active and pulse width is at least 50ns. Low Address Byte(GP0) must be stable before ALE changes state from high to low.

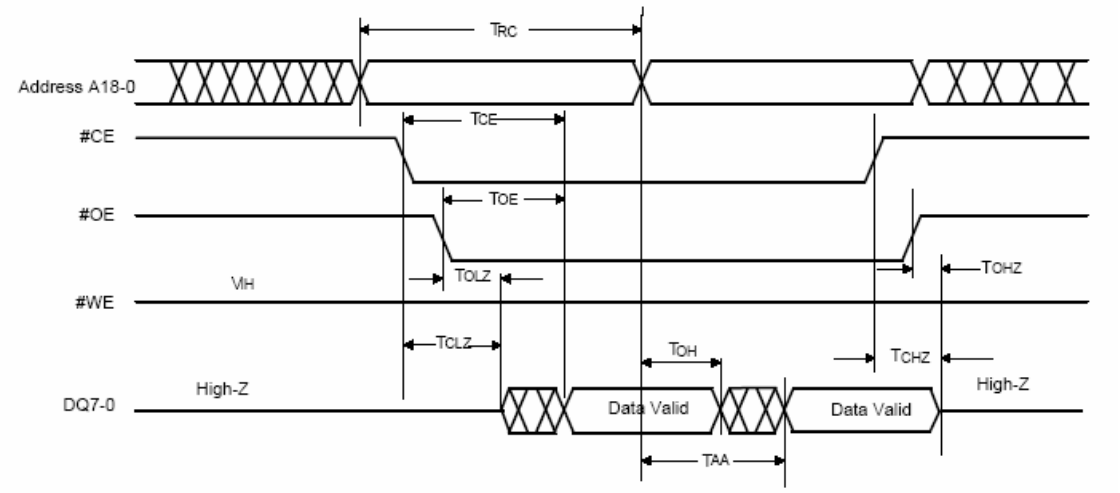


Figure 6-7.Read Cycle Timing Diagram

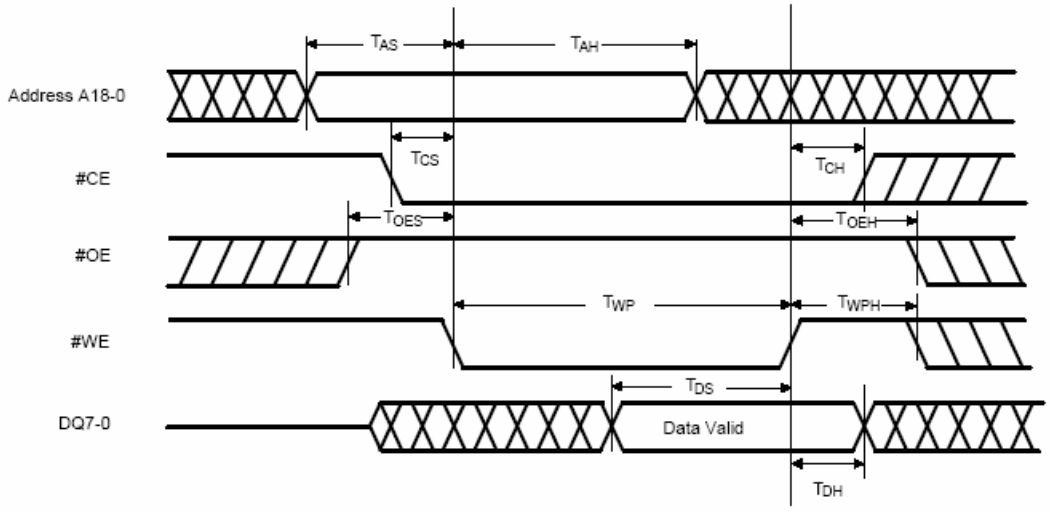


Figure 6-8.#WE Controlled Command Write Cycle Timing Diagram

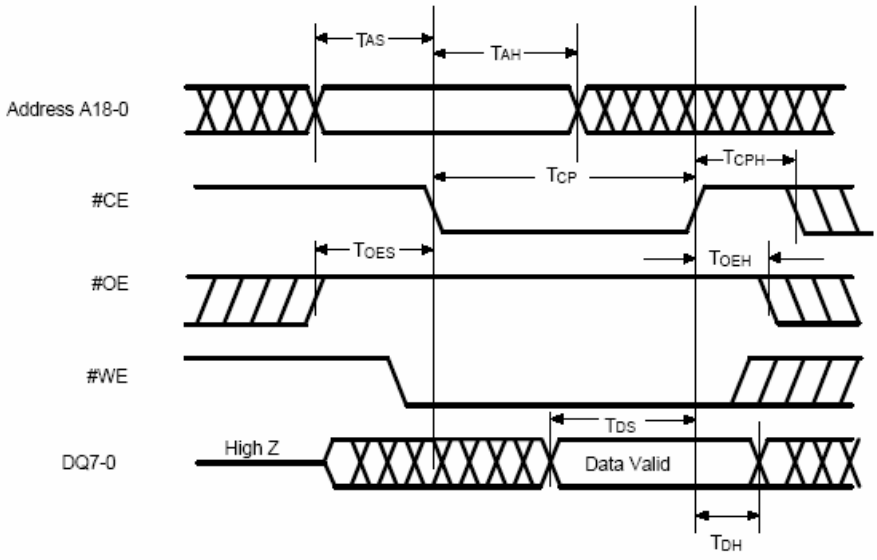


Figure 6-9.#CE Controlled Command Write Cycle Timing Diagram

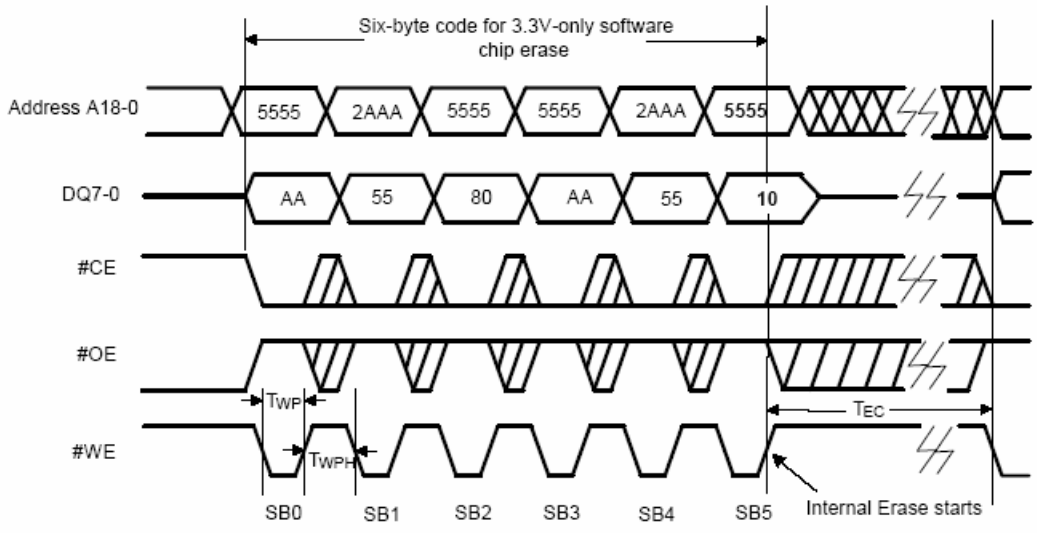


Figure 6-10.Chip Erase Timing Diagram

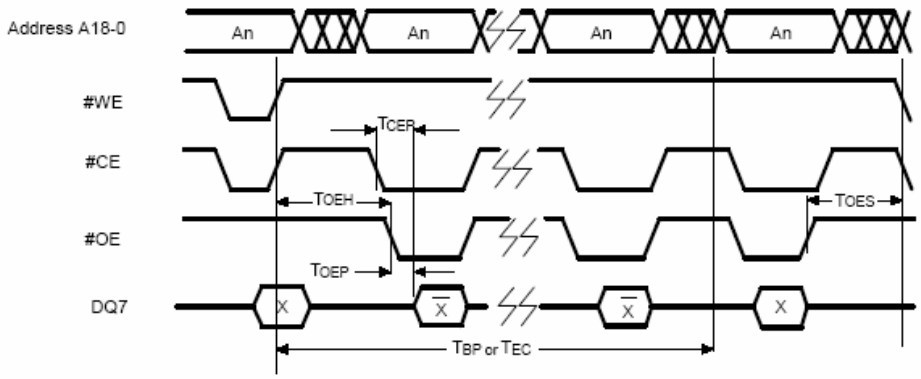


Figure 6-11.Data Polling Timing Diagram

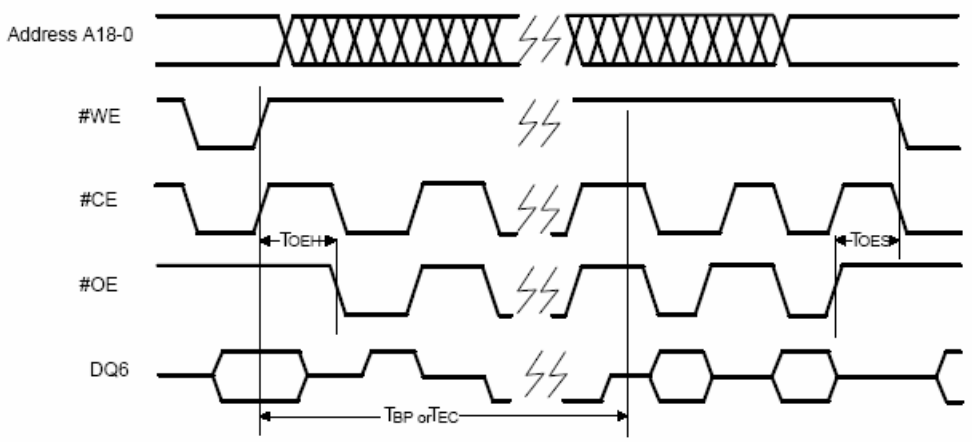


Figure 6-12.Toggle Bit Timing Diagram

7. SPECIFICATIONS

7.1 Absolute Maximum Ratings

Table 7-1 Absolute Maximum Rating Table

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to +4.6	V
Input Voltage	3.3 ± 10%	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +125	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 Analog Characteristics

7.2.1 ADC Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Resolution		10		Bit
Input Accuracy			±3	LSB
Input Voltage Range			AVcc	V
Voltage Conversion Duration			1	ms

7.2.2 DAC Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Resolution		8		Bit
Offset Error			±2	LSB
Output Voltage Range			AVcc	V
DAC Enable Delay			10	μs

7.3 Power Supply Current Consumption

Table 7-2 Power Supply Current Consumption Table

PARAMETER	TYPICAL	UNIT	PIN CONDITIONS
Normal Mode	30	mA	Output , No Load
Power Down Mode	10	uA	

7.4 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{12tsm}—Bi-directional pin, TTL level, Schmitt-trigger input, selectable 250uA/12mA sink capability, 12mA source capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA / -250uA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{12tsai} — Bi-directional pin, TTL level, Schmitt-trigger input, Analog Input, 12mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{12tsao} — Bi-directional pin, TTL level, Schmitt-trigger input, Analog Output, 12mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{16tsh} — Bi-directional pin, TTL level, Schmitt-trigger input, 5V Tolerant, 16mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	2.4			V	IOH = -16 mA

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I/O_{24ts} — Bi-directional pin, TTL level, Schmitt-trigger input, 16mA source-sink capability						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Output High Voltage	VOH	2.4			V	IOH = -24 mA

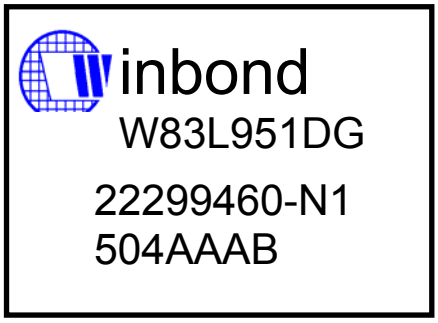
(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

I_{ts} — Input pin, TTL level, Schmitt-trigger input						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL			-1	μA	VIN = 0 V

8. ORDERING INSTRUCTION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83L951DG	128PIN LQFP (LEADFREE)	Commercial, 0°C to +70°C
W83L951FG	128PIN QFP (LEADFREE)	Commercial, 0°C to +70°C

9. HOW TO READ THE TOP MARKING



1st line: Winbond logo

2nd line: W83L951DG, chip part number for Leadfree product

3rd line: Manufacture tracking code 22299460-N1

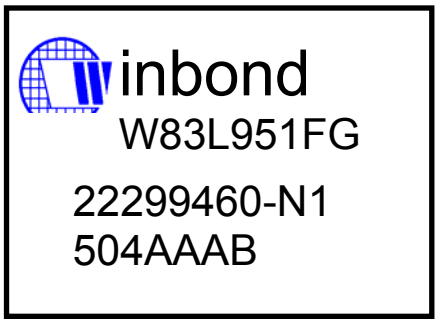
4th line: Tracking code 504 A A AB

504: Packages made in '03, week 04

A: Assembly house ID; A means ASE, O means OSE, G means GR…

A: IC revision

AB: Internal version



1st line: Winbond logo

2nd line: W83L951FG, chip part number for Leadfree product

3rd line: Manufacture tracking code 22299460-N1

4th line: Tracking code 504 A A AB

504: Packages made in '03, week 04

A: Assembly house ID; A means ASE, O means OSE, G means GR…

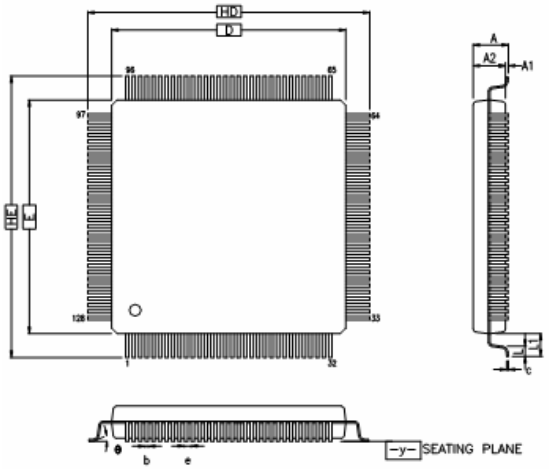
A: IC revision

AB: Internal version

10. PACKAGE DIMENSIONS

Winbond provides two packages for customers that contain 128- pin LQFP and 128-pin QFP.

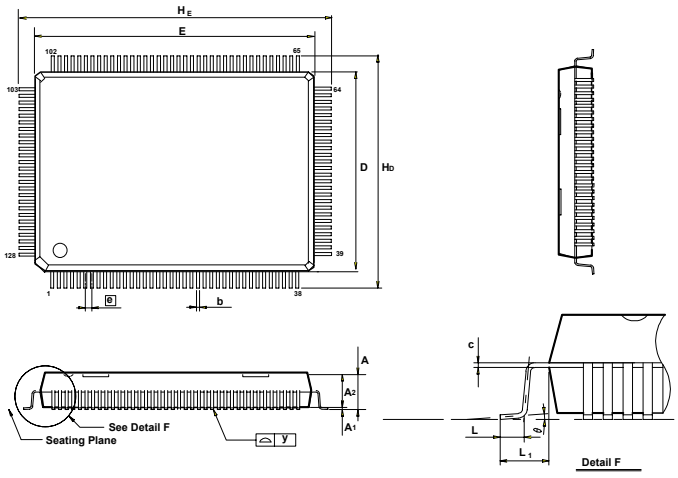
128-pin LQFP



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

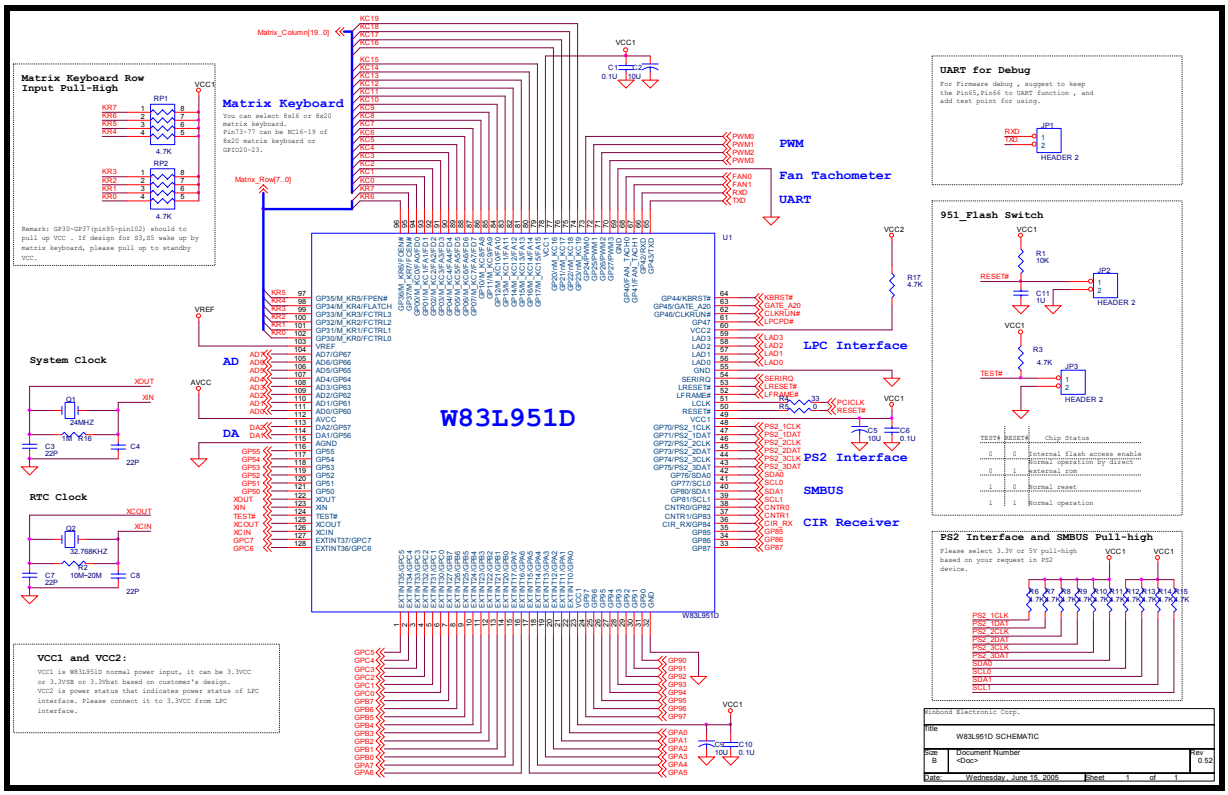
128pin- QFP



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.25	0.35	0.45	0.010	0.014	0.018
A2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
HD	17.00	17.20	17.40	0.669	0.677	0.685
HE	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

11. DEMO CIRCUITS



Important Notice

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Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

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