3 V SILICON MMIC L-BAND FREQUENCY DOWN CONVERTER

FEATURES

- HIGH DENSITY SURFACE MOUNTING: 6 Pin Super Minimold or SOT-363 Package
- BROADBAND OPERATION: RF = 0.8 to 2.0 GHz IF = 100 to 300 MHz
- INPUT IP3: -7 dBm

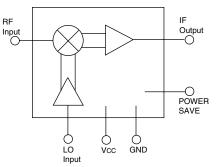
POWER SAVE FUNCTION

• SUPPLY VOLTAGE: Vcc = 2.7 to 3.3 V

DESCRIPTION

NEC's UPC8112TB is a silicon RFIC manufactured using the NESAT III process. This device consists of a mixer, an IF amplifier and a LO buffer amplifier. This device is suitable as a 1st IF downconverter for the receiver stage of cellular and other wireless systems. The UPC8112TB is pin compatible and has comparable performance as the larger UPC8112T, so

INTERNAL BLOCK DIAGRAM



UPC8112TB

it is suitable for use as a replacement to help reduce system size. The IC is housed in a 6 pin super minimold or SOT-363 package.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (TA = 25 °C, VCC = VPS = 3.0 V, PLO = -10 dBm)

PART NUMBER PACKAGE OUTLINE			UPC8112TB S06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	ТҮР	MAX
Icc	Circuit Current (no input signal) Vcc = 3.0 V	mA	4.9	8.5	11.7
	VPS = 0.5 V	μA			0.1
fRFin	RF Frequency Response	GHz	0.8	1.9	2.0
fIFout	IF Frequency Response ¹	MHz	100	250	300
CG	Conversion Gain fRFin = 900 MHz, fLOin = 1000 MHz	dB	11.5	15	17.5
	$f_{\rm RFin} = 1.5 \text{GHz}, f_{\rm LOin} = 1.6 \text{GHz}$	dB		13	
	fRFin = 1.9 GHz, fLOin = 1.66 GHz	dB	9.5	13	15.5
NF	Single Side Band Noise Figure (SSB)				
	fRFin = 900 MHz, fLOin = 1000 MHz	dB		9.0	11
	fRFin = 1.5 GHz, fLOin = 1.6 GHz	dB		11	
	fRFin = 1.9 GHz, fLOin = 1.66 GHz	dB		11.2	13.2
P1dB	Output Power at 1 dB gain compression, fRFin = 1.9 GHz				
	fLOin = 1.66 GHz	dBm		-5	
PSAT	Saturated Output Power fRFin = 900 MHz, fLOin = 1000 MHz	dBm	-6.5	-2.5	
	fRFin = 1.9 GHz, fLOin = 1.66 GHz	dBm	-7	-3	
	(PRFin = -10 dBm)				
IIP3	Input 3rd Order Intercept Point,				
	frfin = 900 MHz, floin = 1000 MHz	dBm		-10	
	fRFin = 1.5 GHz, fLOin = 1.6 GHz	dBm		-9	
	fRFin = 1.9 GHz, fLOin = 1.66 GHz	dBm		-7	
LOrf	LO Leakage at RF pin, fRFin = 900 MHz, fLoin = 1000 MHz	dBm		-45	
	fRFin = 1.5 GHz, fLOin = 1.6 GHz	dBm		-46	
	frifin = 1.9 GHz, floin = 1.66 GHz	dBm		-45	
LOIF	LO Leakage at IF pin, frein = 900 MHz, floin = 1000 MHz	dBm		-32	
	fRFin = 1.5 GHz, fLOin = 1.6 GHz	dBm		-33	
	frefin = 1.9 GHz, floin = 1.66 GHz	dBm		-30	
RFLO	RF Leakage at LO Pin frein = 900 MHz, fLoin = 1000 MHz ²	dBm		-80	
	$f_{\text{RFin}} = 1.5 \text{ GHz}, f_{\text{LOin}} = 1.6 \text{ GHz}^2$	dBm		-57	
	$f_{RFin} = 1.9 \text{ GHz}, f_{LOin} = 1.66 \text{ GHz}^2$	dBm		-55	
Rth(JA)	Thermal Resistance (Junction to Ambient) Mounted on a				
` '	50 x 50 x 1.6 mm epoxy glass PWB	°C/W			325

Notes: 1. External matching required.

2. PRFin = -30 dBm

-California Eastern Laboratories

ABSOLUTE MAXIMUM RATINGS¹ (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
Vcc	Supply Voltage	V	3.6
Icc	Circuit Current	mA	77.7
PD	Power Dissipation ²	mW	200
Тор	Operating Temperature	°C	-40 to +85
Tstg	Storage Temperature	°C	-55 to +150

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.

2. Mounted on a 50 x 50 x 1.6 mm epoxy glass PWB (TA = +85°C).

PIN FUNCTIONS

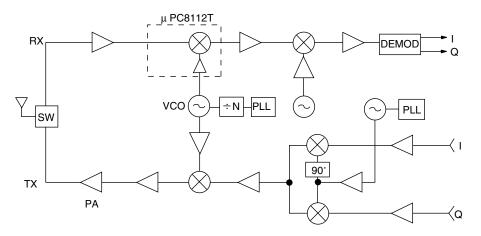
RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	ТҮР	MAX
Vcc	Supply Voltage	V	2.7	3.0	3.3
Тор	Operating Temperature	°C	-40	+25	+85
PLOin	LO Input Level	dBm	-15	-10	0
fRFin	RF Input Frequency	GHz	0.8	1.9	2.0
fIFout	IF Output Frequency	MHz	100	250	300

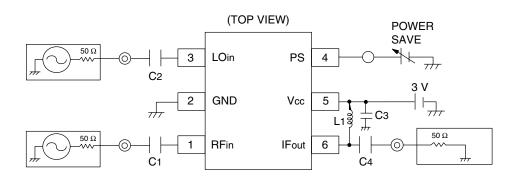
Pin No.	Symbol	Pin Voltage	Description	Internal Equivalent Circuit
5	Vcc	2.7 ~ 3.3	Supply Voltage pin. Connect a bypass capacitor (e.g., 1000 pF) to minimize ground impedance.	5
6	ΙΓουτ	Same as Vcc voltage through external inductor	IF output pin is an open collector with high impedance. External LC matching circuit is required.	from LO AMP
1	RFin	1.2	RF input pin to mixer. Mixer is a double balanced Gilbert cell type. Input RF signal to the pin with a 50 Ω source impedance through a coupling capacitor.	
2	GND	0	Ground pin. Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible to minimize ground impedance.	
3	LOIN	1.4	LO input pin to a differential buffer amplifier. Input LO signal through a coupling capacitor. Recom- mended input level: -15 to 0 dBm.	5 3 (2) (5) (1) (1) (1) (1) (1) (1) (1) (1
4	VPS	Vcc or GND	Power-save control pin. Voltage on this pin controls ON/OFF operation as follows: Operation VPs ON ≥2.5 V OFF 0-0.5 V	

TYPICAL APPLICATION EXAMPLE

PCS or DIGITAL CELLULAR



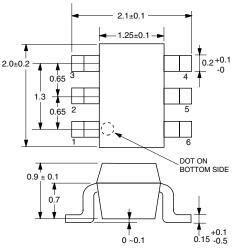
TEST CIRCUIT



Note: 1. C1, C2, C3 are 1,000 pF capacitors. 2. L1 and C4 are matching elements. L1 = 100nH and C4 = 2.7 pF for fIF = 240 MHz

OUTLINE DIMENSIONS (Units in mm)

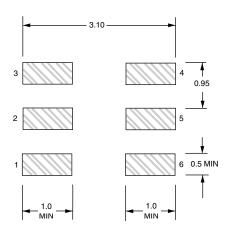
PACKAGE OUTLINE S06



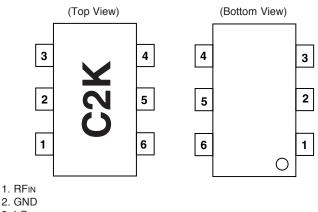
RECOMMENDED P.C.B. LAYOUT (Units in mm)

Note:

All dimensions are typical unless otherwise specified.



LEAD CONNECTIONS



3. LOIN

4. PS

5. Vcc

6. IFout

ORDERING INFORMATION

PART NUMBER	QTY
UPC8112TB-E3-A	3K/Reel

Note:

Embossed tape, 8 mm wide. Pins 1, 2, 3 are in tape pull-out direction.

Life Support Applications

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Mercury	< 1000 PPM	Not Detected	
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Hexavalent Chromium	< 1000 PPM	Not Detected	
РВВ	< 1000 PPM	Not Detected	
PBDE < 1000 PPM Not Dete		etected	

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