



# TSM4835

## 30V P-Channel Enhancement Mode MOSFET

SOP-8



Pin assignment:  
 1. Source 8. Drain  
 2. Source 7. Drain  
 3. Source 6. Drain  
 4. Gate 5. Drain

$V_{DS} = -30V$   
 $R_{DS(on)}, V_{GS} @ -10V, I_{DS} @ -9.5A = 18m\Omega$   
 $R_{DS(on)}, V_{GS} @ -4.5V, I_{DS} @ -7.5A = 30m\Omega$

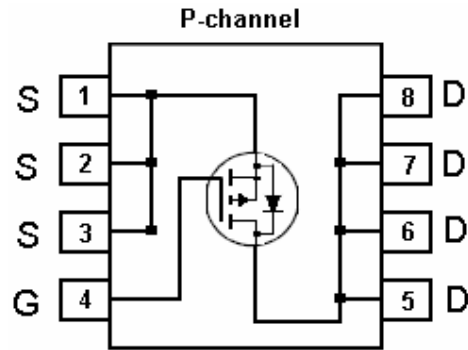
### Features

- ◇ Advanced trench process technology
- ◇ High density cell design for ultra low on-resistance
- ◇ High gate voltage

### Ordering Information

Part No.	Packing	Package
TSM4835CS	Tape & Reel	SOP-8

### Block Diagram



### Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	- 30	V	
Gate-Source Voltage	$V_{GS}$	± 25	V	
Continuous Drain Current, $V_{GS} @4.5V$ .	$I_D$	- 9.5	A	
Pulsed Drain Current, $V_{GS} @4.5V$	$I_{DM}$	- 50	A	
Maximum Power Dissipation	$P_D$	Ta = 25 °C	2.5	W
		Ta > 25 °C	1.6	W
Operating Junction Temperature	$T_J$	+150	°C	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C	

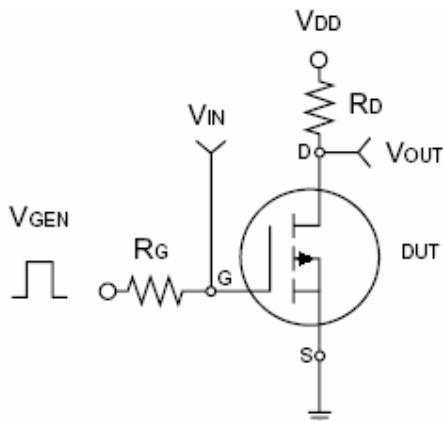
### Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta ja}$	50	°C/W

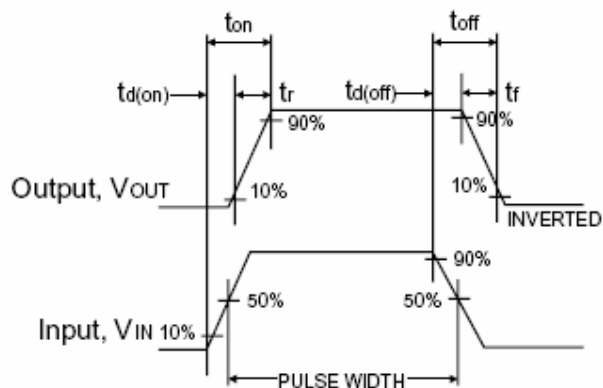
Note: Surface mounted on FR4 board  $t \leq 5sec$ .

Electrical Characteristics						
Ta = 25°C, unless otherwise noted						
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	BV <sub>DSS</sub>	-30	--	--	V
Drain-Source On-State Resistance	V <sub>GS</sub> = -10V, I <sub>D</sub> = -9.5A	R <sub>DS(ON)</sub>	--	13	18	mΩ
Drain-Source On-State Resistance	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -7.5A	R <sub>DS(ON)</sub>	--	22	30	
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	V <sub>GS(TH)</sub>	-1	--	-3	V
Zero Gate Voltage Drain Current	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V	I <sub>DSS</sub>	--	--	-1.0	μA
Gate Body Leakage	V <sub>GS</sub> = ±25V, V <sub>DS</sub> = 0V	I <sub>GSS</sub>	--	--	±100	nA
Forward Transconductance	V <sub>DS</sub> = -15V, I <sub>D</sub> = -8A	g <sub>fs</sub>	--	22	--	S
<b>Dynamic</b>						
Total Gate Charge	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4.6A, V <sub>GS</sub> = -5V	Q <sub>g</sub>	--	23	34	nC
	V <sub>DS</sub> = -15V, I <sub>D</sub> = -4.6A, V <sub>GS</sub> = -10V		--	54	60	
Gate-Source Charge	V <sub>GS</sub> = -10V	Q <sub>gs</sub>	--	8.5	--	nC
Gate-Drain Charge		Q <sub>gd</sub>	--	10.3	--	
Turn-On Delay Time	V <sub>DD</sub> = -15V, R <sub>L</sub> = 15Ω, I <sub>D</sub> = -1A, V <sub>GEN</sub> = -10V, R <sub>G</sub> = 6Ω	t <sub>d(on)</sub>	--	24	30	nS
Turn-On Rise Time		t <sub>r</sub>	--	12	30	
Turn-Off Delay Time		t <sub>d(off)</sub>	--	78	120	
Turn-Off Fall Time		t <sub>f</sub>	--	37	80	
Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1.0MHz	C <sub>iss</sub>	--	2520	--	pF
Output Capacitance		C <sub>oss</sub>	--	490	--	
Reverse Transfer Capacitance		C <sub>rss</sub>	--	330	--	
<b>Source-Drain Diode</b>						
Max. Diode Forward Current		I <sub>S</sub>	--	--	-2.1	A
Diode Forward Voltage	I <sub>S</sub> = -2.1A, V <sub>GS</sub> = 0V	V <sub>SD</sub>	--	-0.77	-1.2	V

Note : pulse test: pulse width ≤300μs, duty cycle ≤2%



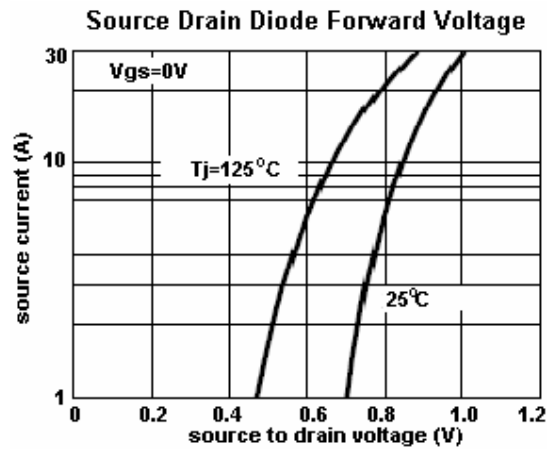
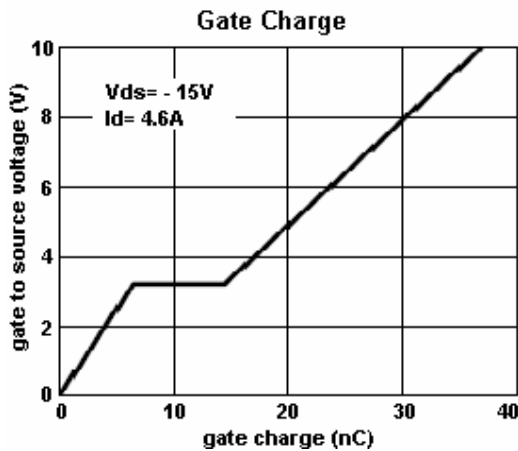
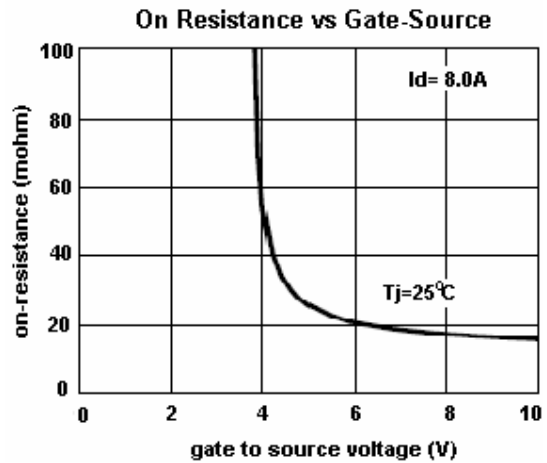
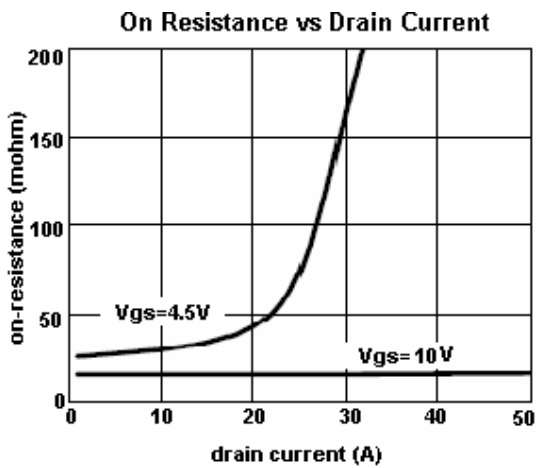
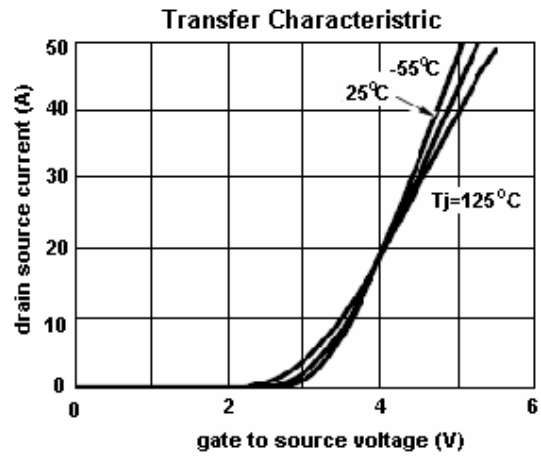
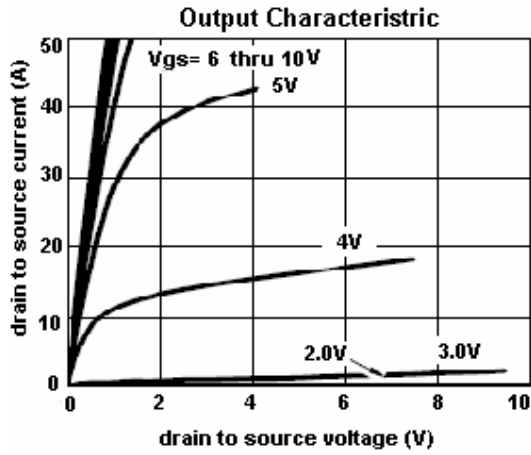
Switching Test Circuit



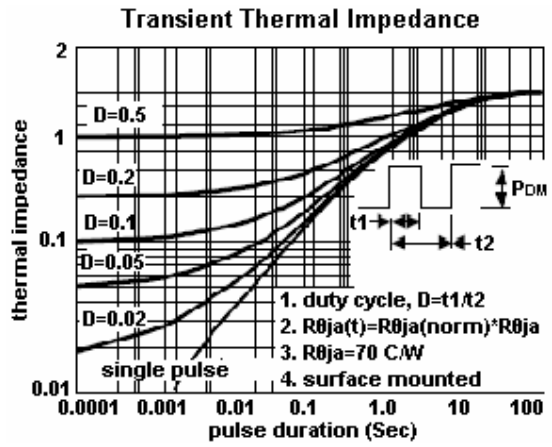
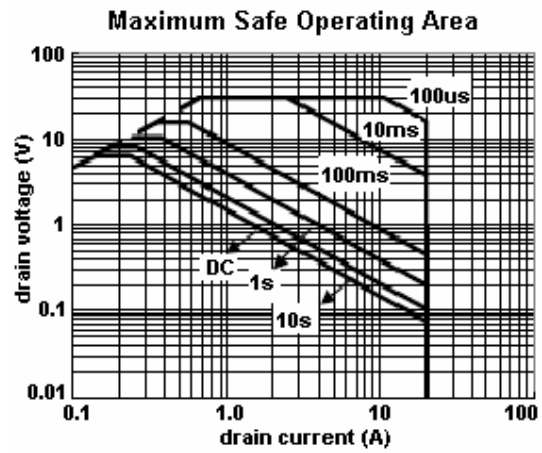
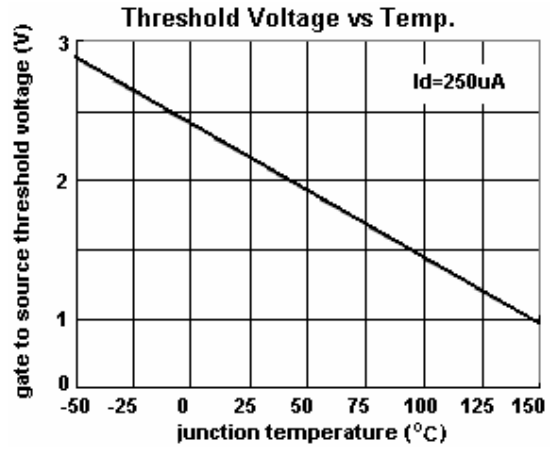
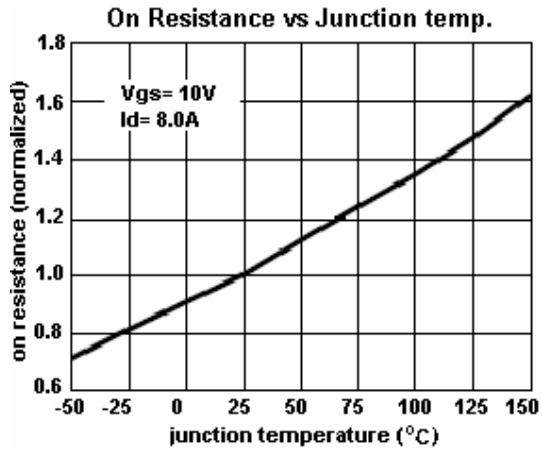
Switchin Waveforms



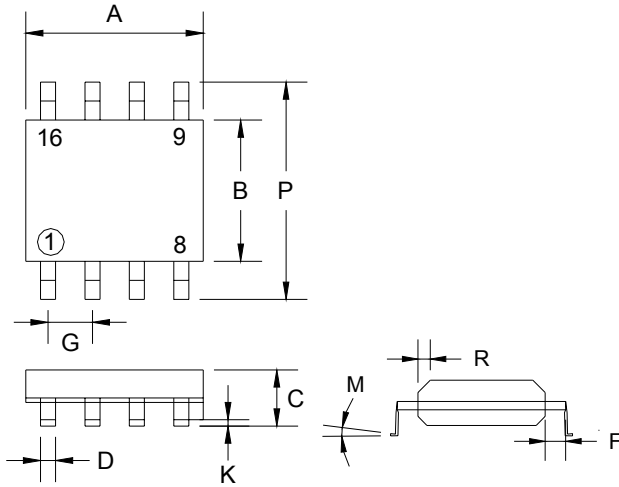
**Typical Characteristics Curve** (Ta = 25 °C unless otherwise noted)



### Electrical Characteristics Curve (continued)



## SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 (typ)		0.05 (typ)	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019