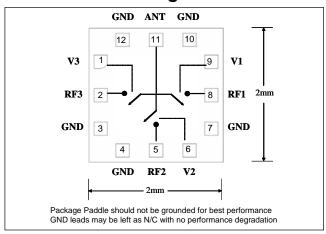


Functional Block Diagram



Product Description

TriQuint's TQP4M3019 is a high power antenna switch in a single pole three throw (SP3T) configuration. The die utilizes TriQuint's PHEMT MMIC switch process to provide optimized cross-modulation performance for use in CDMA applications. PHEMT Switches are a very low DC current replacement for classic PIN diode based switches. This product is ideally suited to applications where the antenna of a CDMA handset is to be routed to the Cellular duplexer, the PCS duplexer and the GPS receiver input. The design is symmetric and broadband allowing the user to assign cellular, PCS and GPS to ports RF1, RF2 or RF3 as desired.

Electrical Specifications^{1, 2}

Parameter	Min	Тур	Max	Units
Cellular Insertion Loss		0.50		dB
GPS Insertion Loss		0.52		dB
PCS Insertion Loss		0.60		dB
Cellular Isolation		27		dB
GPS Isolation		24		dB
PCS Isolation		22		dB
Cellular Cross-Modulation ²		-108	-100	dBm
PCS Cross-Modulation ²	•	-105	-100	dBm

Note 1: Test Conditions Zo = 50 ohms: Vcontrol =0V/2.6V, Tc=25°C.

Note 2: Cross-Modulation Test Conditions:

Cellular: PTx1 = 23 dBm @ 836 MHz, PTx2 = 23 dBm @ 837 MHz, $P_{int} = -23 \text{ dBm } @ 881.5 \text{ MHz}$ PCS: PTx1 = 23 dBm @ 1879.5 MHz, PTx2 = 23 dBm @ 1880.5 MHz, $P_{int} = -23 \text{ dBm } @ 1960 \text{ MHz}$

Features

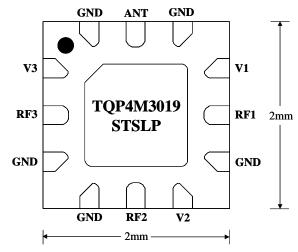
- pHEMT GaAs MMIC Die
- Excellent Cross-Modulation Performance
 - -108 dBm Typ @ Cellular
 - -105 dBm @ PCS
- Excellent ESD Rating: 300V HBM, 2000V CDM
- Low Control Voltage Operation to +2.6V
- High Isolation: 22dB typ at PCS Band
- Very Low Control Current: 10 μA typ
- Low Insertion Loss: 0.6 dB typ at PCS Band
- Small Footprint 2.0 x 2.0 mm 12 lead STSLP Package

Applications

 CDMA Handset Antenna Switch for Cellular, PCS and GPS operation.

Package Styles

12ld STSLP





Absolute Maximum Ratings

Symbol	Parameter	Absolute Maximum Value	Units
P _{IN Max}	Maximum Input Power	+38	dBm
Vctrl	Control Voltage	+/- 6	VDC
Tc	Case Temperature, Survival	-40 to +85	°C
T _{STG}	Storage Temperature	-40 to +150	°C

Note: The part may not survive all maximums applied simultaneously.

Electrical Characteristics^{1,2}

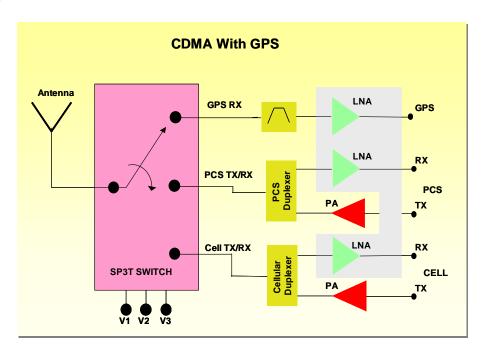
Parameter (all paths)	Test Conditions		Min	Тур	Max
Cellular Insertion Loss	Antenna to Selected Port (824 – 894 MHz)			0.50	
GPS Insertion Loss	Antenna to Selected RF Port (1574 – 1577 MHz)			0.52	
PCS Insertion Loss	Antenna to Selected RF Port (1850 – 1990 MHz)			0.60	
Cellular Isolation	RF Off Port to Selected RF On Port (824 – 894 MHz)	dB		27	
GPS Isolation	RF Off Port to Selected RF On Port (1574 – 1577 MHz)	dB		24	
PCS Isolation	RF Off Port to Selected RF On Port (1850 – 1990 MHz)	dB		22	
Cellular Cross-Modulation	PTx1 = 23 dBm @ 836 MHz, PTx2 = 23 dBm @ 837 MHz, P _{int} = -23 dBm @ 881.5 MHz			-108	-100
PCS Cross-Modulation	PTx1 = 23 dBm @ 1879.5 MHz, PTx2 = 23 dBm @ 1880.5 MHz, P _{int} = -23 dBm @ 1960 MHz			-105	-100
Cellular IIP3	Two tones; +23 dBm each; 837 MHz and 838 MHz			+66	
PCS IIP3	Two tones; +23 dBm each; 1880 MHz and 1881 MHz			+66	
2 nd Harmonic	Cellular; @ +25.5 dBm input dBc			-93	
2 nd Harmonic	PCS; @ +24 dBm input	dBm input dBc -9:		-93	
3 rd Harmonic	Cellular; @ +25.5 dBm input	dBc		-93	
3 rd Harmonic	PCS; @ +24 dBm input	dBc		-95	
P-0.1 dB	Cellular			+34	
P-0.1 dB	PCS			+34.5	
Return Loss	0.5 to 2.0GHz			-25	
Leakage Current	-			10	
Trise, Tfall	10% to 90% RF , 90% to 10% RF				1
Ton , Toff	50% control to 90% RF, and 50% control to 10% RF				1

Note 1: External DC Blocking capacitors are required at all RF ports.

Note 2: Test Conditions Zo = 50 ohms: Vcontrol =0V/2.6V, Tc=25°C.



Application Example



Truth Table 1,2,3,4,5

V1	V2	V3	ANT- RF1	ANT- RF2	ANT- RF3
1	0	0	On	Off	Off
0	1	0	Off	On	Off
0	0	1	Off	Off	On

Note 1: State 1 = +2.6V; State 0 = 0V

Note 2: Differential voltage from State 1 to State 0 must be a minimum of 2.6V Note 3: DC grounding is not required. Control voltages applied to pins 1, 6 and 9 are differential, being 0v and 2.6V nominally.

Note 4: The package center paddle is n/c = no connection and not grounded as the preferred user configuration. RF performance figures are quoted with n/c.. Note 5: The package pins 3, 4, 7, 10 and 11 can be n/c or grounded with the same performance. There are no internal connections between these pads and the die.

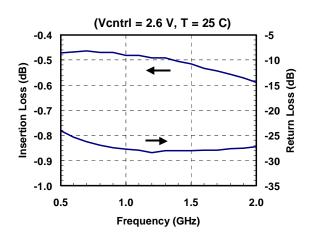
Pin Descriptions 1,2,3,4,5

Pad Number	Pad Name	Description
1	V3	Control RF Port 3
2	RF3	RF Port 3
3	GND⁵	Ground
4	GND⁵	Ground
5	RF2	RF Port 2
6	V2	Control RF Port 2
7	GND⁵	Ground
8	RF1	RF Port 1 Port
9	V1	Control RF Port 1
10	GND⁵	Ground
11	ANT	ANTENNA
12	GND ⁵	Ground

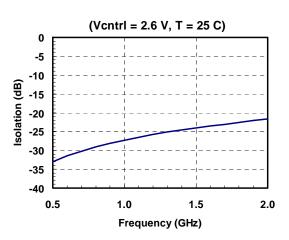


Typical Performance

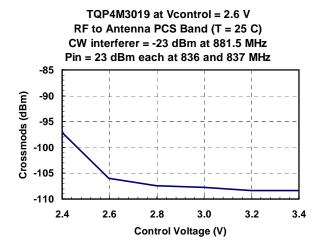
Insertion Loss and Match



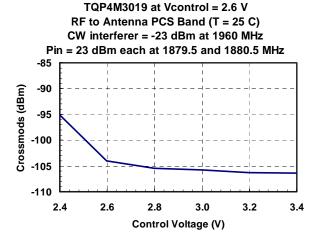
Isolation



Low Band Cross Modulation

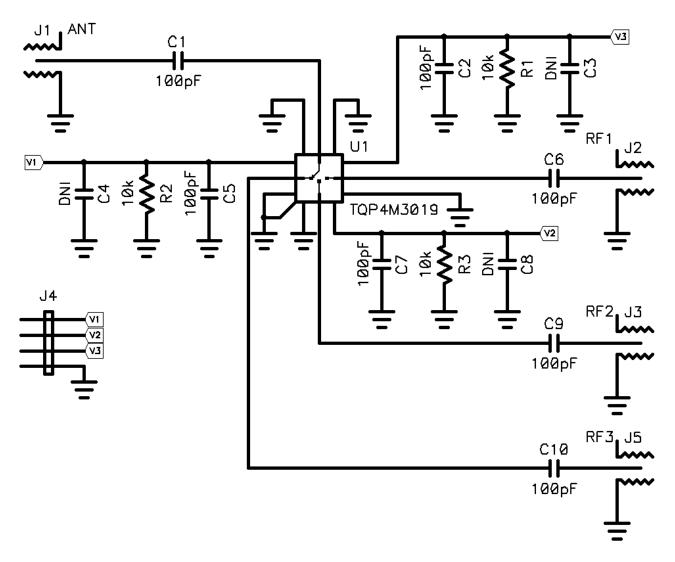


High Band Cross Modulation





Demonstration Board Circuit

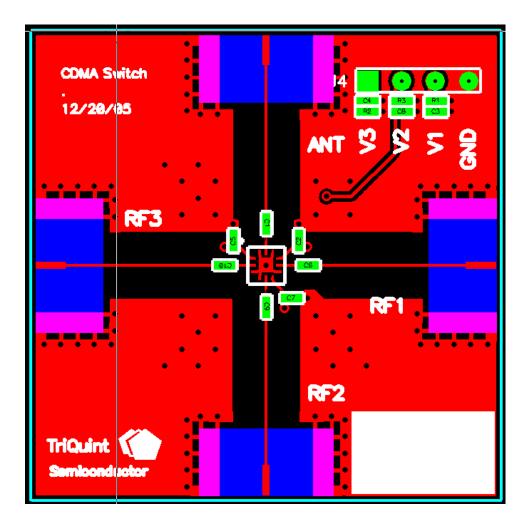


Notes:

- 1. Package Paddle Should Not be Grounded For Best Performance. See Application Note for Details.
- 2. GND leads 3, 4, 7, 10 and 12 may be left as N/C with no performance degradation.
- 3. Control line bypass caps, C2, C5, and C7 should be at least 5 pF and may be larger if needed, depending on the switching time required in the application. See Application Note for details.
- 4. R1, R2 and R3 are optional pull-down resistors to ensure the "Off" legs of the switch are held to a low enough voltage in circuits using "open collector" style control lines. These lines must be held close to zero volts when the corresponding switch leg is "off" for proper operation of the switch. A nominal control voltage of +2.6V is applied to V1, V2 or V3 corresponding to the "On" leg of the switch, with the other two pins held at nominally 0V. Only one switch leg may be "On" at any time.



Application Board Component Locations:

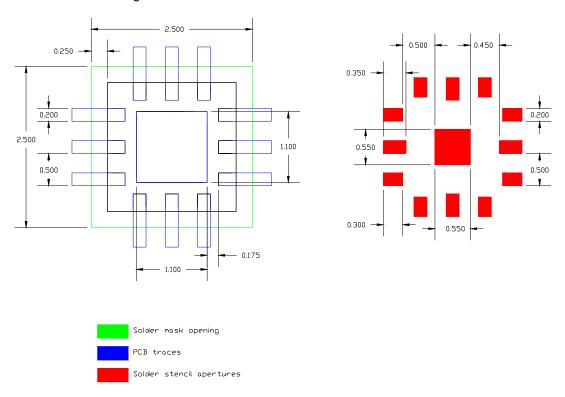


See Application Note for additional details including board level losses for de-embedding.



Recommended PCB Footprint for 12ld STSLP 2 x 2 x 0.57mm Package

Package Paddle Should Not be Grounded For Best Performance



PROCEDURE

PCB Layout:

Leads are to extend away from the pads – these should be the same shape and size to ensure equal solder coverage.

Solder mask:

The solder mask opening should be offset from the package edges by 250um.

Solder stencil:

Center pad opening is about 30% of PCB pad size.



Part Marking Information:



• 019 XXX

WHITE INK OR LASER MARK.

Line 1: 019 - Product code.

Line 2: XXX- Last 3 Char of TriQuint assembly lot number.

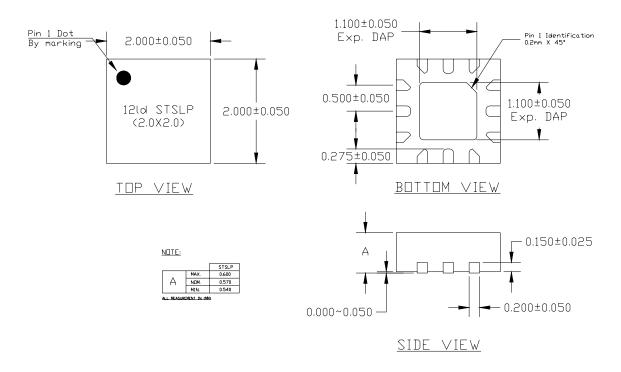
Tape and Reel Information:

TBD



Packaging and Ordering Information

12 lead STSLP 2 x 2 x 0.57 mm



Additional Information ¹T

This part is compliant with RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

1 For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: Hwww.triquint.comH Tel: (503) 615-9000
Email: info_wireless@tqs.com Fax: (503) 615-8902

For technical questions and additional information on specific applications:

Email: info_wireless@tqs.com

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