Low Threshold Dual N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Dual N-channel device
- Low threshold – 2.0V max.
- High input impedance
- Low input capacitance – 200pF
- Fast switching speeds
- Low caps ON resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Medical ultrasound pulsers
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

The Supertex TN2425TG is a dual low threshold enhancement mode (normally off) transistor utilizing a vertical DMOS structure and Supertex's well proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Option	BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ *(max)*	$V_{GS(th)}$ *(max)*	$I_{D(ON)}$ *(min)*
	8-Lead SOIC (Narrow Body)				
TN2425TG	TN2425TG	250V	3.5Ω	2.0V	1.8A

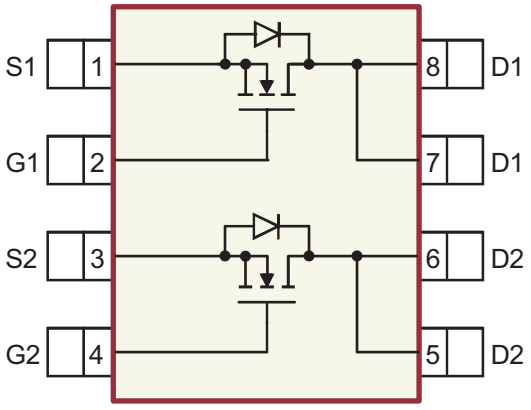
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV_{DSS}
Drain to gate voltage	BV_{DGS}
Gate to source voltage	±20V
Thermal resistance, Junction to drain lead	50°C/W
Operating and storage temperature	-55°C to +150°C
Soldering temperature[1]	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

***Note 1**. Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



8-Lead SOIC
(top view)

Electrical Characteristics *(each device, T_J=25°C unless otherwise specified)*

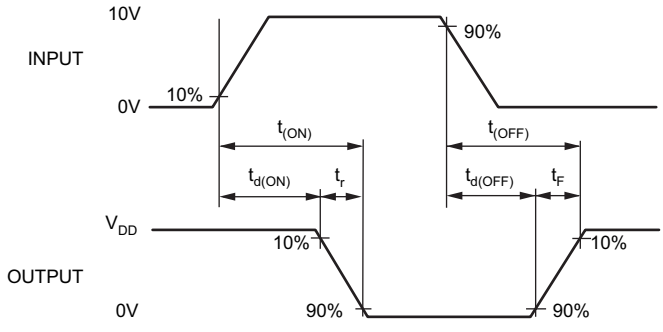
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	250	-	-	V	V_{GS} = 0V, I_D = 250µA
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	V_{GS} = V_{DS}, I_D = 1mA
ΔV_{Match}	Change in $V_{GS(th)}$ with temperature	-	-	25	mV	V_{GS} = V_{DS}, I_D = 1mA, T_A = 10°C - 80°C
$\Delta V_{GS(th)}$	$V_{GS(th)}$ change with temperature	-	-	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-state drain current	1.5	-	-	A	V_{GS} = 6.0V, V_{DS} = 25V
		1.8	-	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	5.0	Ω	V_{GS} = 4.5V, I_D = 300mA
		-	-	3.5		V_{GS} = 10V, I_D = 400mA
R_{MATCH}	Channel to channel $R_{DS(ON)}$ matching	-	-	20	%	V_{GS} = 10V, I_D = 400mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.4	%/°C	V_{GS} = 10V, I_D = 400mA
G_{FS}	Forward transconductance	300	-	-	mmho	V_{DS} = 15V, I_D = 400mA
$G_{FSMATCH}$	Channel to channel G_{FS} matching	-	-	5	%	V_{DS} = 15V, I_D = 50mA
		-	-	5	%	V_{GS} = 15V, I_D = 1.50A
C_{ISS}	Input capacitance	-	115	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common source output capacitance	-	30	100		
C_{RSS}	Reverse transfer capacitance	-	10	40		
$C_{ISSMATCH}$	Channel to channel C_{ISS} matching	-	-	25	%	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz
$C_{OSSMATCH}$	Channel to channel C_{OSS} matching	-	-	25		
$C_{RSSMATCH}$	Channel to channel C_{RSS} matching	-	-	25		
$t_{d(ON)}$	Turn-ON delay time	-	5	15	ns	V_{DD} = 25V, I_D = 500mA, R_{GEN} = 25Ω
t_r	Rise time	-	10	25		
$t_{d(OFF)}$	Turn-OFF delay time	-	25	35		
t_f	Fall time	-	5	15		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 500mA

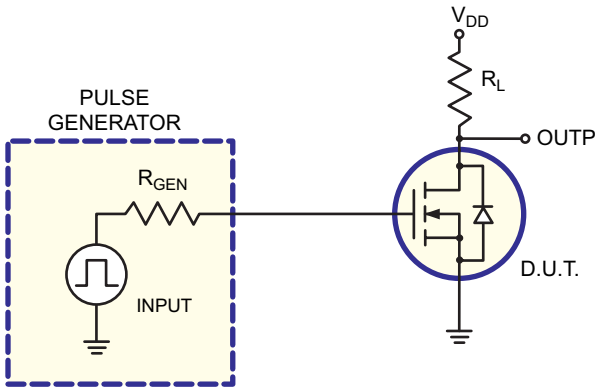
Notes:

1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

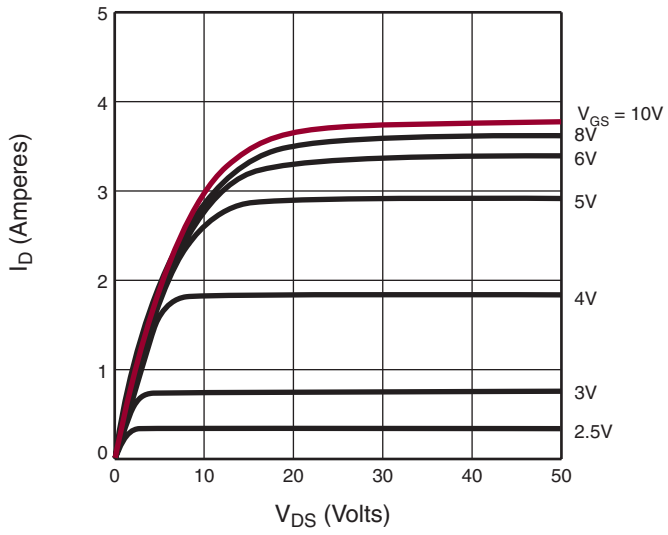
Switching Waveforms and Test Circuit



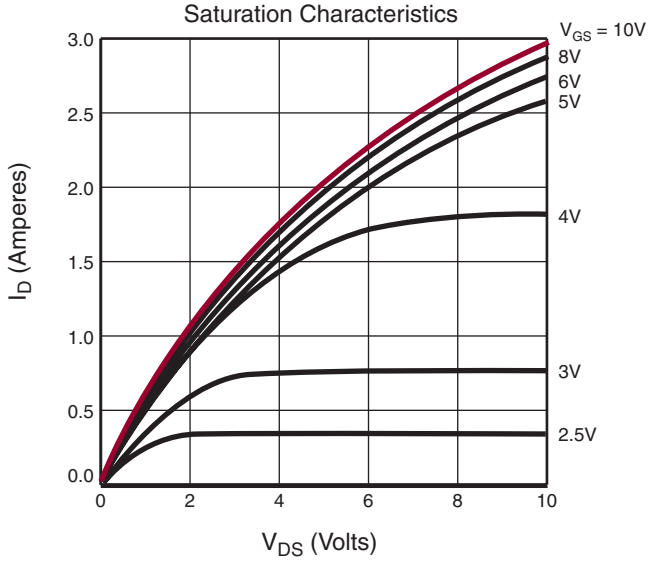


Typical Performance Curves

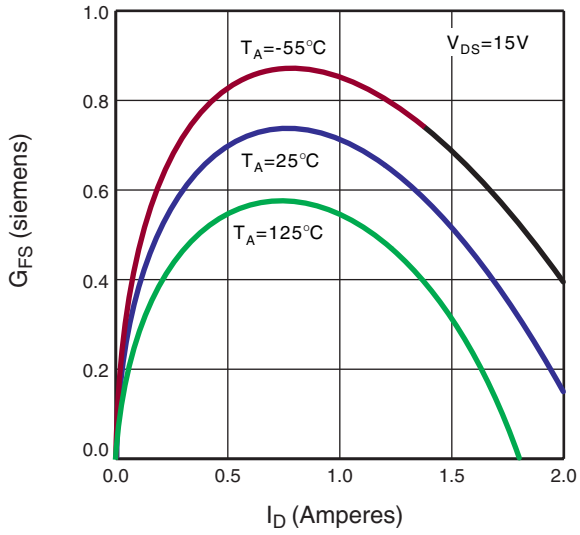
Output Characteristics



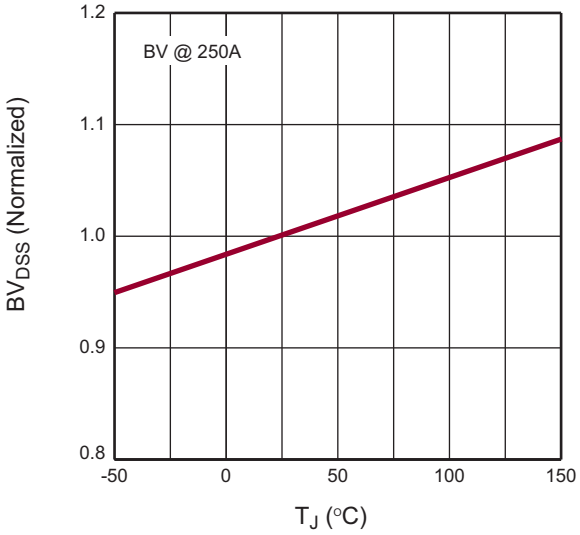
Saturation Characteristics



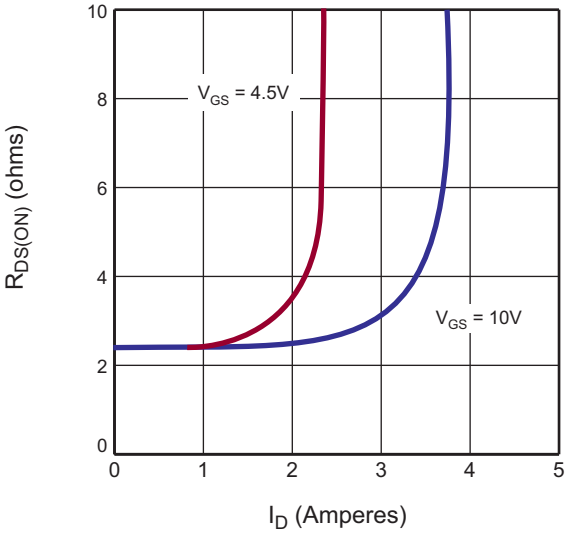
Transconductance vs. Drain Current



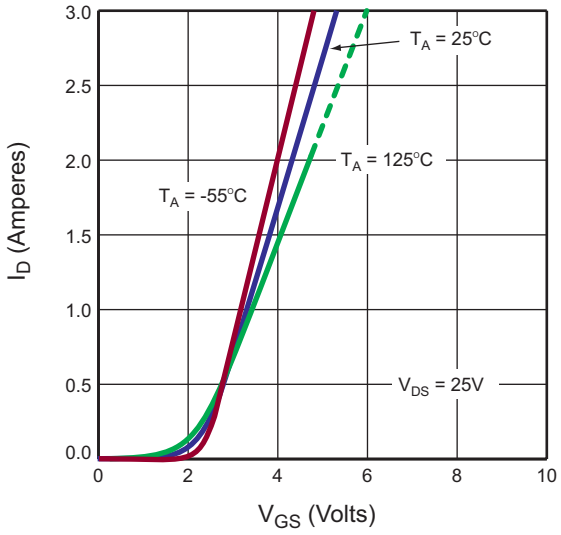
BV_{DSS} Variation with Temperature



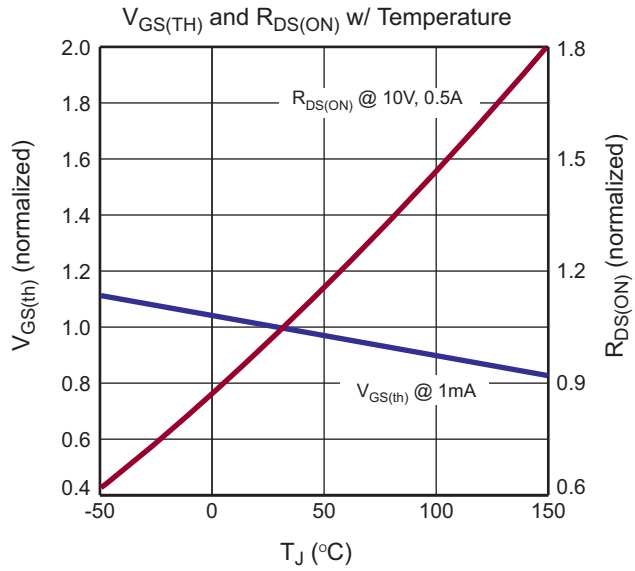
On Resistance vs. Drain Current

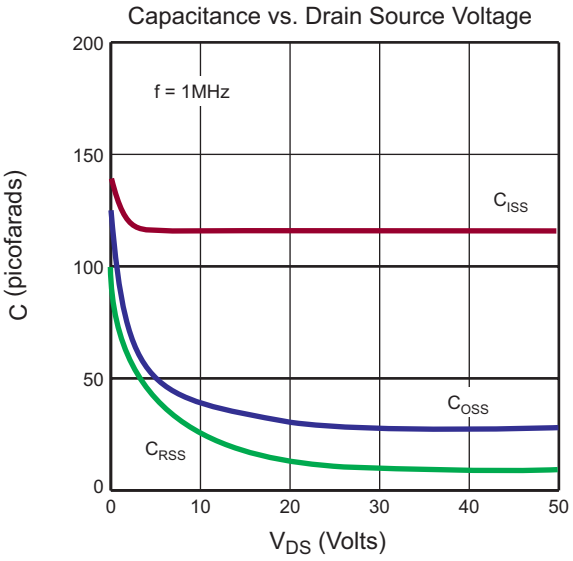


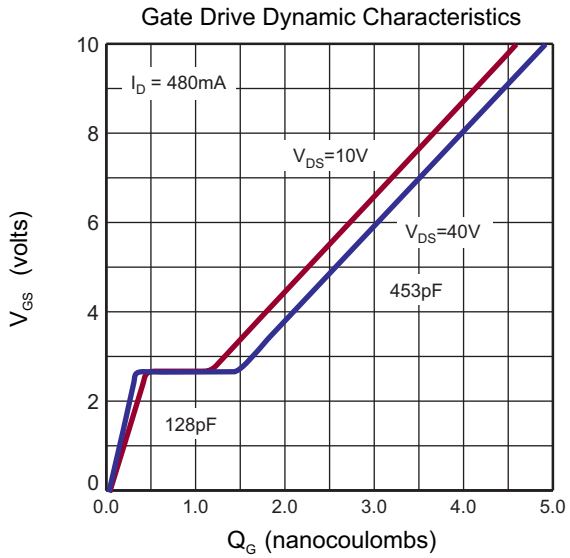
Transfer Characteristics



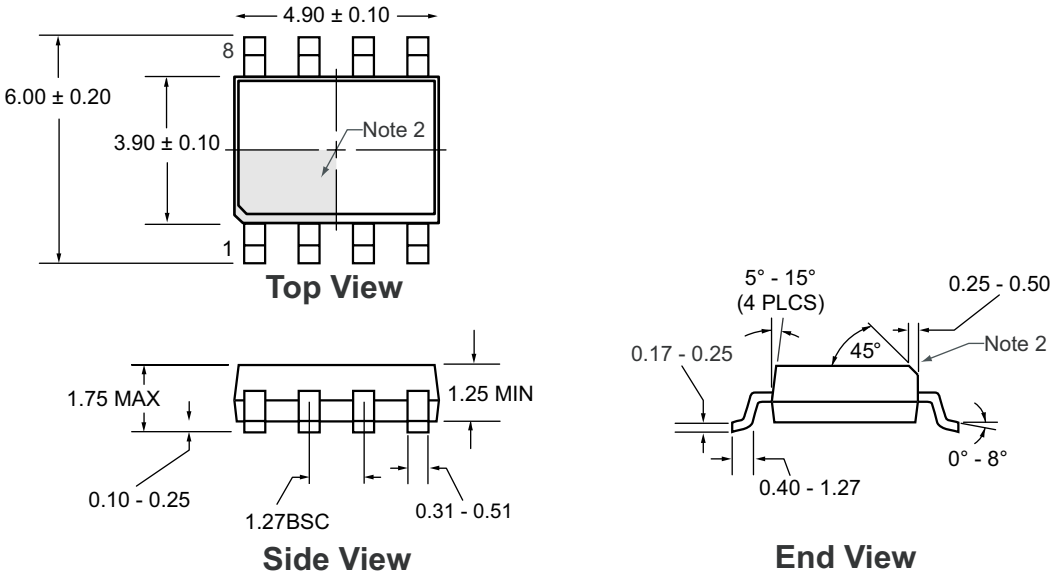
Typical Performance Curves *(cont.)*







8-Lead SOIC (Narrow Body) Package Outline (TG)



Notes:

1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com

Doc.# DSFP-TN2425TG
NR111506