

DATA SHEET

TDA8776A

**10-bit, 1000 Msps Digital-to-Analog
Converter (DAC)**

Product specification
Supersedes data of 1995 May 11
File under Integrated Circuits, IC02

1996 Jun 04

10-bit, 1000 Msps Digital-to-Analog Converter (DAC)

TDA8776A

FEATURES

- 10-bit resolution
- Conversion rate up to 1000 MHz
- 10K/100K ECL input levels
- Internal reference voltage generator
- No deglitching circuit required
- Internal input register
- Power dissipation only 925 mW (typical)
- Internal 50 Ω output load (connected to the analog ground)
- Very few external components required.

APPLICATIONS

High-speed digital-to-analog conversion for:

- High resolution video and graphics
- Direct digital synthesis (DDS)
- Telecommunication
- High-speed modems.

GENERAL DESCRIPTION

The TDA8776A is a 10-bit Digital-to-Analog Converter (DAC) for high resolution video and other high frequency applications. It converts the digital input signal into an analog output voltage at a maximum conversion rate of 1000 Msps. No external reference voltage is required and all digital inputs are 10K/100K-ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		-5.46	-5.20	-4.94	V
V_{EED}	digital supply voltage		-5.46	-5.20	-4.94	V
V_{EEI}	input stages digital supply voltage	note 1	-5.46	-5.20	-4.94	V
I_{EEA}	analog supply current	note 1	–	108	145	mA
I_{EED}	digital supply current	note 1	–	60	85	mA
I_{EEI}	input stages digital supply current	note 1	–	10	15	mA
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)	notes 1 and 2; $Z_L = 50 \Omega$	1.7	2.0	2.5	V
INL	DC integral non-linearity	note 3	–	± 0.3	± 0.5	LSB
DNL	DC differential non-linearity	note 3	–	± 0.2	± 0.45	LSB
$f_{clk(max)}$	maximum clock frequency		1000	–	–	MHz
t_{S1}	settling time (differential)	10% to 90% full scale; Fig.9	–	0.5	–	ns
P_{tot}	total power dissipation		–	925	–	mW

Notes

1. D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and \overline{CLK} is LOW.
2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω .
3. A warm-up time is necessary to reach optimal performances.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8776AK	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2

10-bit, 1000 Msp/s Digital-to-Analog Converter (DAC)

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BLOCK DIAGRAM

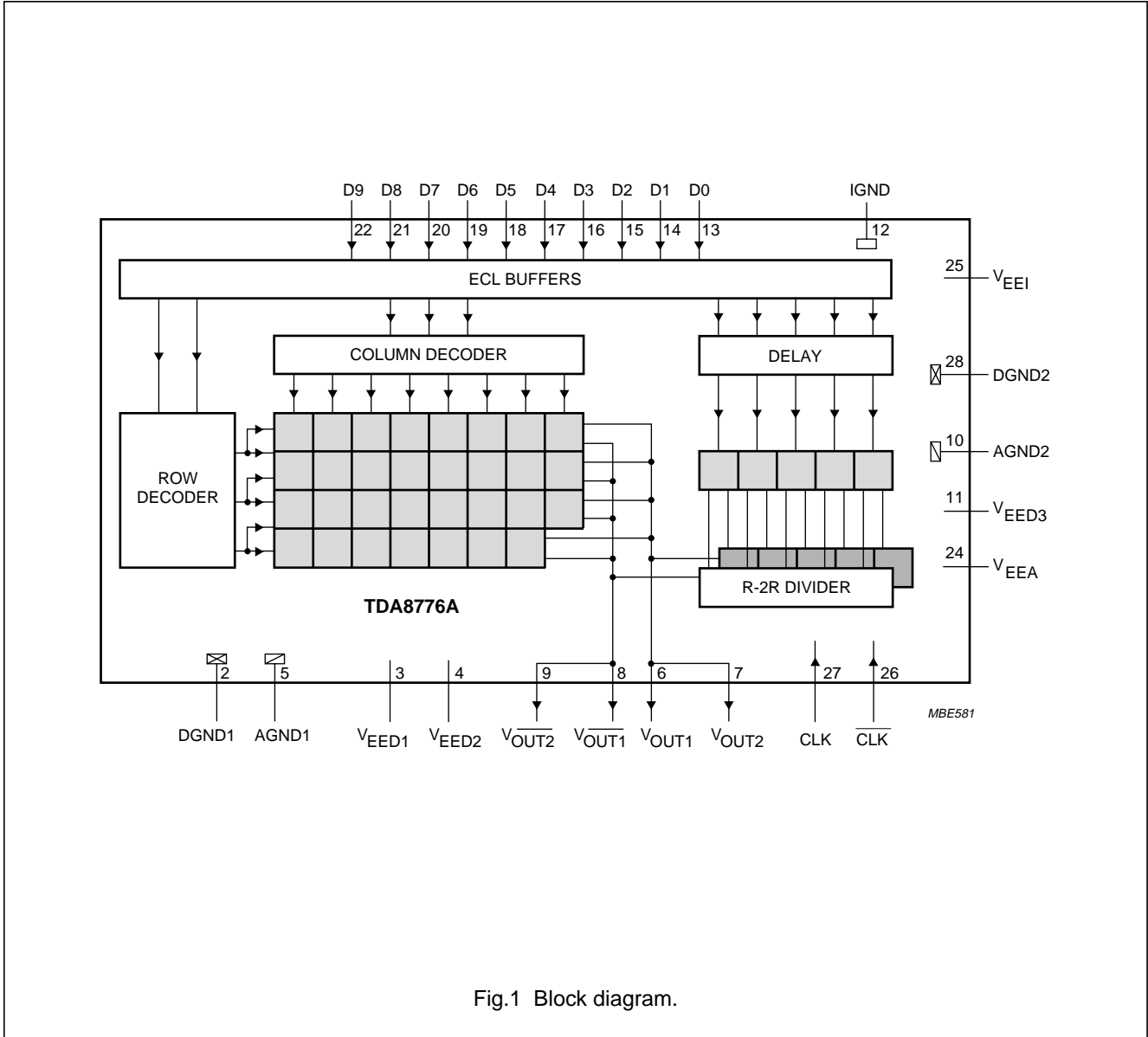


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DGND1	2	digital ground 1
V _{EED1}	3	digital supply voltage 1 (-5.2 V)
V _{EED2}	4	digital supply voltage 2 (-5.2 V)
AGND1	5	analog ground 1
V _{OUT1}	6	analog voltage output 1
V _{OUT2}	7	analog voltage output 2
V _{OUT1}	8	complementary analog voltage output 1
V _{OUT2}	9	complementary analog voltage output 2
AGND2	10	analog ground 2
V _{EED3}	11	digital supply voltage 3 (-5.2 V)
IGND	12	input ground for ECL input buffers
D0	13	data input; bit 0 (LSB)
D1	14	data input; bit 1

SYMBOL	PIN	DESCRIPTION
D2	15	data input; bit 2
D3	16	data input; bit 3
D4	17	data input; bit 4
D5	18	data input; bit 5
D6	19	data input; bit 6
D7	20	data input; bit 7
D8	21	data input; bit 8
D9	22	data input; bit 9 (MSB)
n.c.	23	not connected
V _{EEA}	24	analog supply voltage (-5.2 V)
V _{E EI}	25	input supply voltage for ECL input buffers (-5.2 V)
CLK	26	complementary clock input
CLK	27	clock input
DGND2	28	digital ground 2

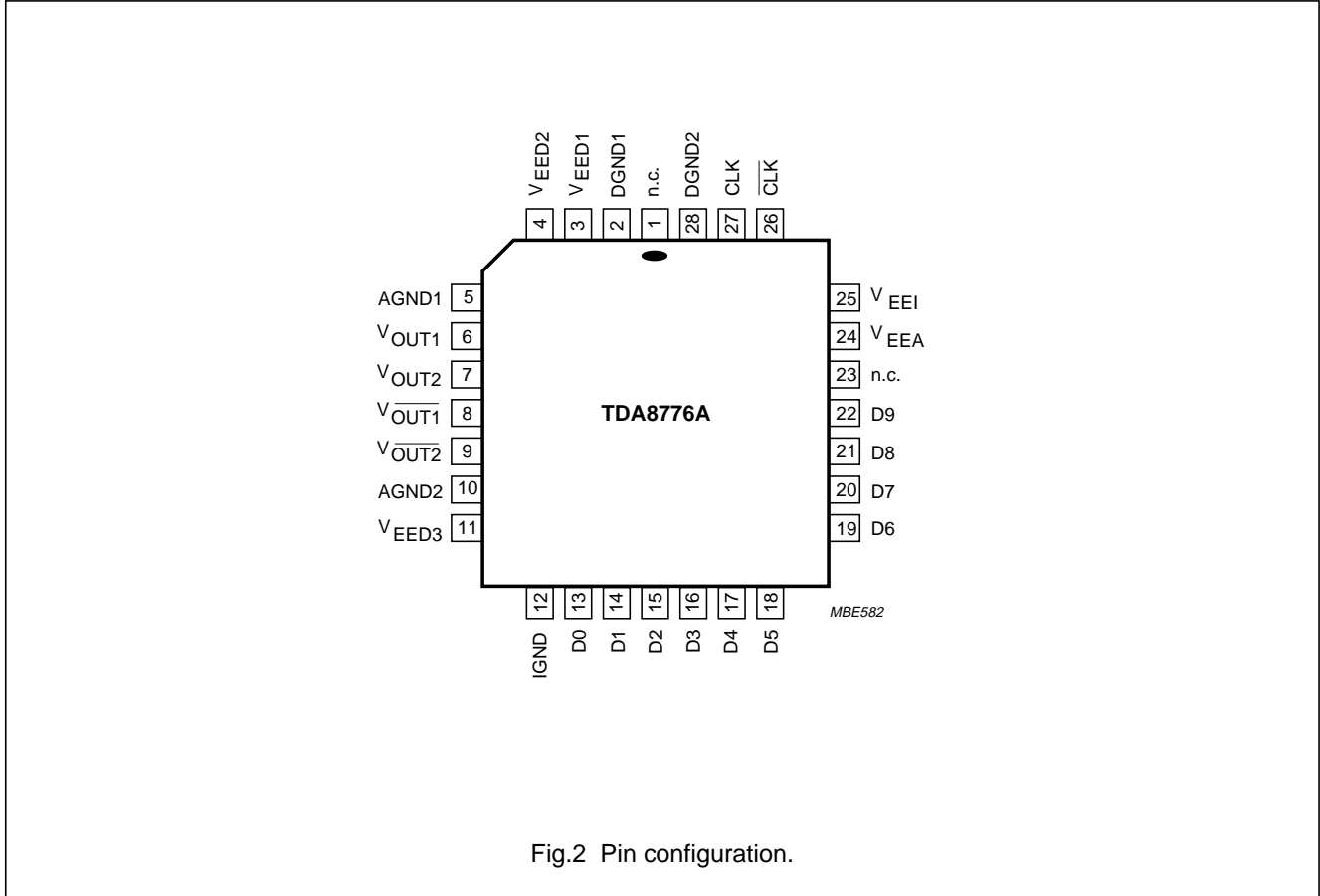


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		-7.0	± 0.3	V
V_{EED}	digital supply voltage		-7.0	± 0.3	V
V_{EEI}	input stages digital supply voltage		-7.0	± 0.3	V
$V_{EEA} - V_{EED}$	supply voltage differential		-0.5	+0.5	V
AGND – DGND	ground voltage differential		-0.1	+0.1	V
V_I	input voltage		V_{EEI}	± 0.3	V
$I_{OUT}/\overline{I_{OUT}}$	total output current	$Z_L = 50 \Omega$	-5	+50	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		-	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	55 (typ.)	K/W

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CHARACTERISTICS

$V_{EEA} = V_{24}$ to V_5 and $V_{10} = -5.46$ to -4.94 V; $V_{EED} = V_3, V_4$ and V_{11} to V_2 and $V_{28} = -5.46$ to -4.94 V;
 $V_{EEI} = V_{25}$ to $V_{12} = -5.46$ to -4.94 V; V_{EED} and V_{EEI} shorted together; $T_{amb} = 0$ to $+70$ °C; AGND, DGND and IGND shorted together; $V_{OUT} - V_{\overline{OUT}} = 2$ V (p-p); $Z_L = 50$ Ω ; unless otherwise specified (typical values measured at $V_{EEA} = V_{EED} = -5.2$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		-5.46	-5.20	-4.94	V
V_{EED}	digital supply voltage		-5.46	-5.20	-4.94	V
V_{EEI}	input stages digital supply voltage	note 1	-5.46	-5.20	-4.94	V
I_{EEA}	analog supply current	note 1	-	108	145	mA
I_{EED}	digital supply current	note 1	-	60	85	mA
I_{EEI}	input stages digital supply current	note 1	-	10	15	mA
AGND – DGND	ground voltage differential		-0.1	-	+0.1	V
Inputs						
DIGITAL INPUTS (D9 TO D0) AND CLOCK INPUTS (CLK AND \overline{CLK})						
V_{IL}	LOW level input voltage		-1.9	-1.8	-1.6	V
V_{IH}	HIGH level input voltage		-1.2	-0.9	-0.8	V
I_{IL}	LOW level input current	$V_I = -1.8$ V	-	-	10	μ A
I_{IH}	HIGH level input current	$V_I = -0.9$ V	-	-	20	μ A
$f_{clk(max)}$	maximum clock frequency		1000	-	-	MHz
Outputs (referenced to AGND); notes 1 and 2						
$V_{OUT} - V_{\overline{OUT}(p-p)}$	full-scale analog output voltage (peak-to-peak value)	$Z_L = 50$ Ω	1.7	2.0	2.5	V
Z_O	output impedance		-	50	-	Ω
Transfer function						
INL	DC integral non-linearity	note 3	-	± 0.3	± 0.5	LSB
DNL	DC differential non-linearity	note 3	-	± 0.2	± 0.45	LSB
Spurious free dynamic range ($f_{clk} = 1000$ MHz); $V_{EEA} = V_{EED} = 5.2$ V; $T_{amb} = 25$ °C; note 4; see Fig.3						
SFDR	spurious free dynamic range					
	$f_{OUT} = 10$ MHz		-65	-69	-	dB
	$f_{OUT} = 50$ MHz		-	-60	-	dB
	$f_{OUT} = 100$ MHz		-52	-57	-	dB
	$f_{OUT} = 200$ MHz		-	-46	-	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics ($f_{\text{clk}} = 1000 \text{ MHz}$); notes 5 and 6; see Figs 8 and 9						
$t_{\text{SU;DAT}}$	data set-up time		–	400	500	ps
$t_{\text{HD;DAT}}$	data hold time		100	150	–	ps
t_{PD}	propagation delay time		–	0.8	0.9	ns
t_{S1}	settling time	10% to 90% full scale	–	0.5	–	ns
t_{S2}	settling time	change to ± 1 LSB	–	2.0	–	ns
t_{d}	input to 50% output delay time		–	1.4	1.5	ns
Output transients; glitches ($f_{\text{clk}} = 1000 \text{ MHz}$); note 7; see Fig.10						
E_{g}	differential glitch energy from code	transition 511 to 512	–	1	2	pV.s

Notes

- D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and $\overline{\text{CLK}}$ is LOW.
- The analog output voltages (V_{OUT} and $V_{\overline{\text{OUT}}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω .
- Due to on-chip regulator behaviour a warm-up time is necessary to reach optimal performances; a typical time is 1 minute.
- Devices with higher SFDR (min.) can be delivered on special request.
- The worst case characteristics are obtained at the transition from input code 0 to 1023 and if an external load impedance greater than 50 Ω is connected between V_{OUT} or $V_{\overline{\text{OUT}}}$ and AGND in parallel with the external 50 Ω load. The specified values have been measured directly on a 50 Ω load between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the falling edge of the clock.
- The data set-up ($t_{\text{SU;DAT}}$) is the minimum period preceding the falling edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the falling edge of the clock and still be recognized. The data hold time ($t_{\text{HD;DAT}}$) is the minimum period following the falling edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the falling edge of the clock and still be recognized.
- The definition of glitch energy and the measurement set-up are shown in Fig.10. The glitch energy is measured at the input transition between code 511 to 512.

Table 1 Input coding and DAC output voltages (typical values; referenced to AGND regardless of the offset voltage)

CODE	BINARY INPUT DATA										DAC OUTPUT VOLTAGES (V) $Z_{\text{L}} = 50 \Omega$	
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	V_{OUT}	$V_{\overline{\text{OUT}}}$
0	0	0	0	0	0	0	0	0	0	0	0	–1.0
1	0	0	0	0	0	0	0	0	0	1	–0.0010	–0.9990
·	·	·	·	·	·	·	·	·	·	·	·	·
512	1	0	0	0	0	0	0	0	0	0	–0.5	–0.5
·	·	·	·	·	·	·	·	·	·	·	·	·
1022	1	1	1	1	1	1	1	1	1	0	–0.9990	–0.0010
1023	1	1	1	1	1	1	1	1	1	1	–1.0	0

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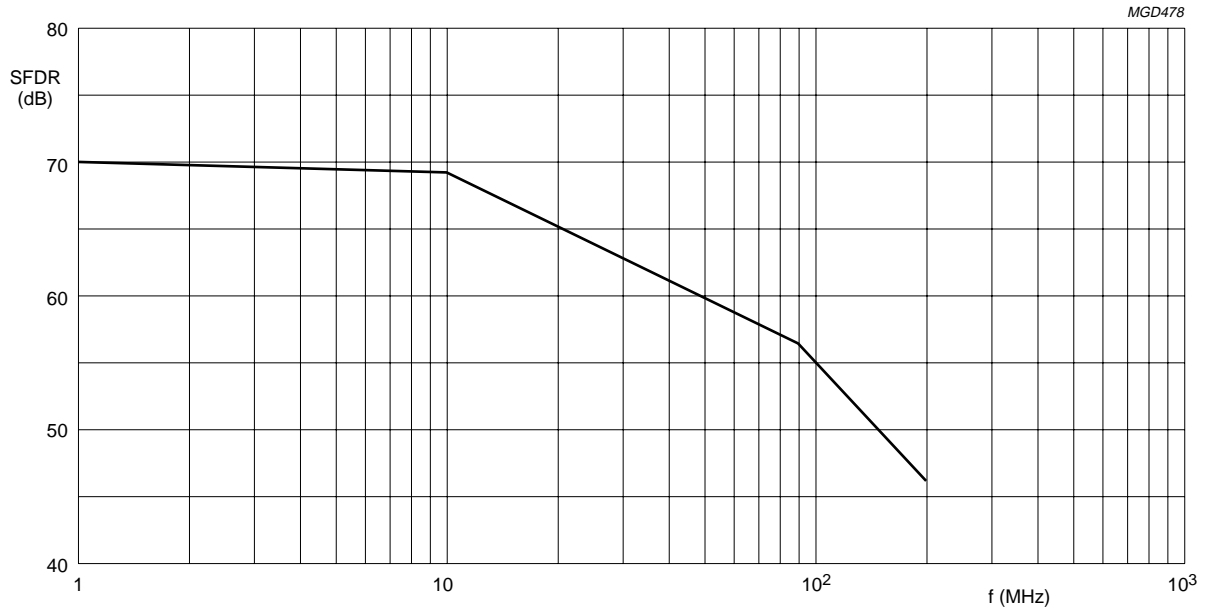


Fig.3 Typical spurious free dynamic range (SFDR) as a function of output frequency.

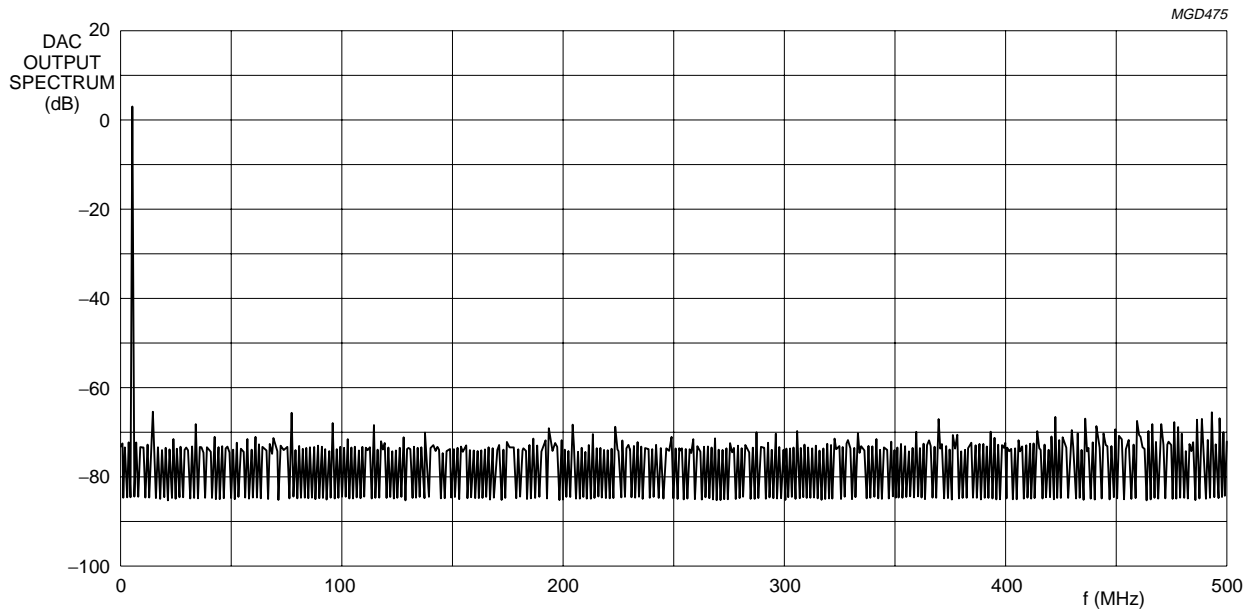
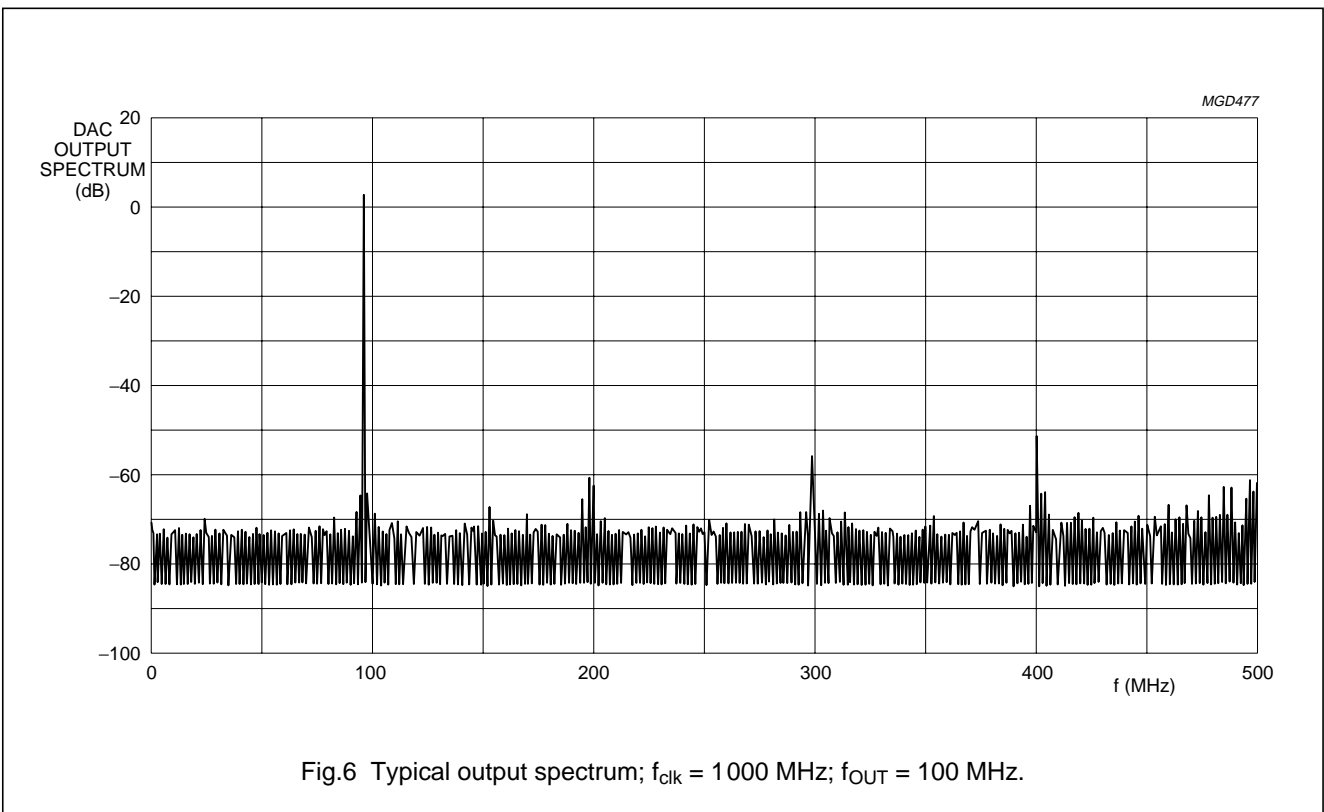
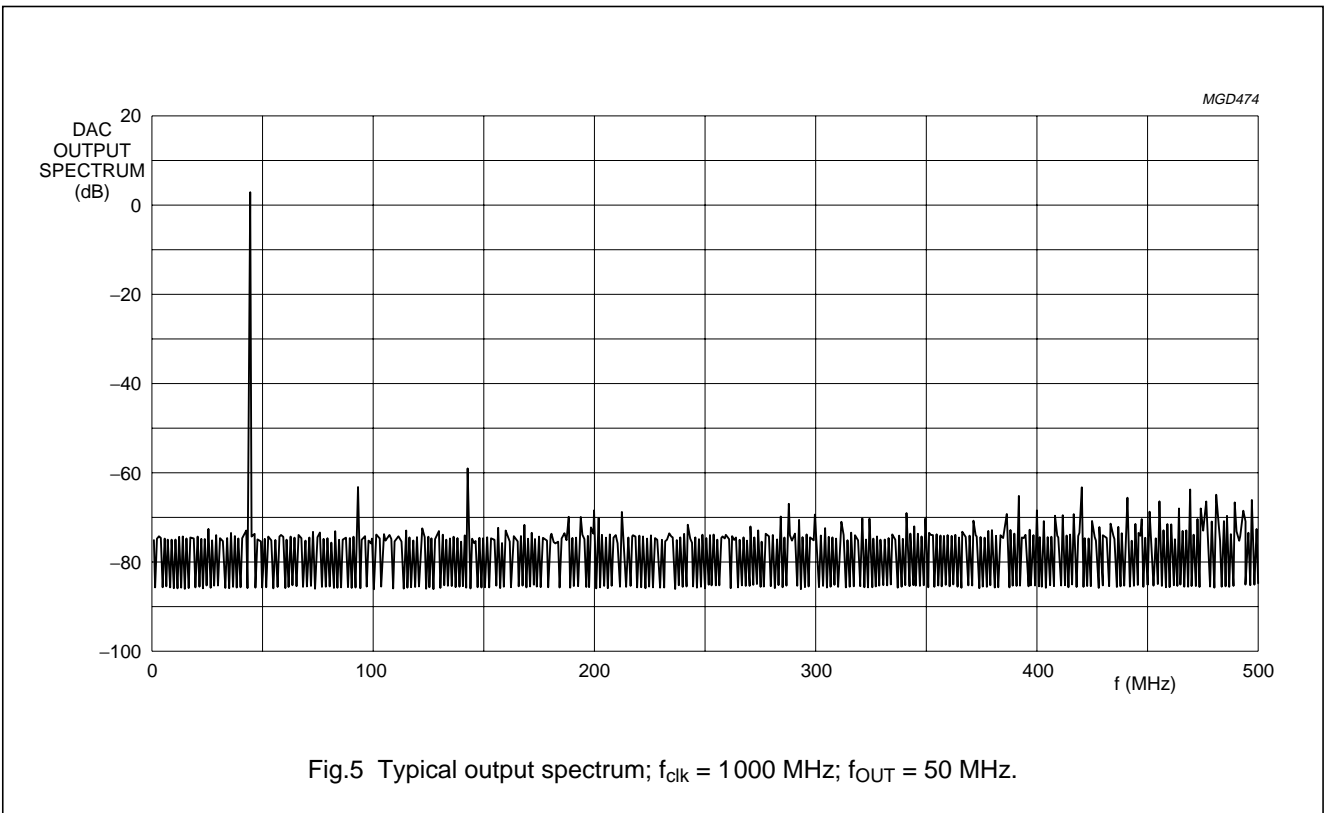


Fig.4 Typical output spectrum; $f_{clk} = 1000$ MHz; $f_{OUT} = 10$ MHz.

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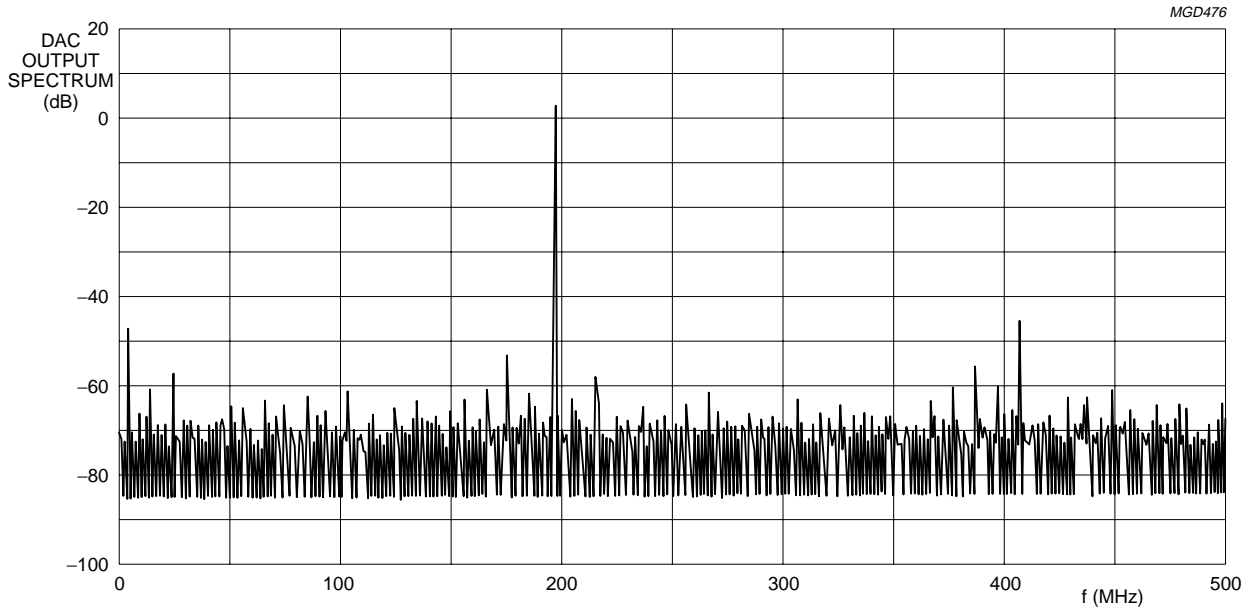
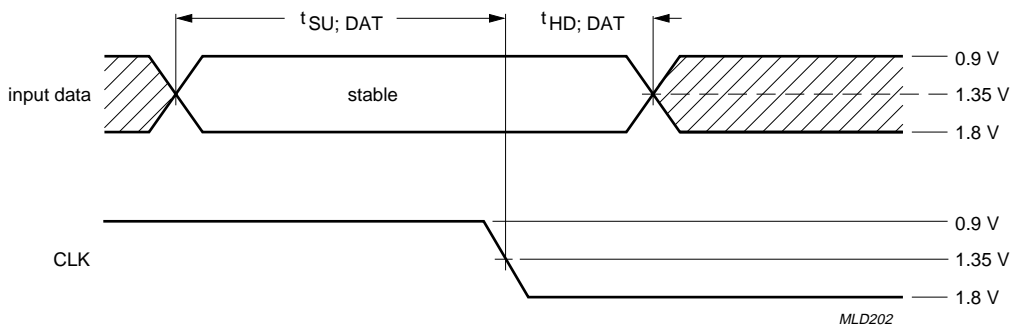


Fig.7 Typical output spectrum; $f_{clk} = 1000$ MHz; $f_{OUT} = 200$ MHz.



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within t_{bf} ns after the falling edge of the clock ($t_{SU; DAT}$ is negative; t_{bf} ns). Data must be held at least t_{bf} ns after the falling edge ($t_{HD; DAT} = t_{bf}$ ns).

Fig.8 Data set-up and hold times.

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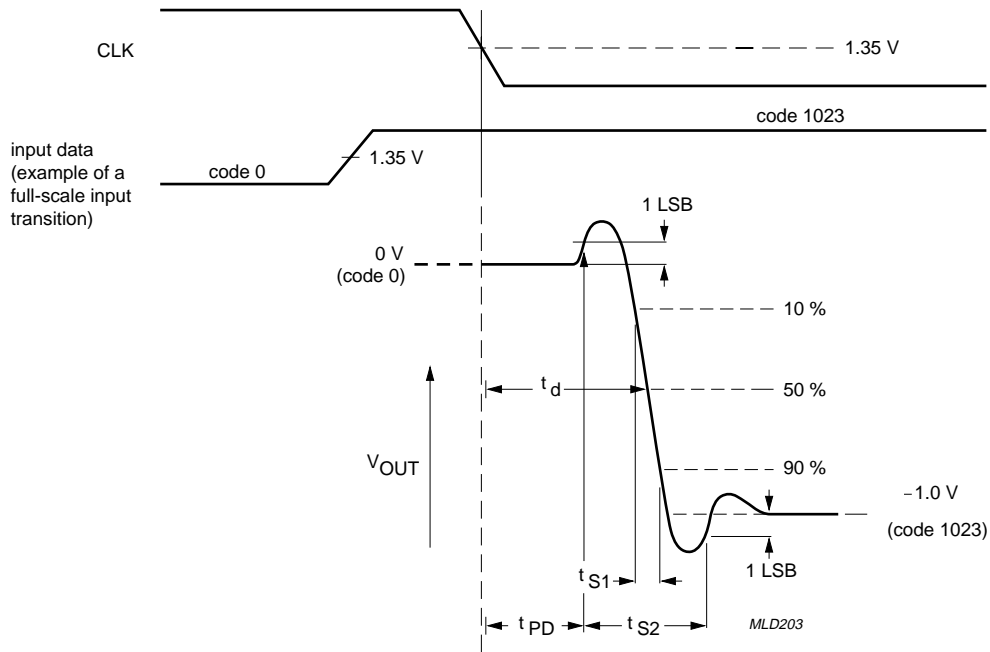
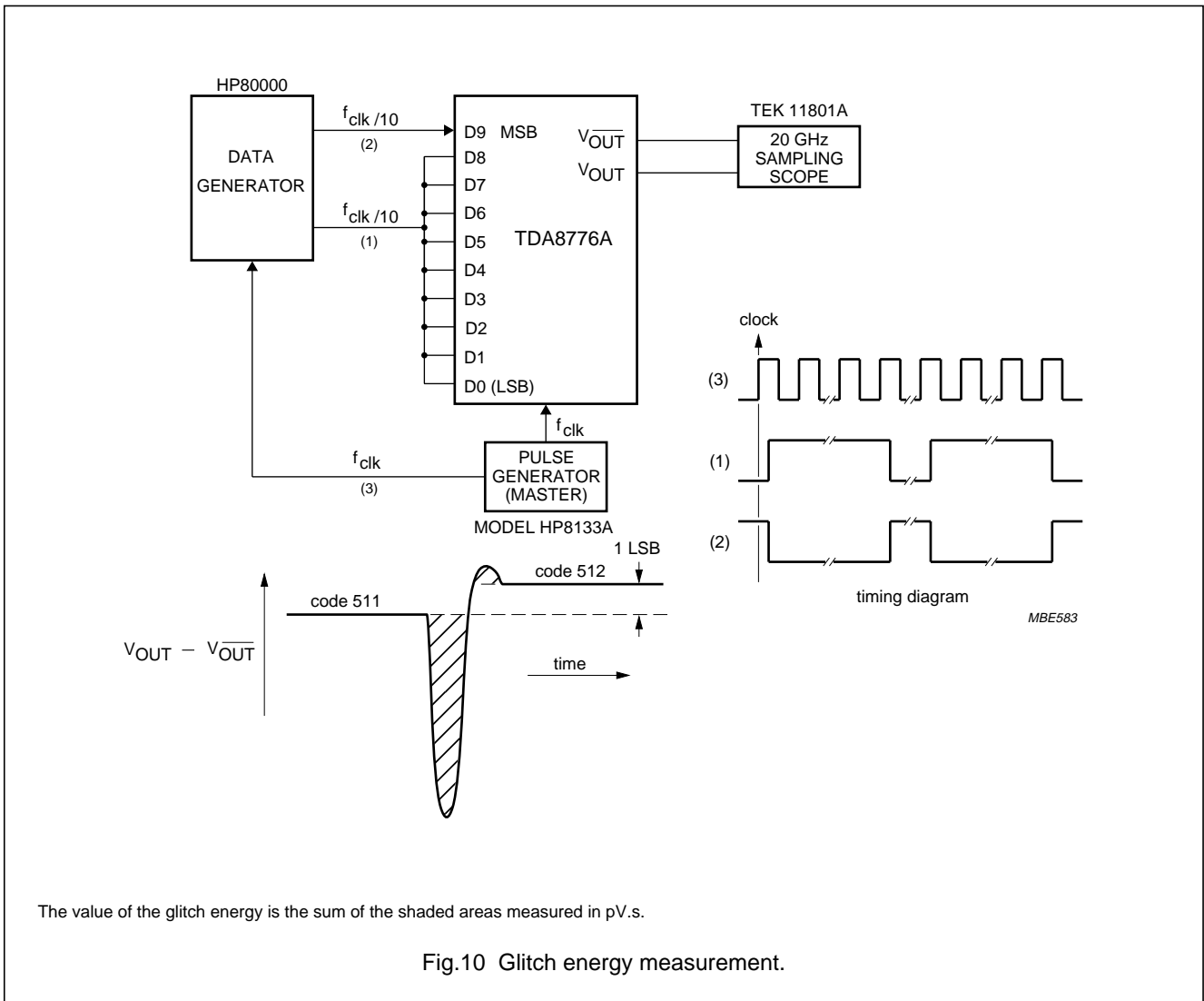


Fig.9 Switching characteristics.

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INTERNAL PIN CONFIGURATIONS

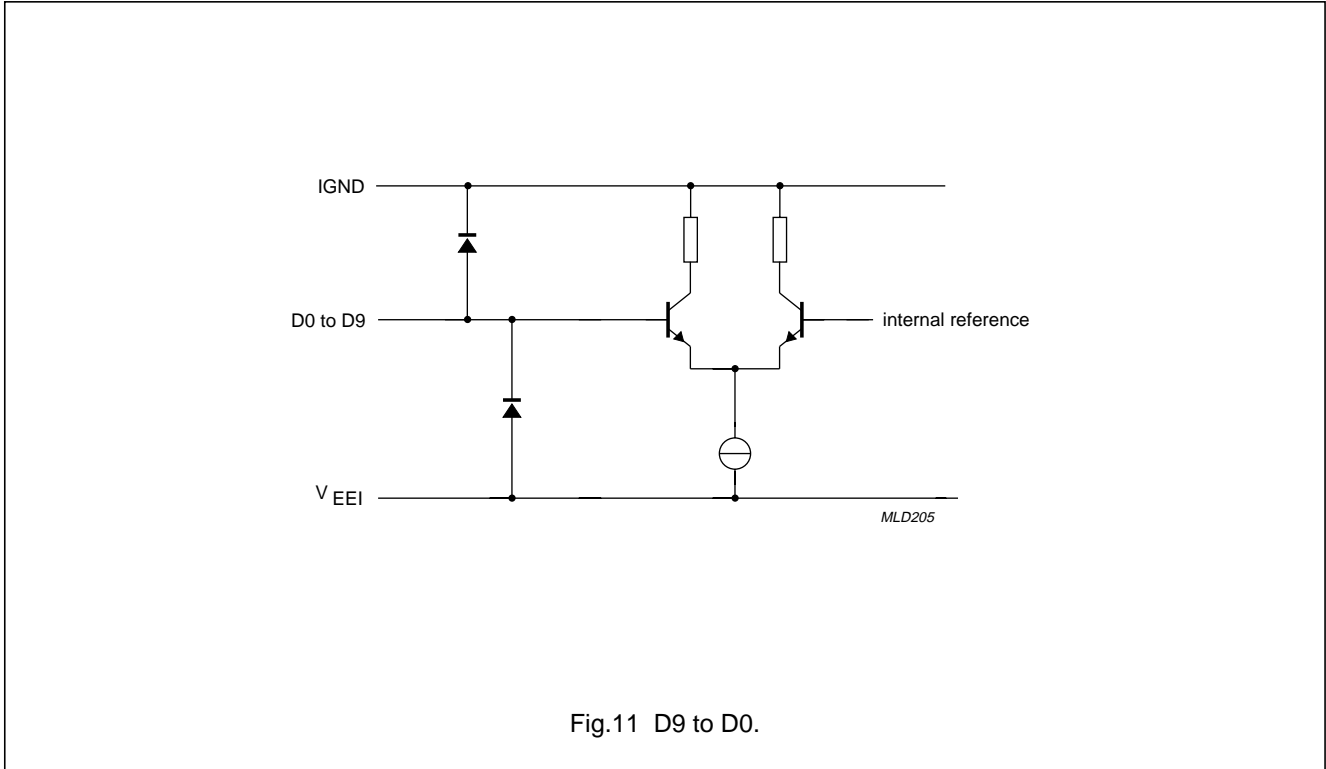


Fig.11 D9 to D0.

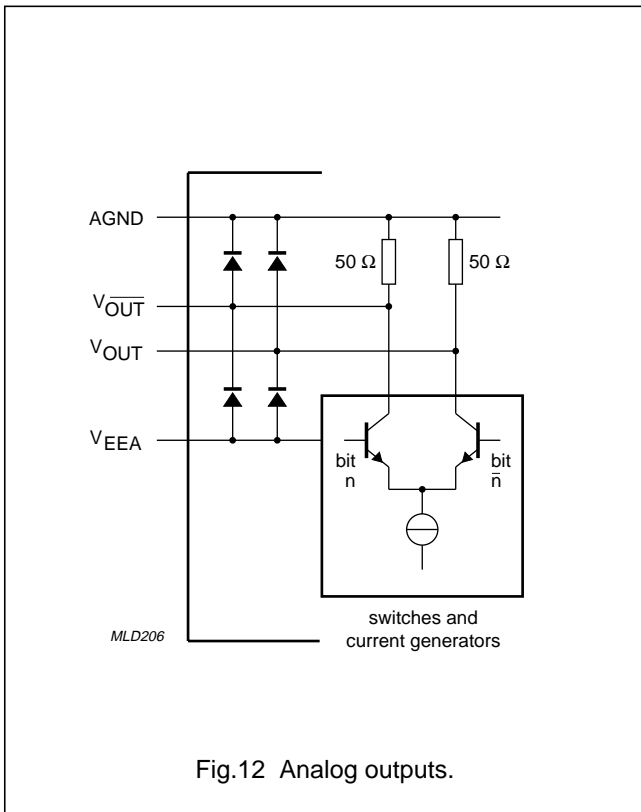


Fig.12 Analog outputs.

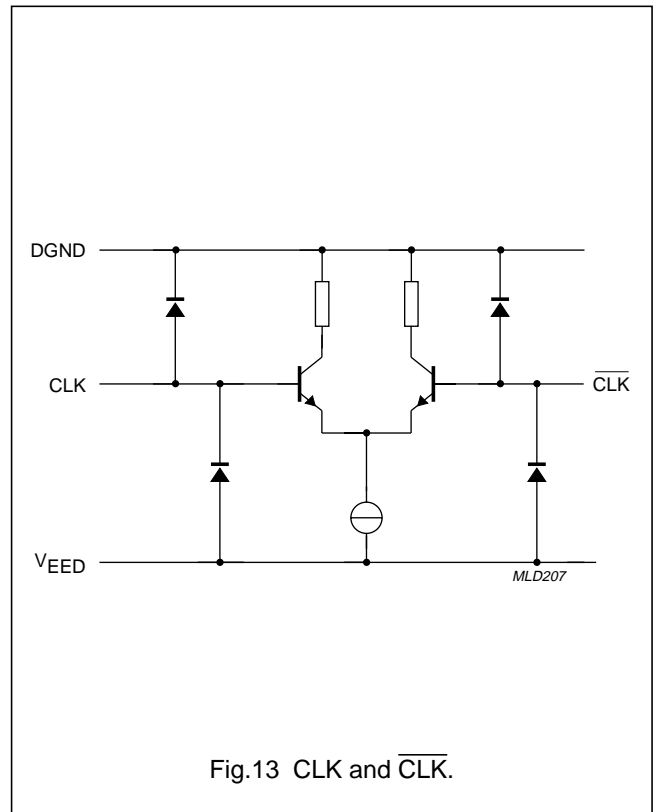


Fig.13 CLK and CLK.

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APPLICATION INFORMATION

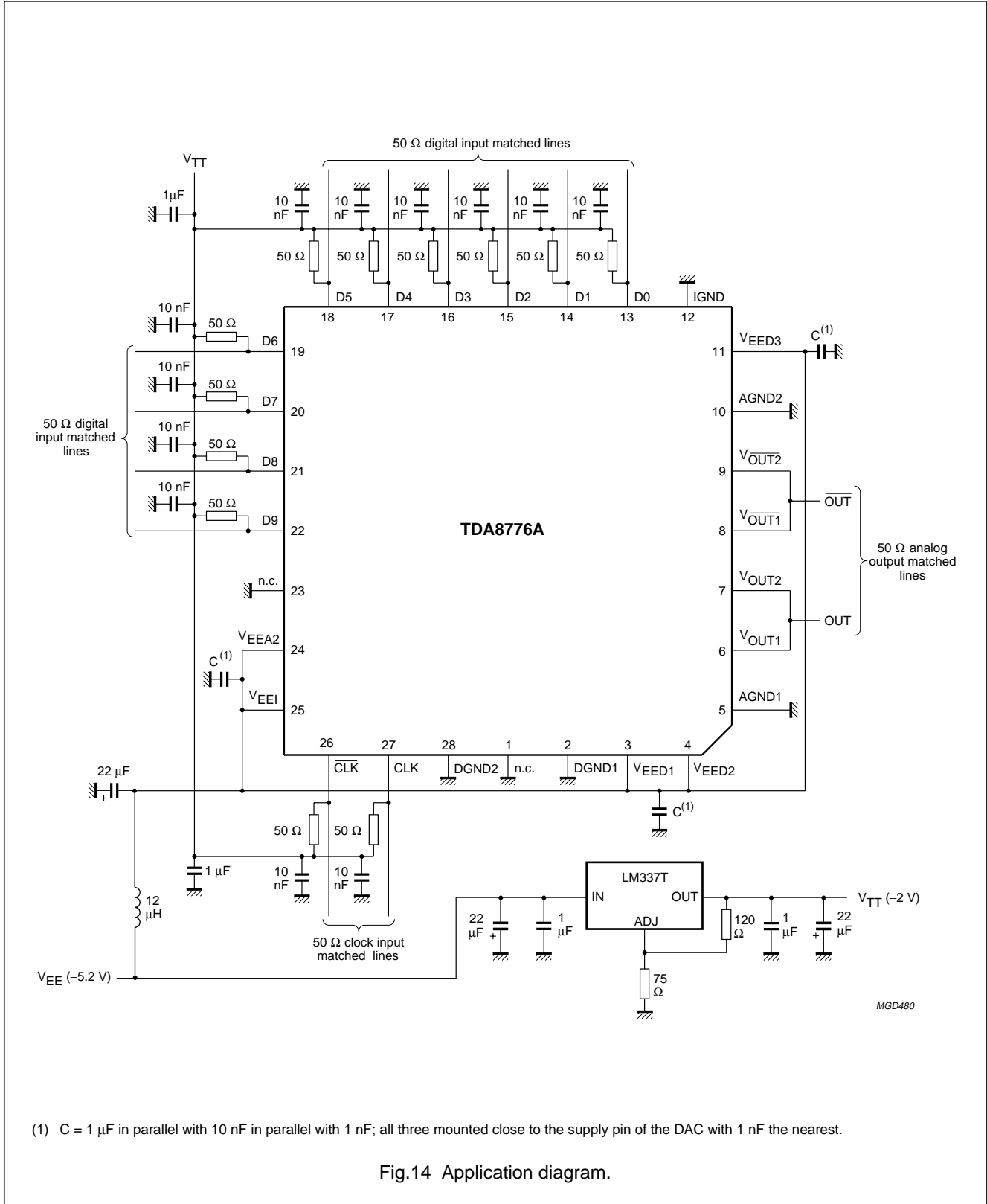


Fig.14 Application diagram.

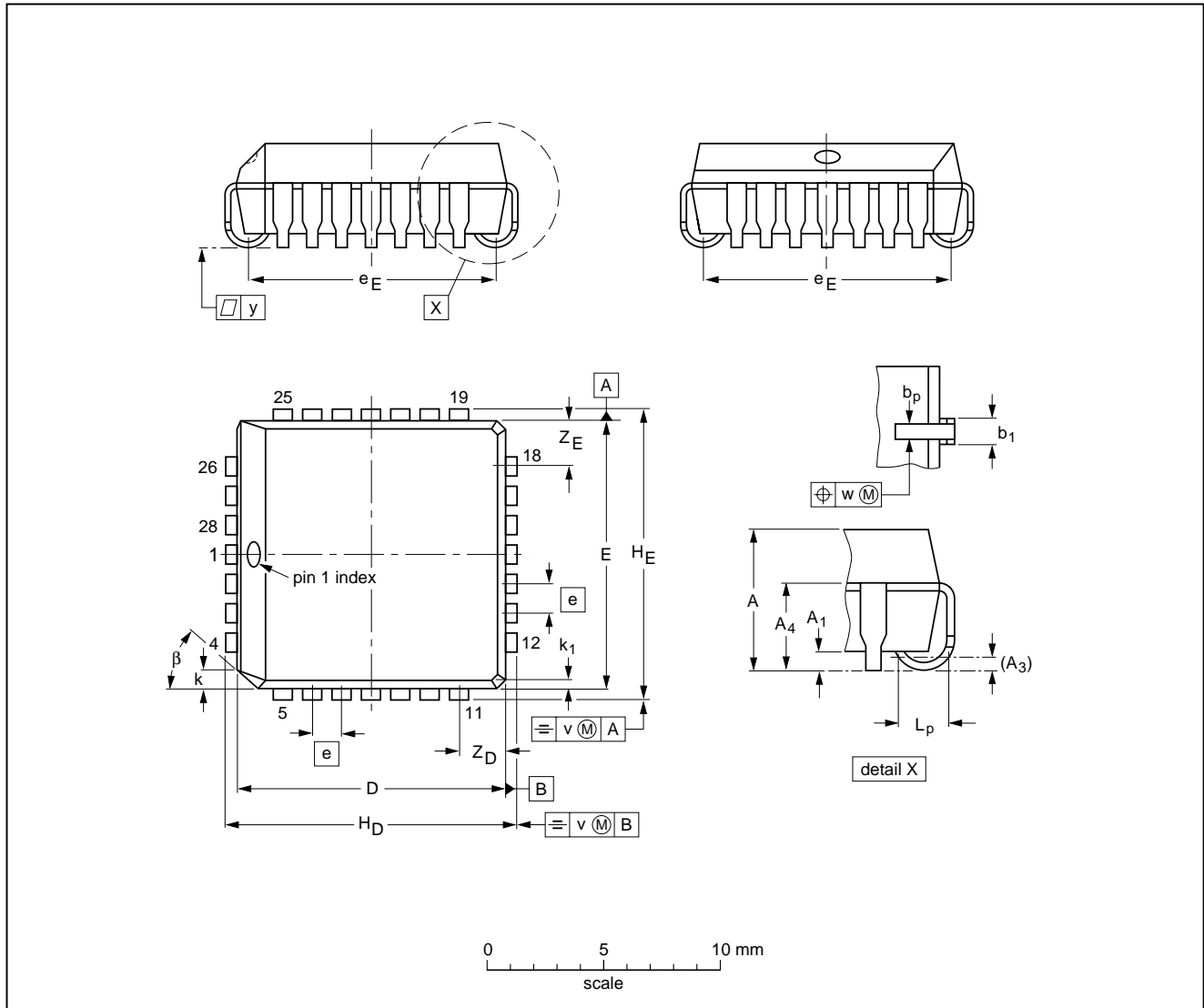
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PACKAGE OUTLINE

PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT261-2					92-11-17 95-02-25

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SOLDERING PLCC

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook2"* (order code 9398 65290011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger plastic packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at 270 to 320 °C

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 805 4455, Fax. +61 2 805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 52 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 648 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 83749, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil. P.O. Box 7383 (01064-970),
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 2A Akademika Koroleva str., Office 165,
252148 KIEV, Tel. +380 44 476 0297/1642, Fax. +380 44 476 6991

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 708 296 8556

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 825 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com/ps/>

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Printed in The Netherlands

537021/1200/02/pp20

Date of release: 1996 Jun 04

Document order number: 9397 750 00888

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