STV82x8

Digital Audio Decoder/Processor for BTSC Television/Video Recorders

PRELIMINARY DATA

Key Features

- **Fully Automatic Multi-Standard Demodulation**
  - M/N standards
  - FM mono
  - BTSC (US MTS) stereo and SAP standards
- **Multi-Channel Capability**
  - 3 I²S digital inputs, S/PDIF (in/out)
  - 5.1 analog outputs
  - Dolby® Pro Logic®
  - Dolby® Pro Logic II®
  - 2 I²S digital outputs (TQFP100 only)
  - 2 asynchronous I²S digital inputs (TQFP100 only)
- **Sound Processing**
  - ST royalty-free processing: ST WideSurround, ST OmniSurround, ST Dynamic Bass, ST Bass Enhancer, SRS® WOW™ , SRS® TruSurround XT™ which is Virtual Dolby® Surround and Virtual Dolby® Digital compliant
  - Independent Volume / Balance for Loudspeakers and Headphone
  - Loudspeakers: Smart Volume Control (SVC), 5-band equalizer and loudness
  - Headphone: Smart Volume Control (SVC), bass-treble, loudness, ST Dynamic Bass and SRS® TruBass™
  - 3 different bip tones
- **Analog Audio Matrix**
  - 4 stereo inputs or 5 stereo inputs (TQFP100 only)
  - 3 stereo outputs
  - Pass-thru mode
- **Audio Delay for Audio Video Synchronization**
  - Embedded stereo delay up to 120 ms for lip-sync function
  - Independent delay on headphone and loudspeaker channels
  - External additional audio delay support (TQFP100 only)

The STV82x8 family, based on audio digital signal processors (DSP), performs high quality and advanced dedicated digital audio processing.These devices provide all of the necessary resources for automatic detection and demodulation of analog audio transmissions for USA, Taiwanese, Brazilian etc. terrestrial analog TV broadcasts.

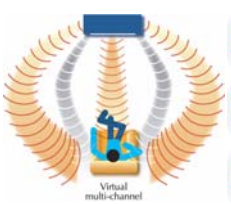
Virtual or true multi-channel capabilities and easy digital links make them ideal for digital audio low cost consumer applications. Starting from enhanced stereo up to independent control of 5 loudspeakers and a subwoofer (5.1 channels), the STV82x8 family offers standard and advanced features plus sound enhancements, spatial and virtual effects to enhance television viewer comfort and entertainment.

Typical Applications

- Analog and digital TV with virtual surround sound
- Analog and digital TV with multi-channel surround sound
- DVD and HDD recorders
- “Palm size” portable TV

TQFP80 Package

TQFP100 Package



Wide Surround
Omni Surround
Dynamic Bass
Bass enhancer
Voice

SRS WOW
SRS TruSurround XT

DOLBY SURROUND PRO LOGIC
VIRTUAL DOLBY SURROUND
VIRTUAL DOLBY DIGITAL
DOLBY PRO LOGIC II
VIRTUAL DOLBY SURROUND PRO LOGIC II

Figure 1: STV82x8 Block Diagram (TQFP80)

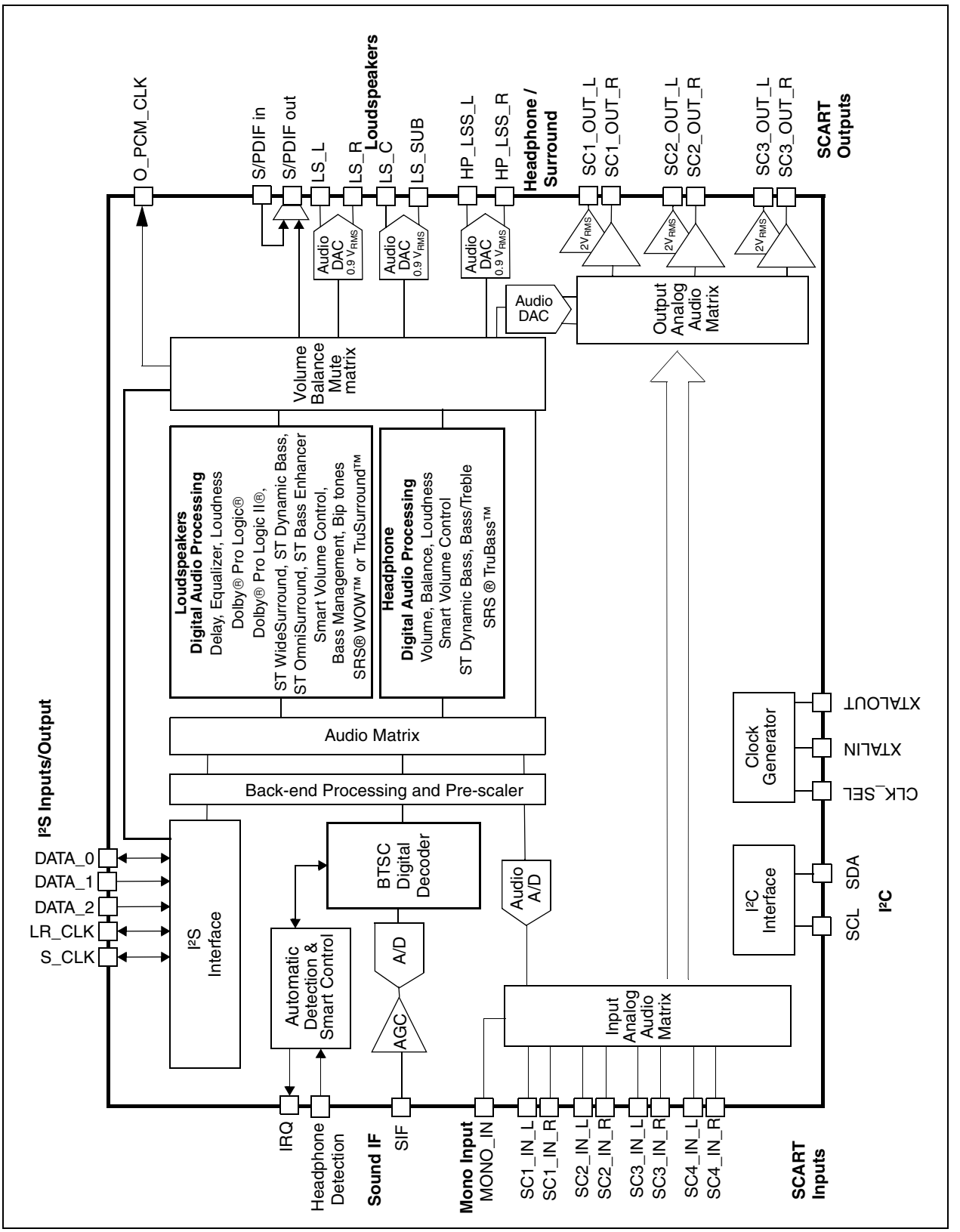
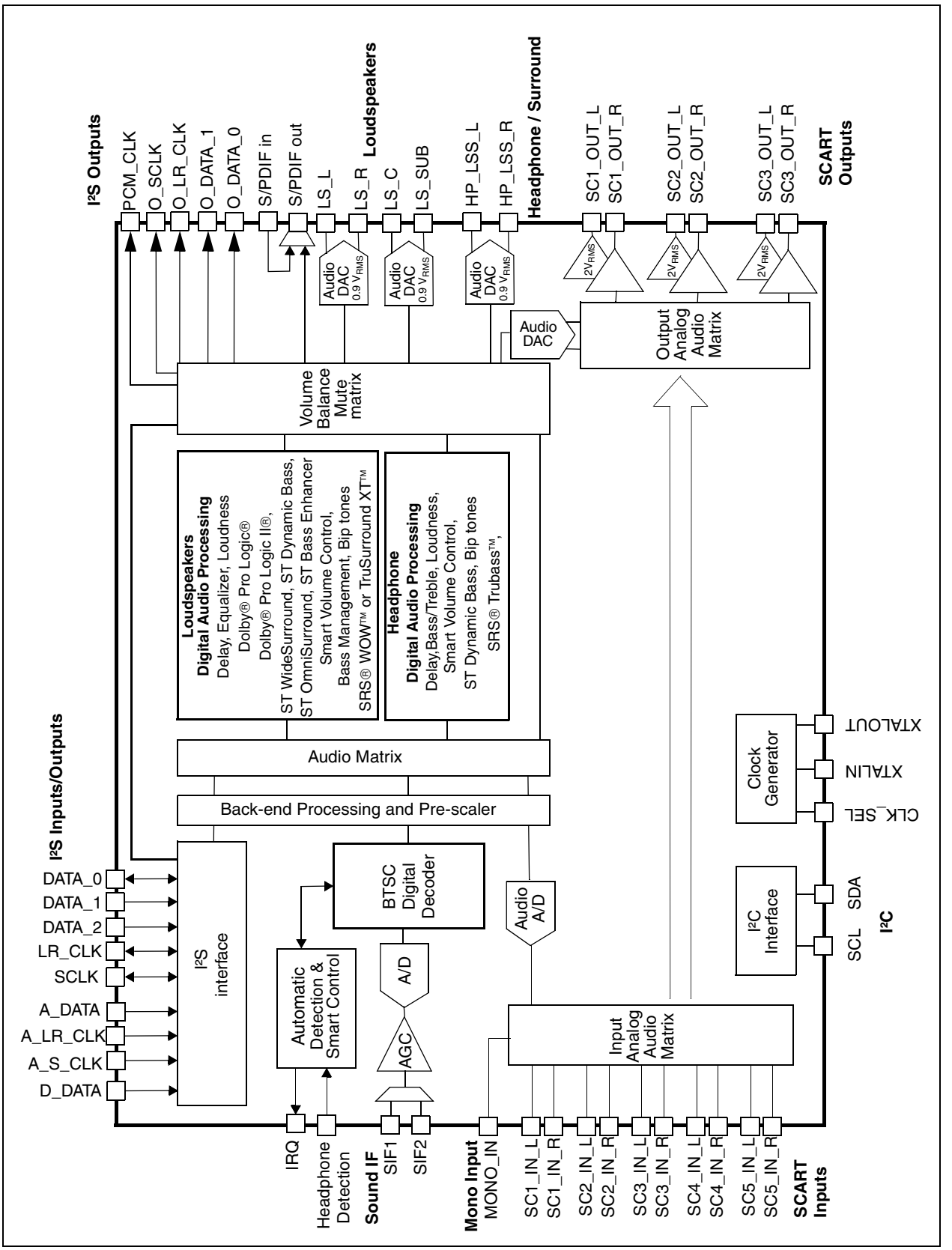


Figure 2: STV82x8 Block Diagram (TQFP100)



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1 General Description

This chip performs **BTSC stereo and SAP analog TV stereo sound identification and demodulation** (no specific I²C programming is required). It offers various audio processing functions such as equalization, loudness, beeper, volume, balance, and surround effects. It provides a cost-effective solution for analog and digital TV designs.

The STV82x8 is an audio processor which integrates **SRS® WOW™**, **SRS® TruSurround XT™**, **Dolby® Pro Logic®**, **Dolby® Pro Logic II®**, **Virtual Dolby® Surround** (VDS) and **Virtual Dolby® Digital** (VDD) capabilities.

Advanced ST royalty-free algorithms such as **ST OmniSurround**, **ST WideSurround**, **ST Dynamic Bass, ST Bass Enhancer** are also available in this audio sound processor. **ST OmniSurround** is a certified **Dolby®** algorithm for the **Virtual Dolby® Digital** (VDD) and the **Virtual Dolby® Surround** (VDS). When using VDD or VDS, either an external **Dolby® Digital** or an internal **Pro Logic®** (or **Pro Logic II®**) decoder must be used respectively.

The STV82x8 is perfectly suited to current and future digital TV platforms, based on audio/video digital chips (**STD2000 - DTV100 platform**) which include an internal digital decoder (**MPEG**, **Dolby® Digital**...). In the case where a Dolby® Digital decoder is embedded in the audio/video digital chip, Virtual Dolby® Digital certification could be obtained.

Table 1: STV82x8 Version List (TQFP 80)

	STV8218	STV8238	STV8248		STV8258		STV8268		STV8278		STV8288	
			STV8248D	STV8248DSX	STV8258D	STV8258DSX	STV8268D	STV8268DSX	STV8278D	STV8278DSX	STV8288D	STV8288DSX
Multi-Channel Capabilities												
I²S data input number	1	1	1	1	3	3	1	1	3	3	3	3
Analog loudspeakers output number	2.1	2.1	2.1	2.1	2.1	2.1	5.1	5.1	5.1	5.1	5.1	5.1
Embedded SRS® and Dolby® algorithms												
Dolby® Pro Logic ® (DPLI) or Dolby® Pro Logic II® (DPLII)			DPLI	DPLI	DPLI	DPLI	DPLI	DPLI	DPLI	DPLI	DPLII	DPLII
SRS® WOW™ (WOW) or SRS® TruSurround XT™ (XT)		WOW		XT		XT		XT		XT		XT
General Capabilities												
S/PDIF Pass-thru	X	X	X	X	X	X	X	X	X	X	X	X
BTSC & SAP / Mono FM Demodulation	X	X	X	X	X	X	X	X	X	X	X	X
ST OmniSurround[1], ST WideSurround	X	X	X	X	X	X	X	X	X	X	X	X
ST Voice, ST Dynamic Bass, ST Bass Enhancer	X	X	X	X	X	X	X	X	X	X	X	X
Dolby® Pro Logic ® (DPLI) or Dolby® Pro Logic II® (DPLII) 5.1 output							DPLI	DPLI	DPLI	DPLI	DPLII	DPLII
Dolby® Digital Bypass 5.1 output[2]									X	X	X	X
Virtual Dolby® Surround			X	X	X	X	X	X	X	X	X	X
Virtual Dolby® Digital capability[2]					X	X			X	X	X	X

1. When using **Virtual Dolby® Digital** or **Virtual Dolby® Surround** with **ST OmniSurround** or **SRS® TruSurround XT™** a **Dolby® Digital** or a **Pro Logic ®** (or **Pro Logic II®**) decoder is mandatory respectively
2. **Dolby® Digital** Bypass capability or **Virtual Dolby® Digital** are obtained with the use of an external **Dolby® Digital** decoder (for example STD2000).

Figure 3: Package Ordering Information

Order Code:
STV82x8 (Tray)
STV82x8/T (Tape & Reel)

For Example: STV8258DSX/T will be delivered in Tape & Reel conditioning

Table 2: STV82x8 Version List (TQFP 100)

	STV8218F	STV8238F	STV8248		STV8258		STV8268		STV8278		STV8288	
			STV8248FD	STV8248FDSX	STV8258FD	STV8258FDSX	STV8268FD	STV8268FDSX	STV8278FD	STV8278FDSX	STV8288FD	STV8288FDSX
Multi-Channel Capabilities												
I²S data input number	1	1	1	1	3	3	1	1	3	3	3	3
Analog loudspeakers output number	2.1	2.1	2.1	2.1	2.1	2.1	5.1	5.1	5.1	5.1	5.1	5.1
Embedded SRS® and Dolby® algorithms												
Dolby® Pro Logic ® (DPLI) or Dolby® Pro Logic II® (DPLII)			DPLI	DPLI	DPLI	DPLI	DPLI	DPLI	DPLI	DPLI	DPLII	DPLII
SRS® WOW™ (WOW) or SRS® TruSurround XT™ (XT)		WOW		XT		XT		XT		XT		XT
General Capabilities												
S/PDIF Pass-thru	X	X	X	X	X	X	X	X	X	X	X	X
Second SIF input	X	X	X	X	X	X	X	X	X	X	X	X
I²S Output (always available)	X	X	X	X	X	X	X	X	X	X	X	X
BTSC & SAP / Mono FM Demodulation	X	X	X	X	X	X	X	X	X	X	X	X
ST OmniSurround[1], ST WideSurround	X	X	X	X	X	X	X	X	X	X	X	X
ST Voice, ST Dynamic Bass, ST Bass Enhancer	X	X	X	X	X	X	X	X	X	X	X	X
Dolby® Pro Logic ® (DPLI) or Dolby® Pro Logic II® (DPLII) 5.1 output							DPLI	DPLI	DPLI	DPLI	DPLII	DPLII
Dolby® Digital Bypass 5.1 output[2]									X	X	X	X
Virtual Dolby® Surround			X	X	X	X	X	X	X	X	X	X
Virtual Dolby® Digital capability[2]					X	X			X	X	X	X

1. When using **Virtual Dolby® Digital** or **Virtual Dolby® Surround** with **ST OmniSurround** or **SRS® TruSurround XT™** a **Dolby® Digital** or a **Pro Logic ®** (or **Pro Logic II®**) decoder is mandatory respectively

2. **Dolby® Digital** Bypass capability or **Virtual Dolby® Digital** are obtained with the use of an external **Dolby® Digital** decoder (for example STD2000).

Figure 4: Package Ordering Information

Order Code:
STV82x8F (Tray)
STV82x8F/T (Tape & Reel)

For Example: STV8258FDSX/T will be delivered in Tape & Reel conditioning

1.1 STV82x8 Overview

1.1.1 Core Features

- Single audio source processing:
  - — IF source and/or analog stereo input (SCART)
  - — one digital source with a maximum of 6 synchronous channels (5.1 is obtained across three I²S)
- SIF input signal with Automatic Gain Control (AGC)
- BTSC and SAP demodulator, FM Mono
- Audio processor working at 48 kHz with specific features:
  - — For loudspeakers (L, R, L_S, R_S, SubW, C):
    Dolby® Pro Logic II ® decoder with bass management
    SRS® WOW™ or TruSurround XT™ including Virtual Dolby® Surround and Virtual Dolby® Digital
    ST WideSurround
    ST OmniSurround
    ST Dynamic Bass / ST Bass Enhancer
    5-band equalizer or bass / treble controls
    Loudness
    Smart Volume Control
    Volume/balance/soft-mute
    Three different types of bips
    Video processing delay compensation
  - — For headphones:
    SRS® TruBass™
    ST Dynamic Bass
    Smart Volume Control
    Bass / treble controls
    Loudness
    Volume/balance/soft-mute
    Three different types of bips
    Video processing delay compensation
- Shared outputs for headphone and certain loudspeakers (surround channels);
- Analog matrix with:
  - — Five external inputs:
    Four SCART inputs (2 V_{RMS} capable)
    One analog mono input (0.5 V_{RMS})
  - — One internal input from a digital matrix via a DAC
  - — Three external outputs (2 V_{RMS} capable)
  - — One internal output for the digital matrix (using an internal ADC)
- Digital matrix with:
  - — Three input modes (demodulator/SCART, SCART only and I²S)
  - — Three stereo outputs (loudspeakers, headphone and SCART)
- High-end audio DAC
- S/PDIF output for connection with an external amplifier/decoder
- Internal multiplexer for the S/PDIF output (to share the internal S/PDIF output and the S/PDIF output generated by the external decoder of the digital broadcast)

- Specific stand-by mode (loop-through)
- Control by I²C bus (two I²C addresses)
- System PLL and clock generation using either a single crystal oscillator or a differential clock input

1.1.2 Software Information

The different software combinations are listed in Table 3.

Table 3: Input/Output Software Configurations

Input (Number of Channels)	Output (Number of Channels)		
	2 (+1)	4 (+1)	5.1
1 (Mono)	ST WideSurround or SRS® WOW™		
2 (L_O & R_O)	ST WideSurround or ST OmniSurround or SRS® TruSurround XT™ or SRS® WOW™ or Dolby® Pro Logic® II	Dolby® Pro Logic® II	Dolby® Pro Logic® II
2 (L_T & R_T)	ST WideSurround or ST OmniSurround or SRS® TruSurround XT™ or SRS® WOW™ or Dolby® Pro Logic® I or II	Dolby® Pro Logic® I or II	Dolby® Pro Logic® II
4 (+1)	ST OmniSurround or SRS® TruSurround XT™	No processing	
5.1	ST OmniSurround or SRS® TruSurround XT™	Downmix	No processing

Note: In addition to the above sound processing, it is always possible to add ST Voice and also ST Dynamic Bass or ST Bass Enhancer algorithms.

Note: The SRS® TruSurround® and ST OmniSurround are approved by Dolby Labs as Virtual Dolby Surround (VDS) and Virtual Dolby Digital (VDD).

The SRS® TruSurround XT™ system is composed of:

- *SRS® TruSurround™*
- *SRS® WOW™*

The SRS® WOW™ system also includes:

- *SRS® Dialog Clarity™*
- *SRS® TruBass™*
- *SRS® 3D mono / stereo*

1.1.3 Electrical Features

Multi Power Supplies: 1.8 V, 3.3 V and 8 V.

Power Consumption:

- lower than 800mW in functional mode (full features)
- 200 mW in loop-through mode corresponding to the switch-off of all digital blocks

1.2 Typical Applications

The STV82x8 is specified to enable flexible, analog and digital TV chassis design (refer to Figure 5, Figure 6, Figure 7 and Figure 8).

The main considerations are:

- all necessary connections between devices can be provided through the TV set,
- pseudo stand-by mode used to copy to VCR or the DVD sources when the TV set is OFF,
- pin compatibility with previous STV82x7 (TQFP80 package) TV design.

The STV82x8 can be used to process dual audio sources (one analog and one digital in parallel).

Note: Headphone and loudspeakers can be used simultaneously for dual-language purpose. In this case, certain restrictions occur (see Section 4.2: Audio Processing).

For more connections, the SCART-to-SCART path can be used. The use of these full analog paths implies that the sound is not digitally processed.

Figure 5: STV8238 Typical Application (Enhanced Stereo)

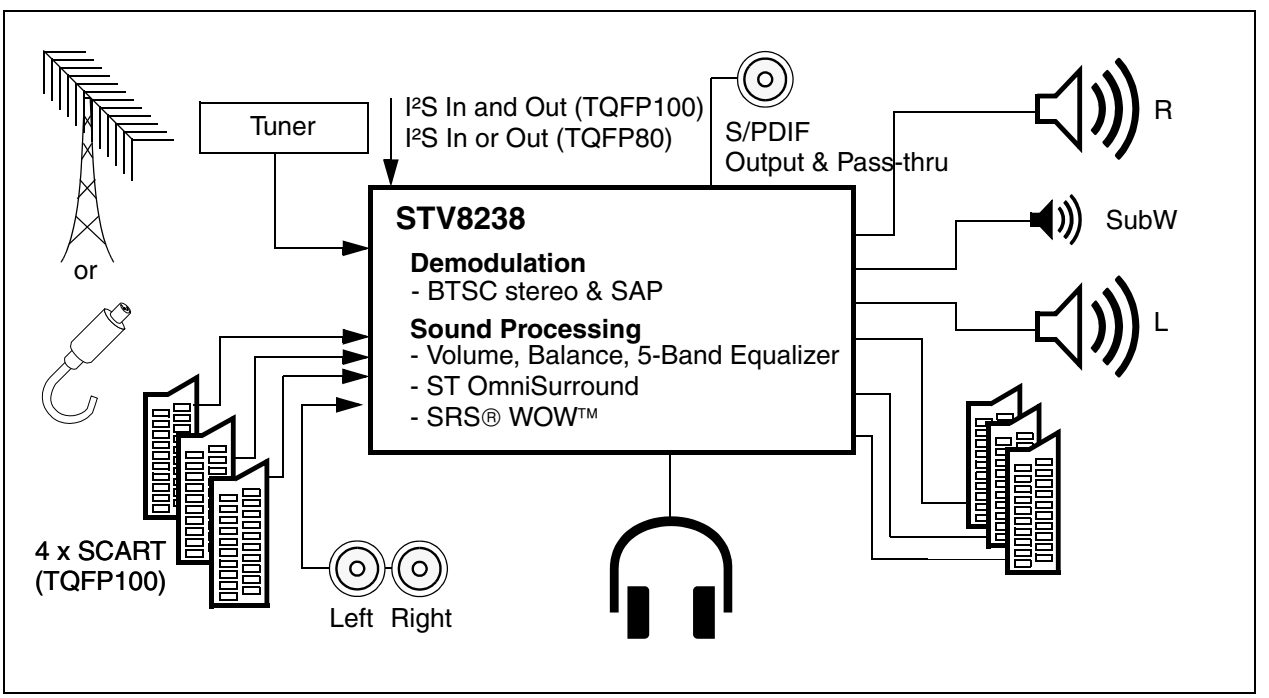
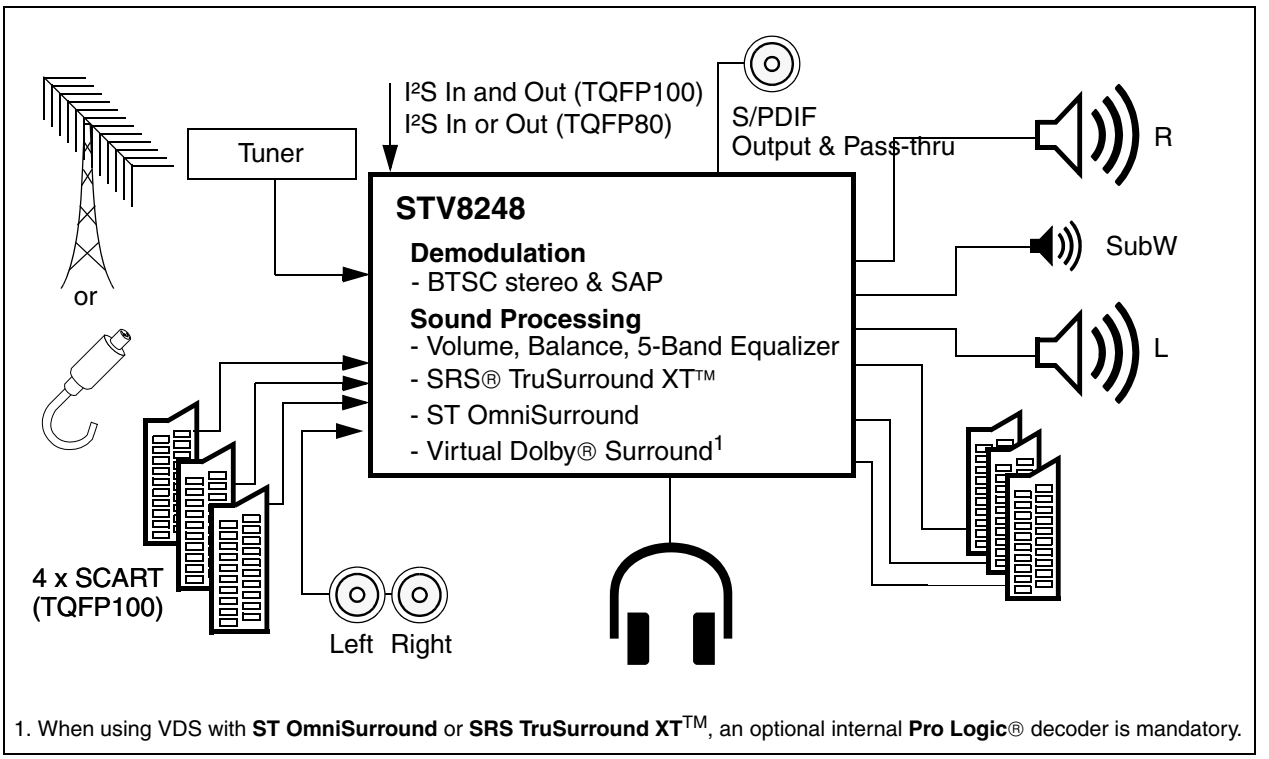
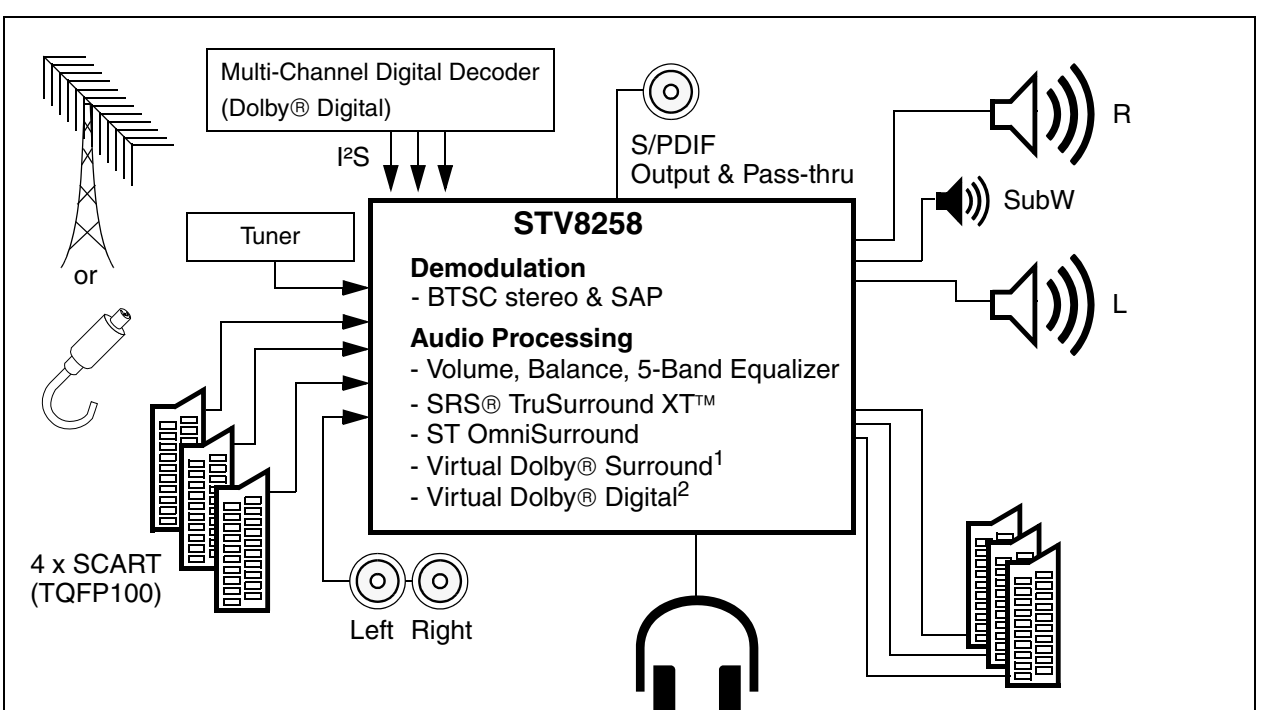


Figure 6: STV8248 Typical Application (Analog Virtual Sound)



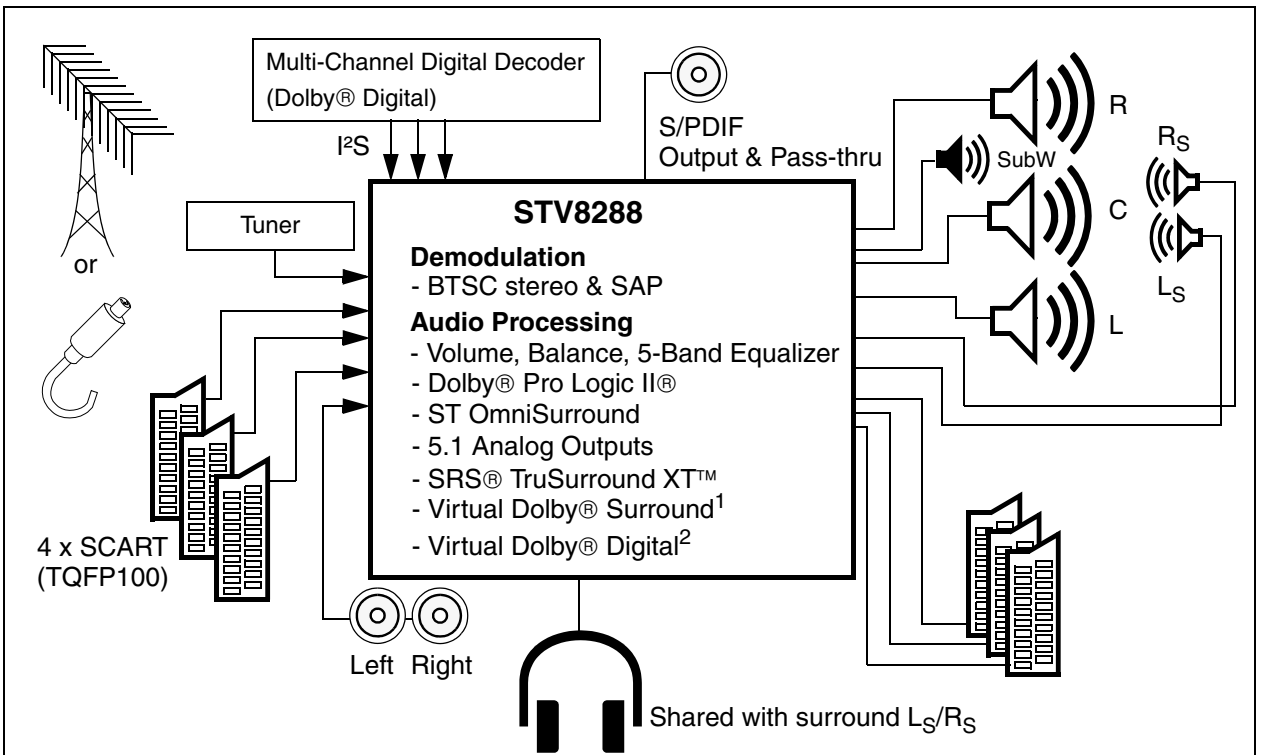
1. When using VDS with **ST OmniSurround** or **SRS TruSurround XT**™, an optional internal **Pro Logic**® decoder is mandatory.

Figure 7: STV8258 Typical Application (Digital: Virtual Sound)



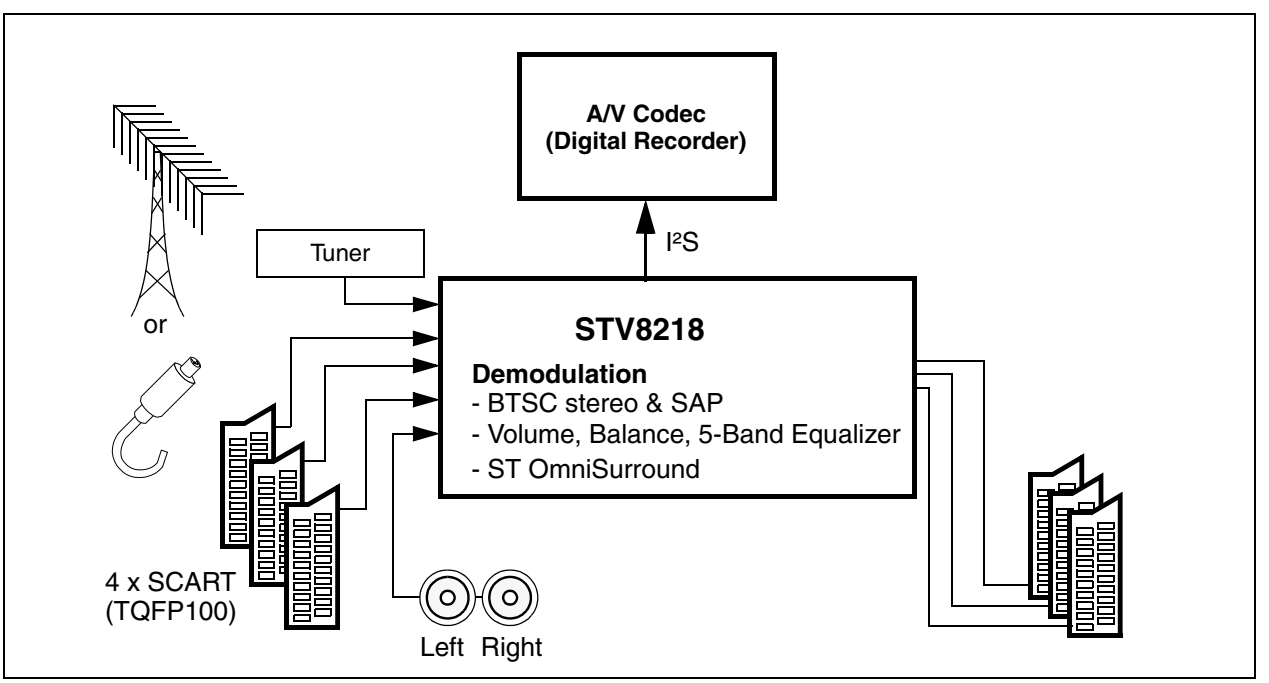
1. When using VDS with **ST OmniSurround** or **SRS TruSurround XT**™, an optional internal **Pro Logic**® decoder is mandatory.
2. When using VDD with **ST OmniSurround** or **SRS TruSurround XT**™, an external **Dolby**® **Digital** decoder is mandatory.

Figure 8: STV8288 Typical Application (Digital TV: Multi-Channel and Virtual Sound)



1. When using VDS with **ST OmniSurround** or **SRS TruSurround XT**™, an optional internal **Pro Logic**® decoder is mandatory.
2. When using VDD with **ST OmniSurround** or **SRS TruSurround XT**™, an external **Dolby**® **Digital** decoder is mandatory.

Figure 9: STV8218 Typical Application (DVD & HDD Recorders)



2 System Clock

The System Clock integrates 2 independent frequency synthesizers.

The first frequency synthesizer is used by the demodulator at a frequency of 24.576 MHz.

The second frequency synthesizer is used by the DSP core and can be adjusted between 100 and 150 MHz depending on the application.

The default values are designed for **a standard 27-MHz reference frequency** provided by a stable single crystal oscillator or an external differential clock signal (for example, from the STV35x0) depending on the CLK_SEL pin configuration (CLK_SEL = 1 means a single crystal oscillator, 0 means an external differential clock).

The 27-MHz value is the recommended frequency for minimizing potential RF interference in the application. The sinusoidal clock frequency, and any harmonic products, remain outside the TV picture and sound IFs (PIF/SIF) and Band-I RF.

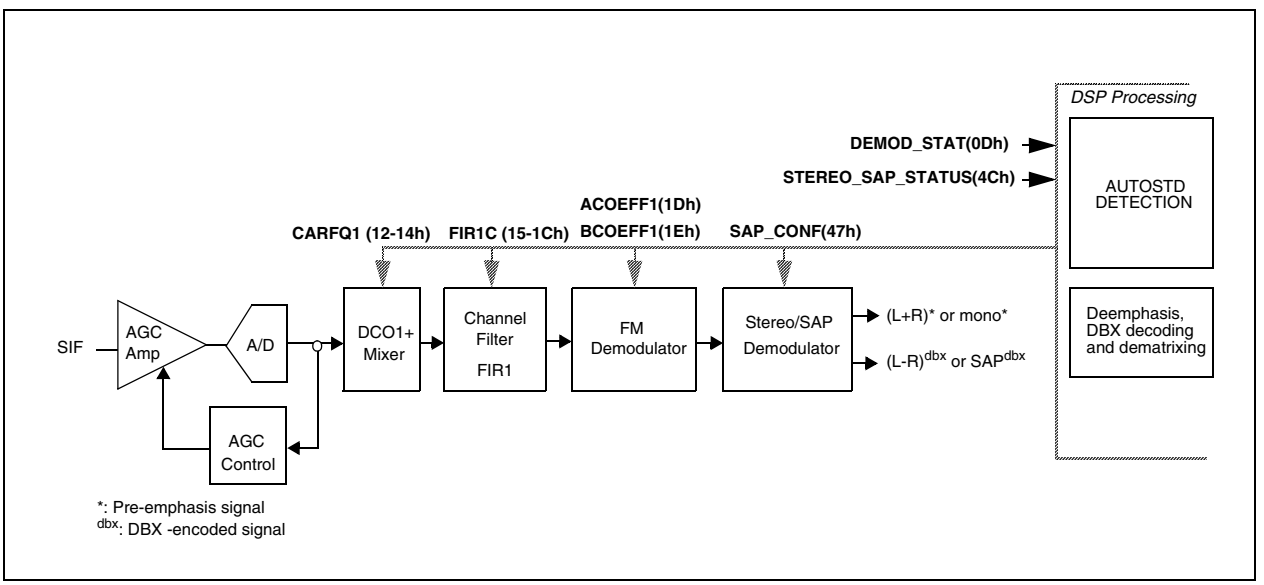
Note: A change in the reference frequency is compatible with other default I²C programming values, including those of the built-in Automatic Standard Recognition System.

3 Digital Demodulator

The Digital Demodulator (see Figure 10) consists of a channel demodulator and a stereo/SAP decoder.

All channel parameters are programmed automatically by the **built-in Automatic Standard Recognition System** (Autostandard) in order to find the STEREO or the SAP modes. Channel parameters can also be programmed manually via the I²C interface for very specific standards not included among the known standards.

Figure 10: Demodulator Block Diagram



3.1 Sound IF Signal

The Analog Sound Carrier IF is connected to the STV82x8 via the SIF pin. Before Analog-to-Digital Conversion (ADC), an Automatic Gain Control (AGC) is performed to adjust the incoming IF signal to the full scale of the ADC. A preliminary video rejection is recommended to optimize conversion and demodulation performances. The AGC system provides a gain value allowing for a wide range of SIF input levels.

The TQFP100 package provides a second SIF input.

3.2 Demodulation

The demodulation system operates by default in Automatic mode. In this mode, the STV82x8 is able to **identify and demodulate the BTSC TV sound standard including stereo and SAP modes** without any external control via the I²C interface.

The **built-in Automatic Standard Recognition System** (Autostandard) automatically programs the appropriate bits in the I²C registers which are forced to Read-only mode for users.

STEREO and SAP modes can be removed (or added) from the List of modes to be recognized by programming registers AUTOSTD_CTRL. The identified standard is displayed in register AUTOSTD_STATUS and any change to standard is flagged to the host system via pin IRQ. This flag

must be reset by re-programming the LSB of register IRQ_STATUS while checking the detected standard status by reading registers AUTOSTD_STATUS.

ITo recover out-of standard FM deviations or the Sound Carrier Frequency Offset, additional I²C controls are provided without interfering with the Automatic Standard Recognition System (Autostandard).

Table 4: BTSC Standard

Source	Modulation	Frequency Range	Audio Pre-processing	Sub-Carrier	Modulation Type	Sub-Carrier Deviation	Aural Carrier (4.5 MHz) Peak Deviation
Monophonic	L+R	0.05 -15 kHz	75 µs Pre-emphasis				25 kHz (1)
Pilot				0Fh			5 kHz
Stereophonic	L-R	0.05 -15 kHz	DBX Compression	2Fh	AM DSB SC		50 kHz(1)
SAP	2nd Channel	0.05 -15 kHz	DBX Compression	5Fh	FM	10 kHz	15 kHz

(1) L+R and L-R must not exceed 50 kHz

Sound Carrier Frequency Offset Recovery:IF Carrier frequency can be adjusted with register CAROFFSET1 within a large range (up to 120 kHz) while the Automatic Standard Recognition System remains active. The frequency offset estimation is written in registers DEMOD_DC_LEVEL and can be used to implement the Automatic Frequency Control (AFC) via an external I^2C control.

Manual Mode: If required, the Automatic Standard Recognition System system can be disabled (Manual mode) and the user can control all registers including those only controlled by the Automatic Standard Recognition System function when active. Manual mode is selected in register AUTOSTD_CTRL by setting to 0 bits SAP_CHECK, STEREO_CHECK and MONO_CHECK.

4 Dedicated Digital Signal Processor (DSP)

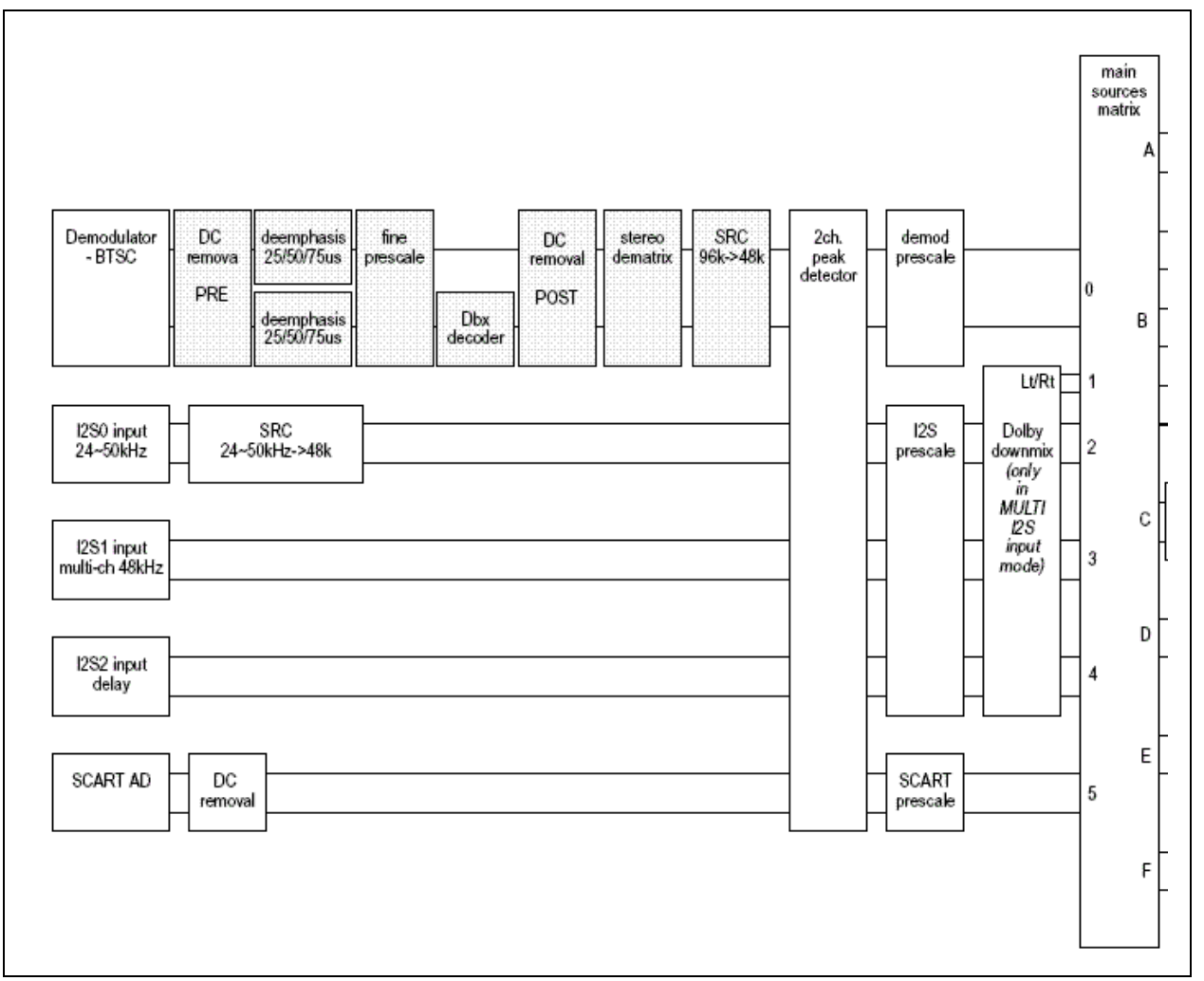
A dedicated Digital Signal Processor (DSP) takes charge of all audio processing features and the low frequency signal processing features of the demodulator. The internal 24-bit architecture will ensure a high quality signal treatment and an excellent dynamic.

4.1 Back-end Processing

The “back-end” processing corresponds to the low frequency signal processing (32 kHz or higher frequencies) of the demodulator and other inputs (I²S, ADC).

Figure 11 shows a flowchart of the back-end processing tasks. However, the figure shows that the processing is only a SINGLE SOURCE PROCESSING flow (no processing is possible with “Demod + SCART” and I²S inputs simultaneously) and that the selection of a headphone output restricts the loudspeakers configuration to 2.1 instead of 5.1.

Figure 11: Back-end Audio Processing



The main features depend on the path:

- FM Channel
  - — DC Removal
  - — Prescaling
  - — De-emphasis (50 or 75 us)
  - — Stereo Dematrix
- Input SCART Channel
  - — DC Removal
  - — Prescaling
- Input I²S Channel
  - — I²S Prescaling
- Digital Audio Matrix
  - — Audio Channel Multiplexer between the different sources (IF, I²S, SCART) towards all outputs (S/PDIF, LS, HP or SCART).
- Autostandard management
  - — device configuration depending on the standard to be detected
  - — freeze the device when a standard is detected
  - — once a standard detected, check that there is no change in the detection status
  - — set the correct action depending on any change in the detection status (mono backup or mute setup and new standard detection)
- SCART
  - — Downmixing: L_T / R_T or L_0 / R_0 (see AC-3 specification)
  - — Soft Mute

4.2 Audio Processing

The following software is provided for main loudspeakers (L, R, C, L_S, R_S, SubW):

- Downmix
- Dolby® Pro Logic II® Decoder (L_T, R_T →L, R, C, Ls, Rs, SubW) with Bass Management
- ST WideSurround, ST OmniSurround, SRS® WOW™ or SRS® TruSurround XT® (certified Virtual Dolby® Surround and Virtual Dolby® Digital)
- ST Dynamic Bass and ST Bass Enhancer
- Smart Volume Control (SVC)
- 5-band Equalizer or Bass-Treble
- Loudness
- Volume with independent channels (Smooth Volume Control)
- Master Volume Control
- Mute/soft-mute
- Balance
- Beeper
- Pink Noise Generator (used to position the loudspeakers)
- Programmable Delay for each loudspeaker
- Adjustable Delay for “lip sync” up to 120 ms (to compensate for audio/video latency)

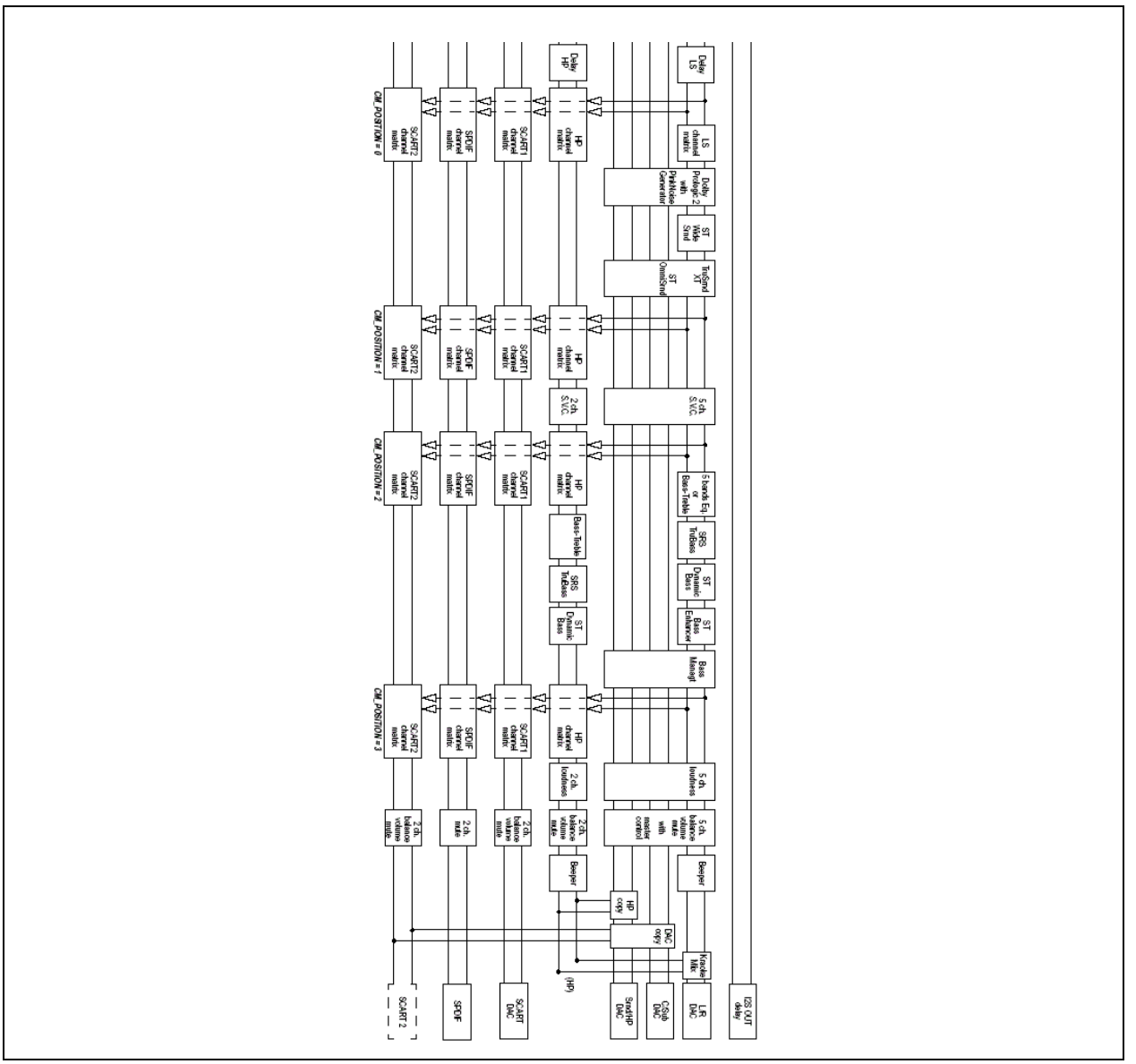
The following software is provided for the headphone or auxiliary output:

- Downmix
- SRS® TruBass™
- ST Dynamic Bass
- Smart Volume Control (SVC)
- Bass/Treble
- Loudness
- Independent Volume for each channel (Smooth Volume Control)
- Soft Mute
- Balance
- Beeper
- Adjustable Delay for “lip sync” feature up to 120 ms (to compensate for audio/video latency)

The following software is provided for SCART or S/PDIF outputs:

- Downmix
- Soft Mute

Figure 12: Audio Processing for Loudspeakers, Headphone, SCART and S/PDIF outputs



4.3 ST WideSurround

STV82x8 offers three preset ST WideSurround Sound effects on the Loudspeakers path:

- Music, a concert hall effect
- Movie, for films on TV
- Simulated Stereo, which generates a pseudo-stereo effect from mono source

“ST WideSurround Sound” is an extension of the conventional stereo concept which improves the spatial characteristics of the sound. This could be done simply by adding more speakers and coding more channels into the source signal as is done in the cinema, but this approach is too costly for

normal home use. The ST WideSurround system exploits a method of phase shifting to achieve a similar result using only two speakers. It restores spatiality by adding artificial phase differences.

The Surround/Pseudo-stereo mode is automatically selected by the Automatic Standard Recognition System (Autostandard) depending on the detected stereo or mono source. By default, “Movie” is selected for Surround mode. This value may be changed to “Music” by the WIDESRND_MODE bit in the WIDESRND_CONTROL register.

Additional user controls are provided to better adapt the spatial effect to the source. The ST WideSurround Gain (WIDESRND_LEVEL) and ST WideSurround Frequency (WIDESRND_FREQ) registers can be used to enhance Music Predominancy in Music mode and Theater effect and Voice Predominancy in Movie mode.

4.4 ST OmniSurround

STV82x8 offers a spatial virtualizer to output any multi-channel input in stereo on the Loudspeakers path.

“ST OmniSurround” will recreate a multi-channel spatial sound environment using only the Left and Right front speakers. It can be adapted to any input configuration (OMNISRND_INPUT_MODE).

ST Voice will allow you to enhance the voice content of your program to increase the intellegibility and the presence of the sound.

4.5 Dolby Pro Logic II Decoder

Dolby® Pro Logic II® is a matrix decoder that decodes the five channels of surround sound that have been encoded onto the stereo sound tracks of Dolby® Surround program material such as DVD movies and TV shows.

It is even possible to decode standard stereo signals like music or non encoded movies. Furthermore, it is an active process designed to enhance sound localization through the use of very high-separation decoding techniques.

The Dolby® Pro Logic II® decoder is also able to emulate the former Dolby® Pro Logic® decoder in a specific mode.

4.6 Bass Management

This processing will generate the subwoofer signal and adjust all loudspeakers channels gain and bandwidth.

Speakers capable of reproducing the entire frequency range will be referred to as “full range speakers”, then signals sent to full range speaker will be full bandwidth (no filtering).

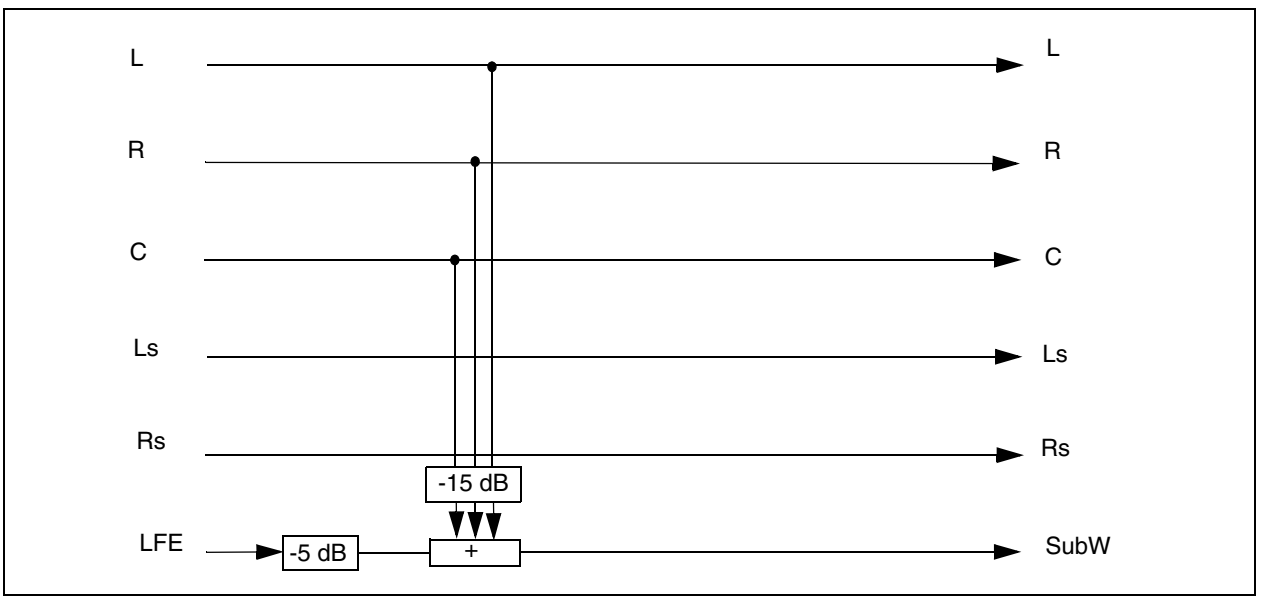
Speakers that have limited bass handling capabilities will be referred to as “satellite speakers”, then signals sent to satellite speaker will be high-pass filtered to remove bass information below 100 Hz.

In the STV82x8, five output configuration modes have been implemented according to “Dolby Digital Consumer Decoder” specifications. They are described below.

4.6.1 Bass Management Configuration 0

In some cases, the bass management filters are available in the decoder itself, so there is no need to reproduce these filters. The output configuration shown in Figure 13 offers this possibility.

Figure 13: Bass Management Configuration 0 (with Pro Logic switch indicating its reset state)

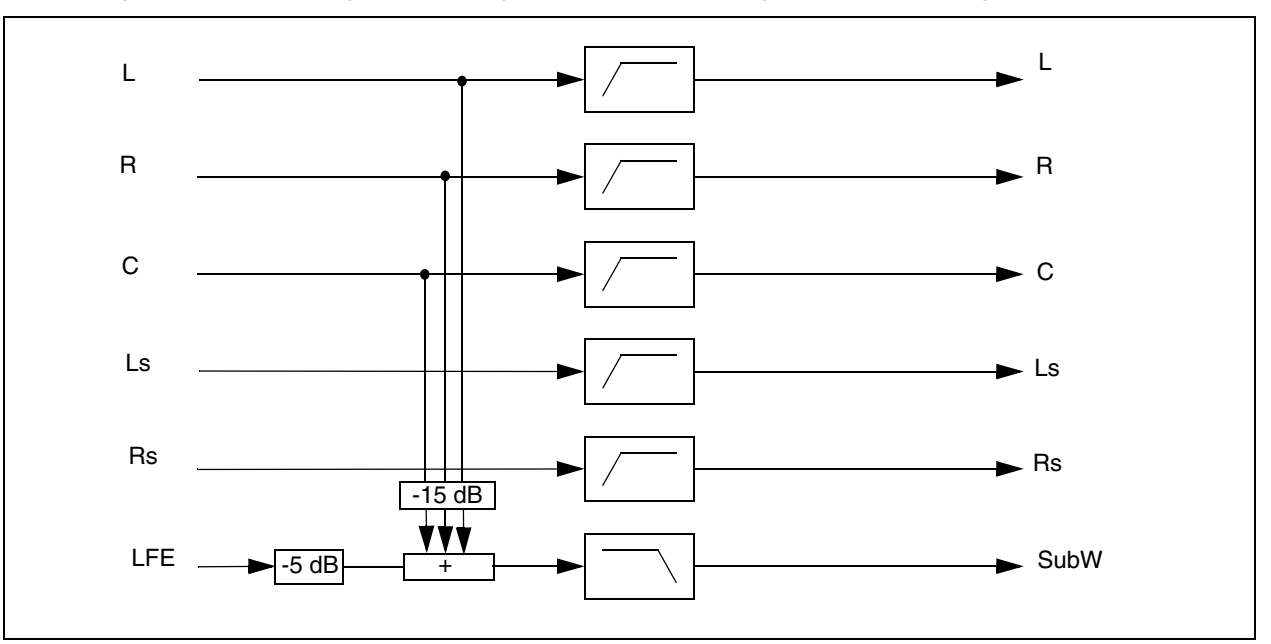


4.6.2 Bass Management Configuration 1

Configuration 1, shown in Figure 14, assumes that all five speakers are not full range and that all of the bass information will be redirected to and reproduced by a single subwoofer. This configuration is intended for use with 5 satellite speakers.

To prevent signal overload, the five main channels are attenuated by 15 dB, while the LFE channel is attenuated by 5dB to maintain the proper mixing ratio.

Figure 14: Bass Management Configuration 1 (with Pro Logic switch indicating its reset state)

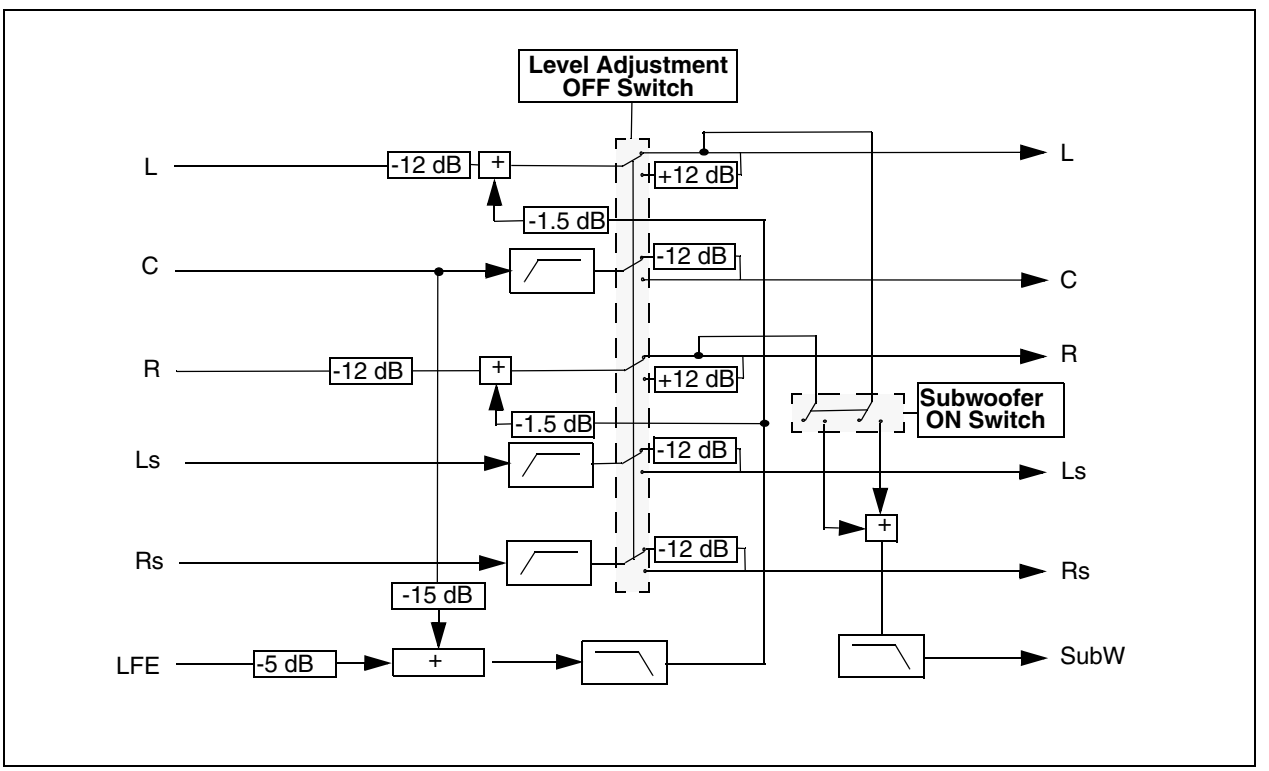


4.6.3 Bass Management Configuration 2

Configuration 2 assumes that the left and right speakers, are full range while the center and surround speakers are smaller speakers. Also, all bass data is redirected to the left and right speakers.

This configuration include output level adjustment that allows 12 dB attenuation for the 3 smaller speakers (C, Ls, Rs). When the level adjustment will be disabled the decoder boosts by 12 dB the full range speakers (Left, Right).

Figure 15: Bass Management Configuration 2 (all switches indicate their reset state)

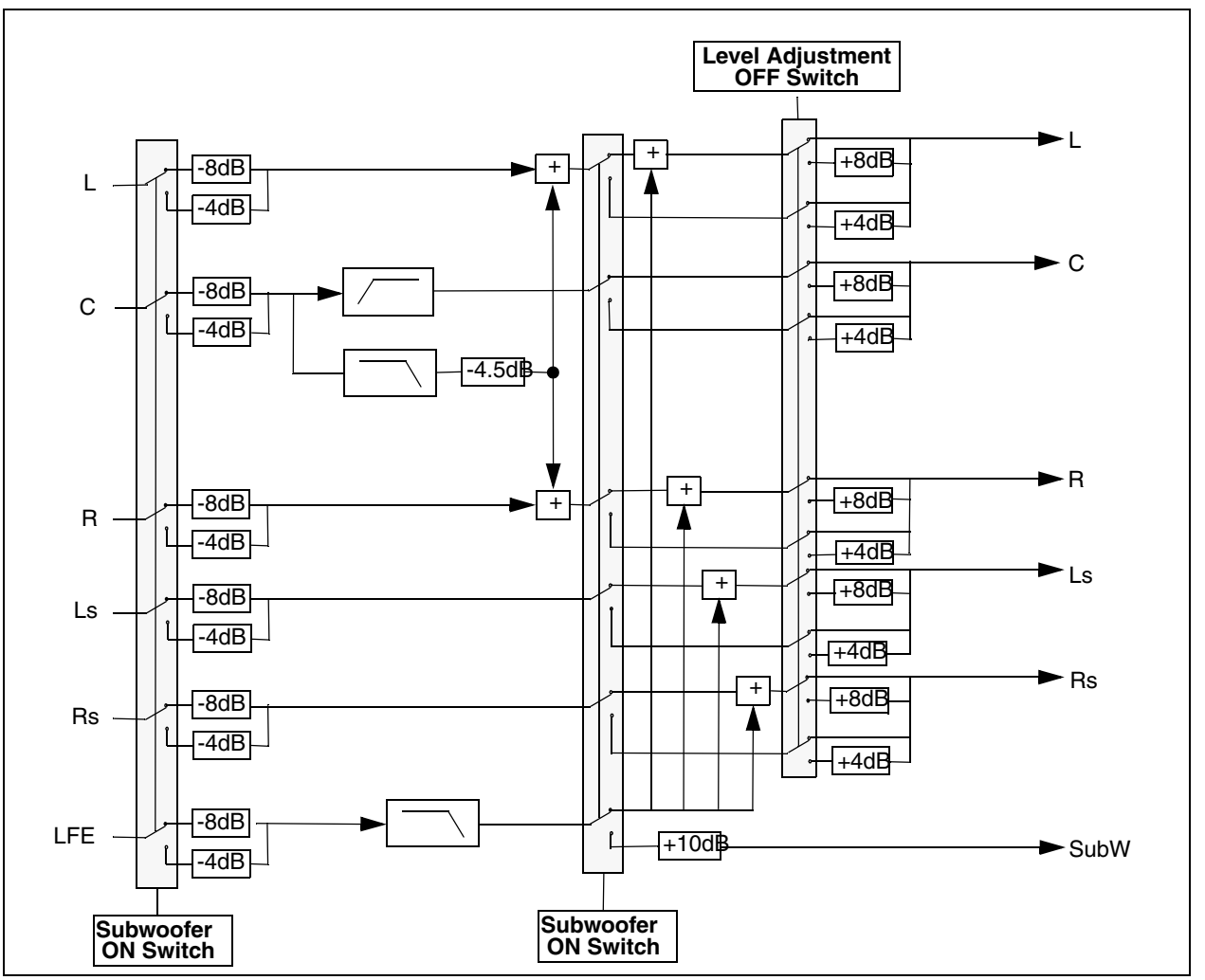


4.6.4 Bass Management Configuration 3

The third configuration, shown in Figure 16, assumes that all speakers except the center are full range, then all bass information will be directed to and reproduced by the front left and front right and both surround speakers. In order to provide more flexibility to this configuration, a switch will offer an option which will produce a subwoofer channel by the LFE channel.

When the Subwoofer Switch is OFF, the input channels will be attenuated by 8 dB. Configuration 3 is required in certain high-end products.

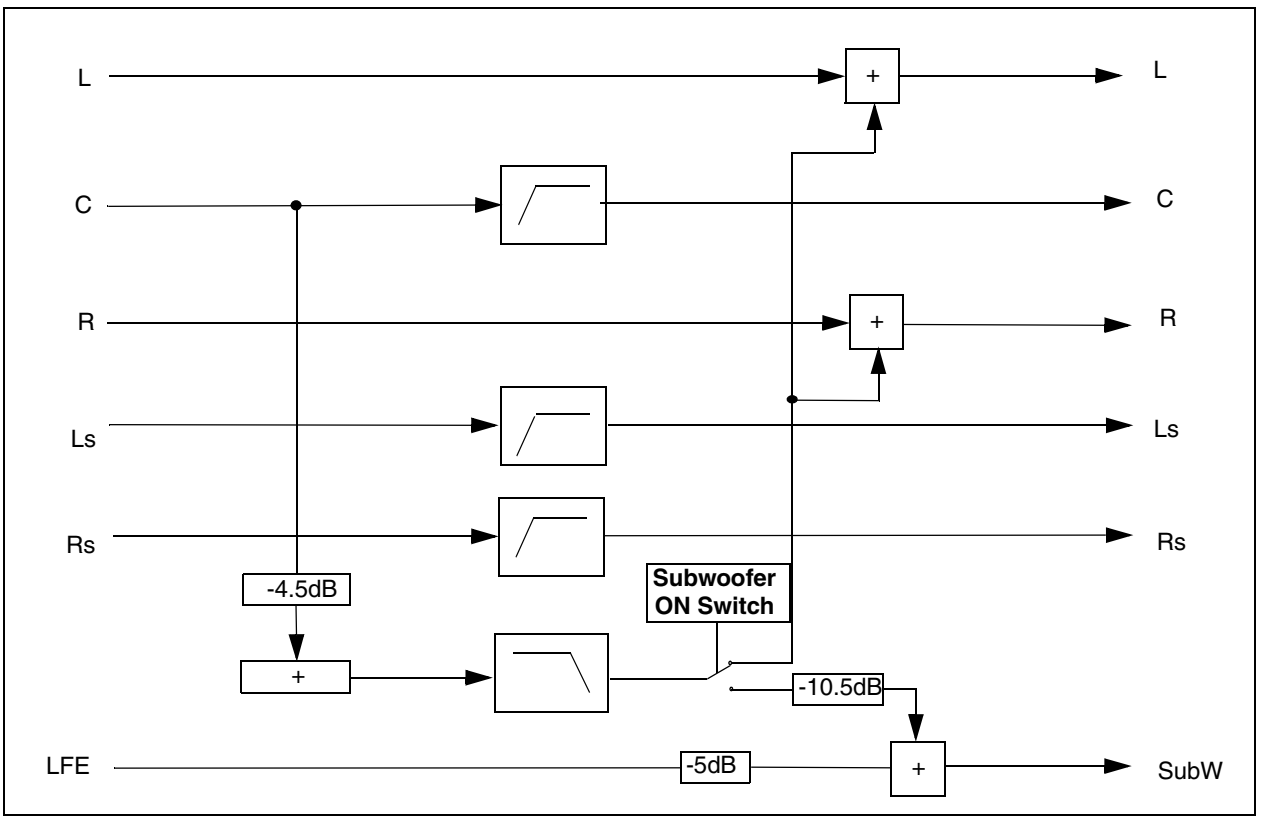
Figure 16: Bass Management Configuration 3 (all switches indicate their reset state)



4.6.5 Bass Management Configuration 4

This configuration implements the Simplified Dolby configuration. The center, left surround and right surround channels are summed and then filtered by the LPF. The composite bass information is either summed back into the left and right channels or summed with the LFE channel and sent to the subwoofer output, see Figure 17.

Figure 17: Implementation of the Bass Management Configuration 4 (Simplified Configuration)



4.7 SRS WOW and TruSurround XT

The SRS® TruSurround XT™ is a processing system that can accept from 1 to 6 channels on input and that will generate a 2-channel output signal.

This processing system includes the latest SRS® algorithms:

- SRS® WOW™
- SRS® TruSurround® (Multi-channel signal virtualizer)

4.7.1 SRS TruSurround

The SRS® TruSurround® is a processing that can accept from 2 to 5 channels on input and that will generate a 2-channel output signal.

SRS® TruSurround® uses Head-Related Transfer Function (HRTF) -based frequency tailoring of (L/R) difference signals to extend the sound image out past the physical boundaries of the speaker placements to surround channel information. These rear channel HRTF curves have much greater peak to valley differences at center frequencies. These were chosen to cause rear channel difference signals to virtualize farther behind the listener and directed to a different virtual position as compared to front channel signals. Information that is equal (L+R) in the rear surround channels

is processed by an identical HRTF curve but mixed in at a much lower amount. This HRTF processing of equal (L/R) signals was again used to virtualize information to the rear of the listener.

The SRS® TruSurround® is certified by Dolby Laboratories to be a Virtual Dolby® Digital and Virtual Dolby® Surround.

4.7.2 SRS WOW

The SRS® WOW™ is an a sound processing system including:

- SRS® 3D Mono/Stereo™
- SRS® Dialog Clarity™
- SRS® TruBass™

4.7.2.1 SRS 3D Mono/Stereo

This system is used to create a pseudo-stereo signal for mono inputs or a three-dimensional spatial signal for stereo inputs.

4.7.2.2 SRS Dialog Clarity

This system is used to enhance dialog perception.

4.7.2.3 SRS TruBass

The SRS® TruBass™ audio enhancement technology provides deep, rich bass to small speaker systems without the need for a subwoofer or additional extra physical components. For systems with a subwoofer, TruBass™ complements and enhances bass performance. Psycho-acoustically, when the human ear is presented with a low frequency sound signal that is missing the fundamental harmonic, it will fill in the fundamental frequency based on the higher harmonics that are present. By accentuating the second and higher frequency harmonics of the bass portion of a signal, TruBass™ gives the perception of greatly improved bass response.

SRS® TruBass™ is implemented on loudspeakers path, headphone path or on both in parallel.

4.8 Smart Volume Control (SVC)

The Smart Volume Control regulates the audio signal level before audio processing. This regulation is necessary in order for the signal level to be independent from the source (terrestrial channels, I2S or SCART), its modulation (FM) and annoying volume changes (advertising, etc.). The Smart Volume Control works as an audio compressor/expander; i.e. when the input signal exceeds the threshold level, a very rapid attenuation (-2 dB/ms) is applied to rescale the signal down to the threshold value. When the input signal is below the threshold level, the previous attenuation is reduced slowly in order to retrieve the original input level (0dB gain). If the input signal is too low, an addition gain of 6 dB can be provided.

To personalize the action of the SVC, five parameters are available:

1. Threshold: Maximum quasi-peak level that can be expected on output
2. Peak measurement mode: Select the channel on which the peak measurement must be performed (Left, Right, Center...)
3. Release time: Gain slope applied to the amplification phase
4. Expander switch: To allow a +6dB amplification of small signals in order to reduce the output dynamic range
5. Make up gain: Allows compensation of the signal amplitude limitation thanks to a 0 to 24 dB adjustable gain.

The SVC is implemented on the loudspeakers path, headphone path or on both in parallel (independent settings). Also, the SVC can be applied in six-channel mode (L, R, L_S, R_S, C and SubW).

4.9 ST Dynamic Bass/ST Bass Enhancer

STV82x8 offers dynamic bass boost processing on the Loudspeakers path:

ST Dynamic Bass is a bass boost process that can dramatically increase the bass content of any program without any output level saturation.

3 cutoff frequencies (BASS_FREQ) can be chosen, 100 Hz, 150 Hz and 200 Hz to adapt the effect to your loudspeakers. The amount of bass (BASS_LEVEL) can also be fine tuned in order to adapt the effect loudness.

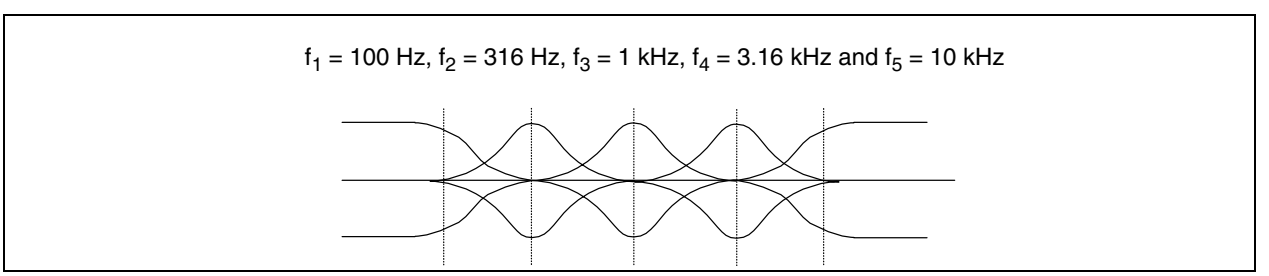
4.10 5-Band Audio Equalizer

The loudspeakers audio spectrum is split into 5 frequency bands and the gain of each of band can be adjusted within a range from -12 dB to +12 dB in steps of 0.25 dB. The Audio Equalizer may be used to pre-define frequency band enhancement features dedicated to various kinds of music or to attenuate frequency resonances of loudspeakers or the listening environment. The Equalizer is enabled by the LS_EQ_ON bit in the EQ_BT_CTRL register. The gain value for Band X is programmed in register LS_EQ_BANDX.

The 5-Band Audio Equalizer is exclusive with Bass-Treble control. Bit LS_EQ_BT_SW in register EQ_BT_CTRL is used to select either the 5-Band Audio Equalizer or the Bass-Treble control for the Loudspeakers path.

Depending on the LS Equalizer or LS Bass-Treble value, the volume level can be clamped to the LS output to prevent any possible signal clipping from occuring using the ANTICLIP_LS_VOL_CLAMP bit in the VOLUME_MODES (D7h) register.

Figure 18: Equalizer



4.11 Bass/Treble Control

The gain of bass and treble frequency bands for Headphone can be also tuned within a range from -12 dB to +12 dB in steps of 0.25 dB. It may be used to pre-define frequency band enhancement features dedicated to various kinds of music. The Headphone Bass/Treble feature is enabled by setting the HP_BT_ON bit in the EQ_BT_CTRL register. The Bass and Treble gain values are adjusted in registers HP_BASS_GAIN and HP_TREBLE_GAIN, respectively.

Depending on the HP Bass-Treble value, the volume level can be clamped to the HP output to prevent any possible signal clipping from occuring using the ANTICLIP_HP_VOL_CLAMP bit in the VOLUME_MODES (D7h) register.

4.12 Automatic Loudness Control

As the human ear does not hear the audio frequency range the same way depending on the power of the audio source, the Loudness Control corrects this effect by sensing the volume level and then boosting bass and treble frequencies proportionally to middle frequencies at lower volume.

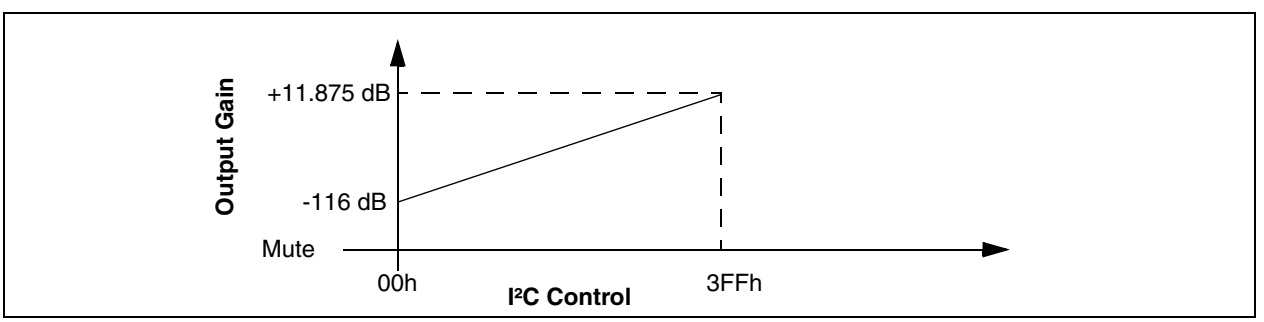
While maintaining the amplitude of the 1 kHz components at an approximately constant value, the gain values of lower and higher frequencies are automatically progressively amplified up to +18 dB when the audio volume level decreases.The maximum treble amplification can be adjusted from 0 dB (first order loudness) to +18 dB (second order loudness) in steps of 0.125 dB. As the volume is proportional to the external audio amplification power, the loudness amplification threshold is programmable in order to tune the absolute level. The Loudspeakers Loudness function is enabled by setting the LS_LOUD_ON bit in register LS_LOUDNESS. The Loudspeakers Loudness Threshold and Maximum Treble Gain values are also programmed in this register. The Headphone Loudness function is enabled by setting the HP_LOUD_ON bit in register HP_LOUDNESS. The Headphone Loudness Threshold and Maximum Treble Gain values are also programmed in this register.

The loudness cut-off frequency is 100 Hz.

4.13 Volume/Balance Control

The STV82x8 provides a Volume/Balance Control for all output channels configuration (except for S/PDIF) with different volume level per channel (L, R, C, L_S, R_S, SubW, SCART). Its wide range (from +11.875 to -116 dB, in a dB linear scale with a 0.125 dB step) largely covers typical home applications (approx. 60 dB) while maintaining a good S/N ratio.

Figure 19: Volume Control



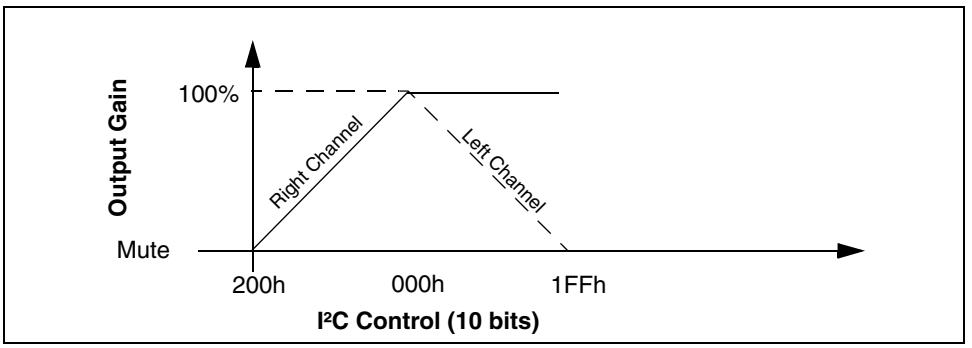
An extra Master Volume Control can apply an extra gain/attenuation on L, R, C, L_S, R_S and SubW channels.

The Volume/Balance Control can operate in one of two different modes:

- In **Differential mode** (default value), the volume control is a common volume value for both the Left and Right Loudspeakers or Headphone channels (see Figure 19) and complimentary balance control is used (see Figure 20).

- In **Independent mode**, the volume for the Left and Right channels for Loudspeakers or Headphone is controlled independently.

Figure 20: Differential Balance



4.14 Soft Mute Control

The Digital Soft Mute is applied smoothly (20 ms for 120 dB range) to avoid any switch noise on output. It is available on all output channels pairs:

- S/PDIF channel (Left/Right)
- SCART channels (Left/Right)
- Loudspeakers channels (Left/Right)
- Center
- Subwoofer
- Headphone/Surround channels (Left/Right)

Another soft mute (analog) is also available on each DAC output.

4.15 Beeper

The beeper is used to generate a tone on the Loudspeakers or/and Headphone outputs. The beeper sound (square wave) is added to the audio signal which is attenuated by 20 dB. The beep sound amplitude includes a smooth attack and decay to avoid any parasitic noise when starting and stopping.

It can be used for various applications such as beep sounds for remote control, alarm clock or other features.

The Beeper operates in one of two modes:

- **Pulse mode** (beep applications): A tone with a programmable short duration (0.1, 0.25, 0.5 and 1.0 s) is generated. Afterwards, the beeper is automatically disabled and the output is switched back to the audio signal, see Figure 21.
- **Continuous mode** (alarm application): A tone with a programmable long duration is generated. Its start and stop controls must be programmed by I²C, see Figure 22.

The Beeper function is enabled by setting the BEEPER_ON bit in register BEEPER_ON.

Beeper parameters are controlled in register BEEPER_MODE.

The beeper tone level and frequency are programmed in register BEEPER_FREQ_VOL. The level (or volume) ranges between 0 dB and -93 dB in steps of 3 dB and the tone frequency ranges between 62.2 Hz and 8 kHz in steps of 1 octave.

A beep generator is shared only by the Loudspeakers or Headphone outputs. Therefore, in the event of simultaneous beeps when in Pulse mode, only the first beep will define the effective duration that will be the same for both outputs.

Figure 21: Pulse Mode

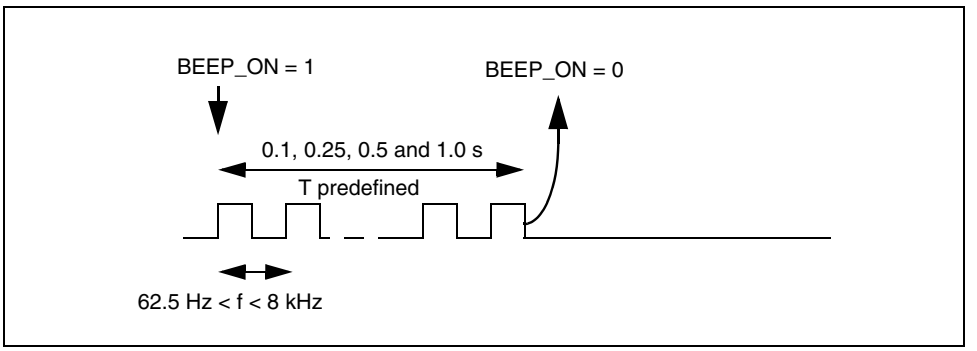
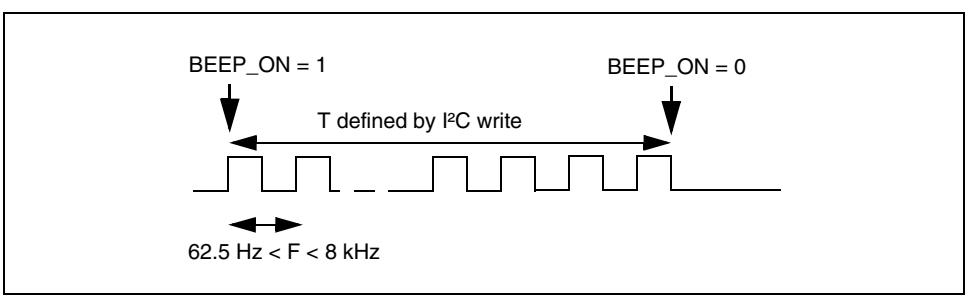


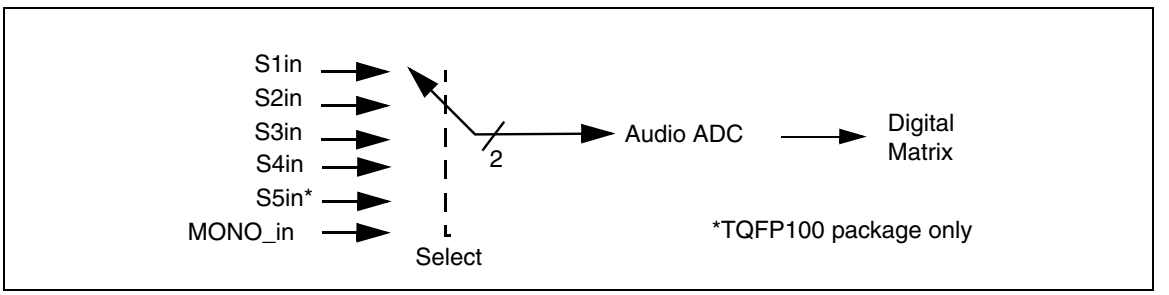
Figure 22: Continuous Mode



5 Analog Audio Matrix (Input / Output)

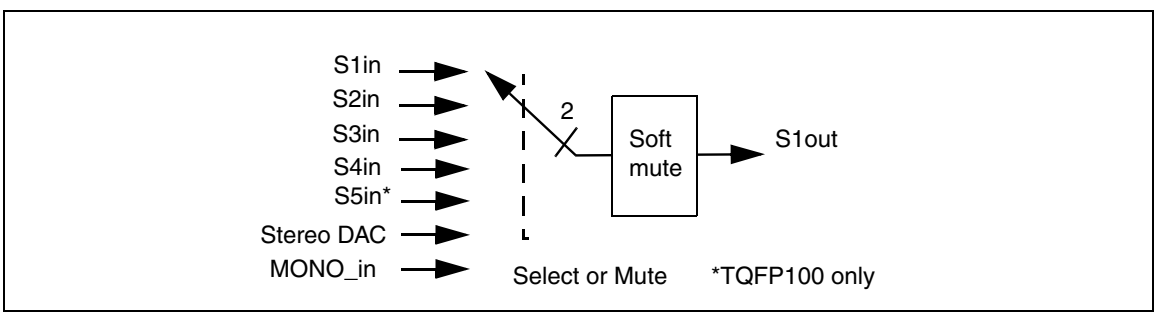
The analog part of the audio matrix can be divided into two parts: the SCART input matrix and the SCART output matrix.

Figure 23: SCART Input Matrix



The SCART input matrix is an input for the digital matrix (after the ADC) which select which source will be sent to the DSP.

Figure 24: SCART1/2/3 Output Matrix



The SCART output matrix selects the sound to output, which can be directly a SCART input or the output of the DSP. A mute function is provided to switch off the outputs.

A soft-mute function is provided to avoid all spurious sounds when switching from one position to another position.

The SCART 2 and 3 output matrices have the same functions as the SCART 1 output matrix.

The particularity of the matrix is to accept input signal of 2 V_{RMS} and to have the capability to output such level. In this case, the power supply must be 8 V.

The Mono audio input is able to accept signals with a 0.5 V_{RMS} amplitude.

6 I²S Interface (In / Out)

6.1 I²S Inputs

6.1.1 I²S Inputs in TQFP 80 Package

The STV82x8 can interface with a digital sound decoder. In this case, the digital data can be input at a speed of 0.384 Mbytes/s (3.072 MHz for a 48 kHz sampling frequency with 32 bits of data).

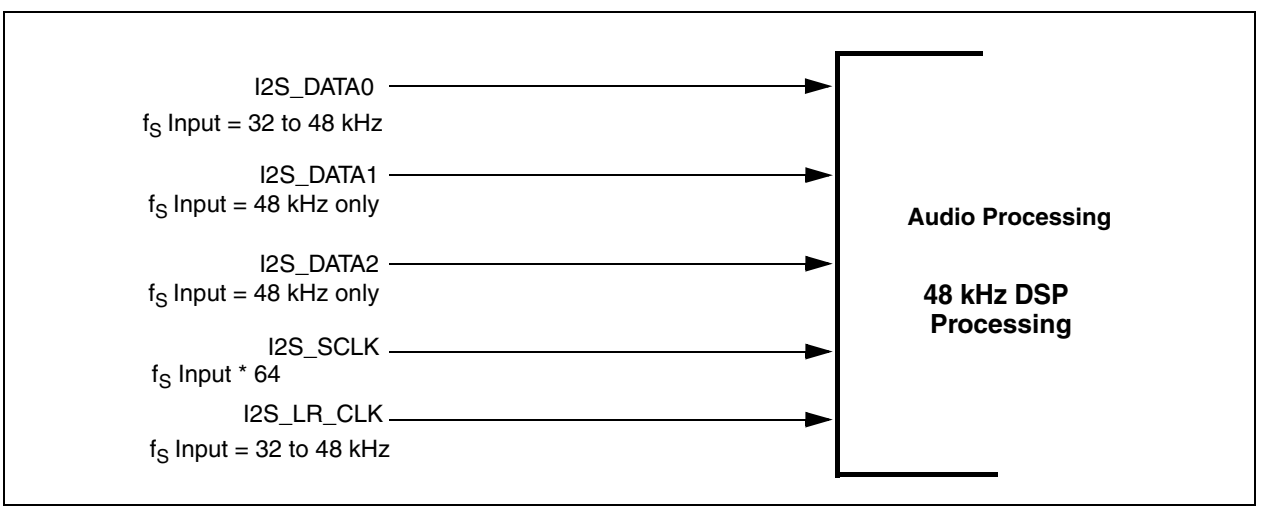
A Sample Rate Conversion (SRC) is necessary if input frequency is not 48 kHz (STV82x8 slave) in order to obtain a fixed frequency output from this block (48 kHz).

Note: The SRC function is only available in single I²S input mode.

The interface with one I²S connection (I2S_DATA0) enables the input of stereo or stereo-coded Dolby® Pro Logic®.

One interface with three I²S connections connected to the DSP enables the processing of a multi-channel signal (maximum of 6 channels).

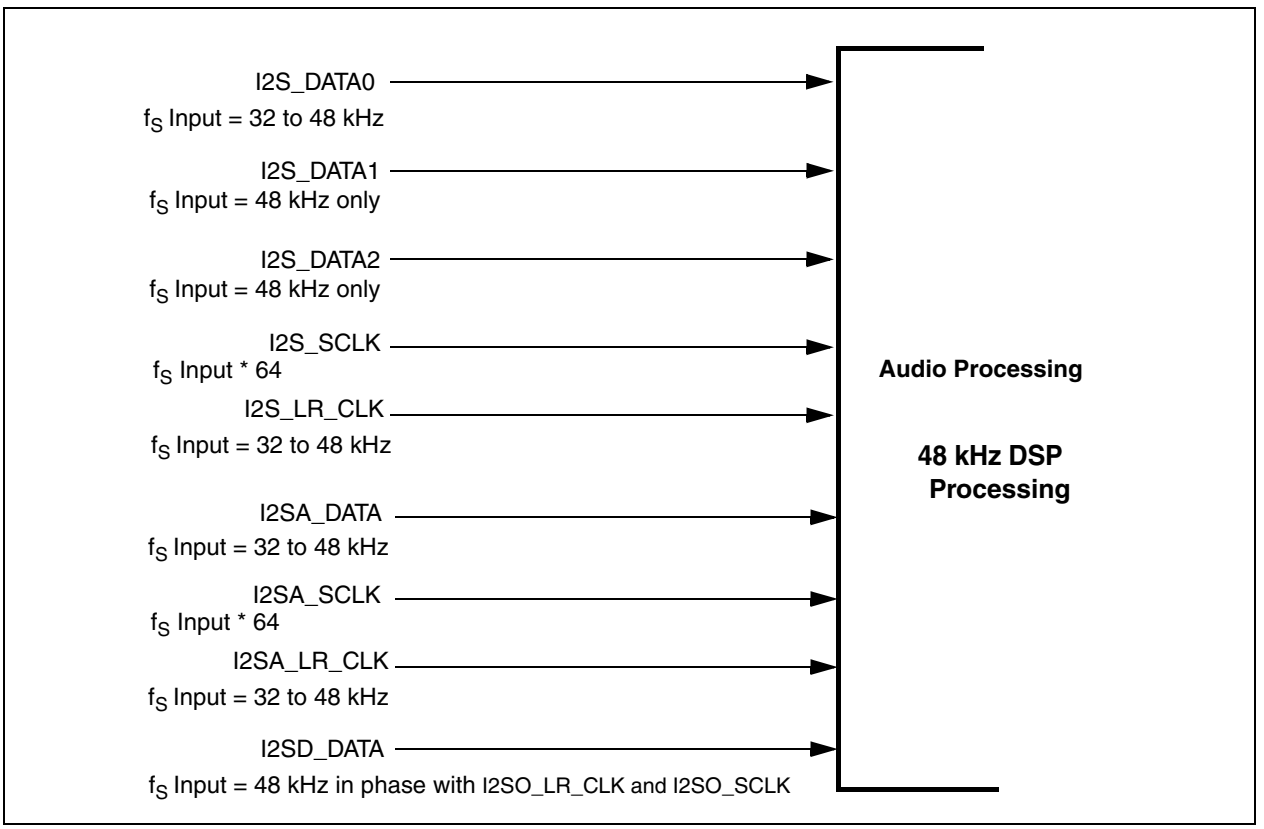
Figure 25: TQFP 80 I²S Input Block Diagram



6.1.2 I²S Inputs in TQFP 100 Package

An additional (auxiliary) asynchronous input is available in the TQFP100 package. An I2SD_DATA input for external delay is also available, but it must be in phase with the I²S output clocks.

Figure 26: TQFP100 I²S Input Block Diagram



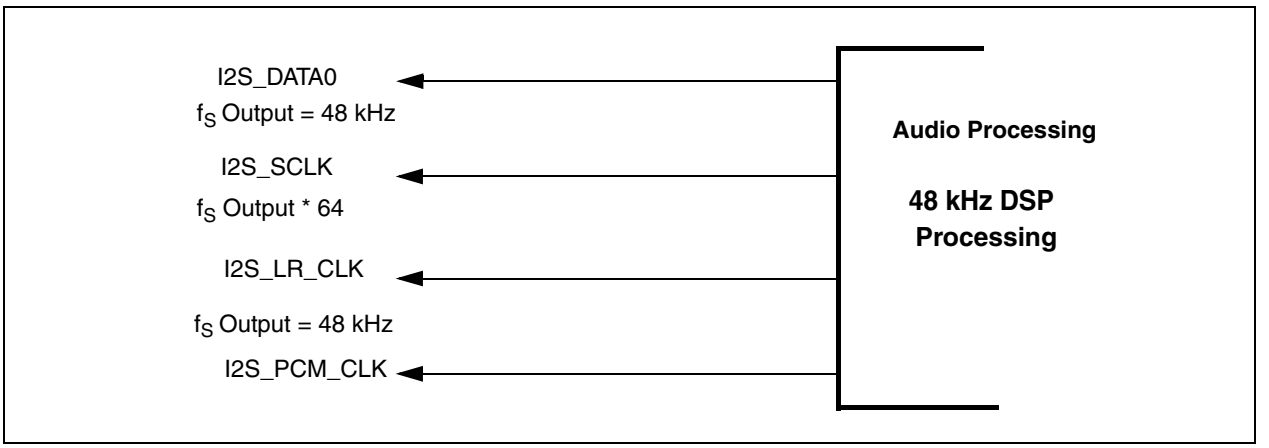
6.2 I²S Outputs

6.2.1 I²S Outputs in TQFP 80 Package

A digital stereo output (I²S compatible) is also available for routing the demodulated signal or a converted input audio signal to an external device. In this case, the I2S_DATA0 signal and all clock signals are set as outputs by setting bit D5 in register RESET to 1 (and bit D6 for the clocking). The STV82x8 drives the serial bus (I2S_SCLK, I2S_LR_CLK, and I²2S_DATA0) in master mode in 64.fs format with a sampling frequency (f_s) of 48 kHz. The I2S_PCM_CLK signal can be used as a master clock for the slave interface, if required. Both standard and non-standard modes are available.

.

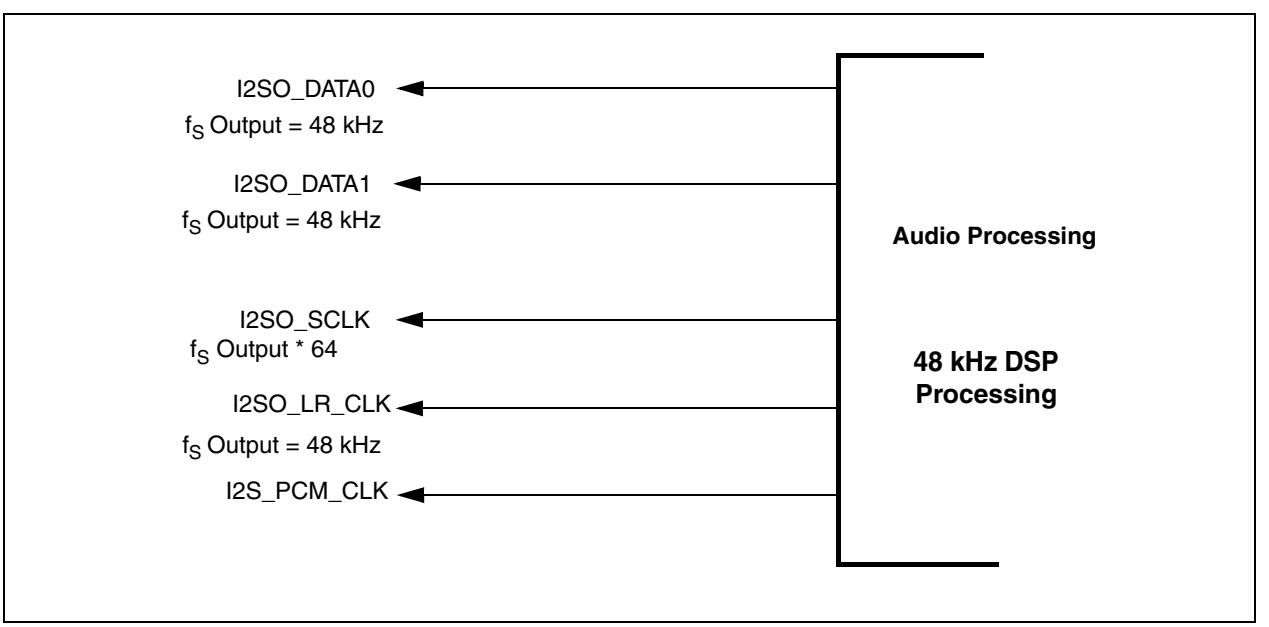
Figure 27: TQFP 80 I²S Output Block Diagram



6.2.2 I²S Outputs in TQFP 100 Package

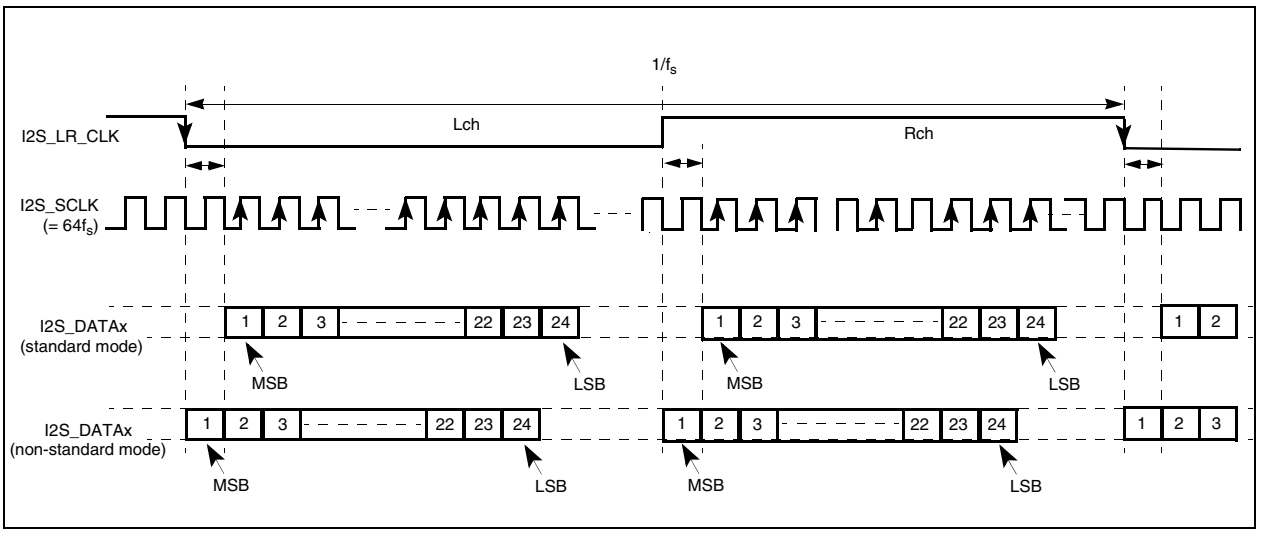
Two digital stereo outputs (I²S compatible) are available for routing the demodulated signal or a converted input audio signal to an external device or perform an external delay. In this case, the I2SO_DATA0 and I2SO_DATA1 signals are available with all I²S inputs active. The STV82x8 drives the serial bus (I2SO_SCLK,I2SO_LR_CLK, I2SO_DATA0, and I2SO_DATA1) in master mode in 64.fs format with a sampling frequency (fs) of 48 kHz. The I2S_PCM_CLK signal can be used as a master clock if required for the slave interface. Both standard and non-standard modes are available. .

Figure 28: TQFP100 I²S Output Block Diagram



Note: The Input and Output modes for I²S are exclusive in the TQFP80 package.

Figure 29: I²S Data Format: Lch = LOW, Rch = HIGH (I²S Input or Output mode)



7 S/PDIF Input/Output

An S/PDIF output is available for connection with an external decoder/amplifier. An internal multiplexer allows selection of either the internal signal or the external signal connected on the S/PDIF input (for example, the signal provided by the external MPEG audio / Dolby Digital decoder). The outputted internal signal can be selected from:

- L/R
- C/Sub
- HP or Surround
- SCART

A Mute facility is also provided on the S/PDIF output.

8 Power Supply Management

A mixed supply voltage environment requires the following voltages:

- 3.3V capable inputs/outputs for digital pins;
- 1.8V digital core;
- 8V capable inputs/outputs for analog audio interfaces (capability to output 2 V_{RMS} for SCART requirements);
- 3.3V for stereo ADC and DAC (analog part);
- 1.8V for stereo ADC and DAC (digital part);
- 1.8V for IF ADC and AGC.

These voltages will be delivered by the application with an accuracy of **±5%**. For more information, refer to Section 16.3: Power Supply Data.

Other specific DC voltages or features are provided:

- Voltage Reference and Biasing Generation (AGC, ADCs, DACs),
- Bandgap reference.

8.1 Standby Mode (Loop-through mode)

The STV82x8 provides a Loop-through mode configuration that bypasses IC functions via a SCART I/O pin (Full Analog Path only). In this case, only a minimum power of 200 mW is required.

In Standby mode, the digital and analog power supplies are switched off, except for pins VCC_H, VCC33_LS, VCC33_SC, and VCC_NISO which are used to maintain the SCART path with the last configuration programmed by analog matrixing (register SCART1_2_OUTPUT_CTRL and SCART3_OUTPUT_CTRL). When switching back to normal Full Power mode, all I²C registers are reset except for those used in Standby mode to maintain the original configuration.

In Standby mode, the I²C bus does not operate. However, the bus can still be used by other ICs since the I²C I/O pins (SDA and SCL) of the STV82x8 are forced into a high-impedance configuration.

9 Additional Controls and Flags

This logic contains:

- the headphone detection,
- the IRQ generation, signal to be output to the MCU,
- the I²C bus expander output pin.

9.1 Headphone Detection

For headphone, the $\overline{\text{HP\_DET}}$ input can be used to automatically mute the Loudspeakers and Subwoofer outputs when the HP_LS_MUTE bit is set in register HEADPHONE_CONFIG (active low). When a headphone is detected (the $\overline{\text{HP\_DET}}$ pin is set to 0) and the Mute function is enabled. Each change on the $\overline{\text{HP\_DET}}$ pin generates an IRQ request to the microprocessor on the IRQ pin.

9.2 IRQ Generation

Four IRQs are generated by the STV82x8. On each IRQ generation, the IRQ pin is set to 1. The pending IRQ status must be read at the I²S address 81h and the acknowledge is done by writing 0 to this register.

The four availables IRQs are:

IRQ0: The identified TV sound standard is displayed in register AUTOSTD_STATUS. Each change in the detected standard is flagged to the host system via hardware pin IRQ. The flag must be reset by re-programming the IRQ bit in register AUTOSTD_CTRL and then checking the detected standard status by reading registers AUTOSTD_DEM_STATUS and AUTOSTD_TIME.

IRQ1: This IRQ is enabled only in digital input mode. In case of I²S synchronisation loss, this IRQ is set to 1.

IRQ2: This IRQ is set to 1 when the device detects any change on the HP Detection pin (Headphone connection or deconnection).

IRQ3: On the STV82x8, same pins are used for both Headphone and Surround loudspeaker signal output. A change in the Headphone configuration (HP active or not active) will lead to a signal switch on those hardware pins. In order to ensure a smooth audio transition, the output is soft muted before the signal is switched. The IRQ3 is then set to 1 to advise the master processor that the signal has been switched and to request a HP/Srnd Ouput Un-Mute.

9.3 I²C Bus Expander

Pin BUS_EXP can be used to control external switchable IF SAW filters or audio switches. This pin can be directly programmed by register RESET.

10 STV82x8 Reset

All STV82x8 features are controlled via the I²C bus.

The STV82x8 can be "reset" in 2 ways:

1. By Software via the I²C bus: This clears all synchronous logic, except for the I²C bus registers.
2. By Hardware via the RESET pin: In addition to clearing all synchronous logic, the RESET input (active on the low level) resets all the I²C bus registers to the *default values* listed below.

Table 5: RESET Default Values

Function	Default Mode
Demodulation	
Auto-standard	OFF
Scanned Standards	M/N BTSC
Audio Outputs	
Automatic Mute Mode	ON
Loudspeaker Source	Demodulated Sound
Loudspeaker Volume	-40 dB, Differential Mode, Muted
Loudspeaker L/R Balance	L/R = 100%
Subwoofer	-40 dB / OFF
Headphone Source	Demodulated Sound
Headphone Automatic Detection	ON
Headphone Volume	-40 dB, Differential Mode, Muted
Headphone L/R Balance	L/R = 100%
SCART1 Output	Demodulated Sound
SCART2 Output	SCART1 Source
SCART3 Output	SCART2 Source
I²S Output (TQFP 100)	Mute

11 I²C Interface

11.1 I²C Address and Protocol

The STV82x8 I²C interface works in Slave mode and is fully compliant with I²C standards in Fast mode (maximum frequency of 400 kHz). Two pairs of I²C chip addresses are used to connect two STV82x8 chips to the same I²C serial bus. The device address pairs are defined by the polarity of the ADR_SEL pin and are listed in the following table:

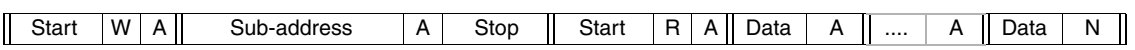
Table 6: I²C Read/Write Addresses

ADR	Write Address (W)	Read Address (R)
LOW (connected to GND1)	80h	81h
HIGH (connected to VDD1)	84h	85h

Protocol Description

- Write Protocol

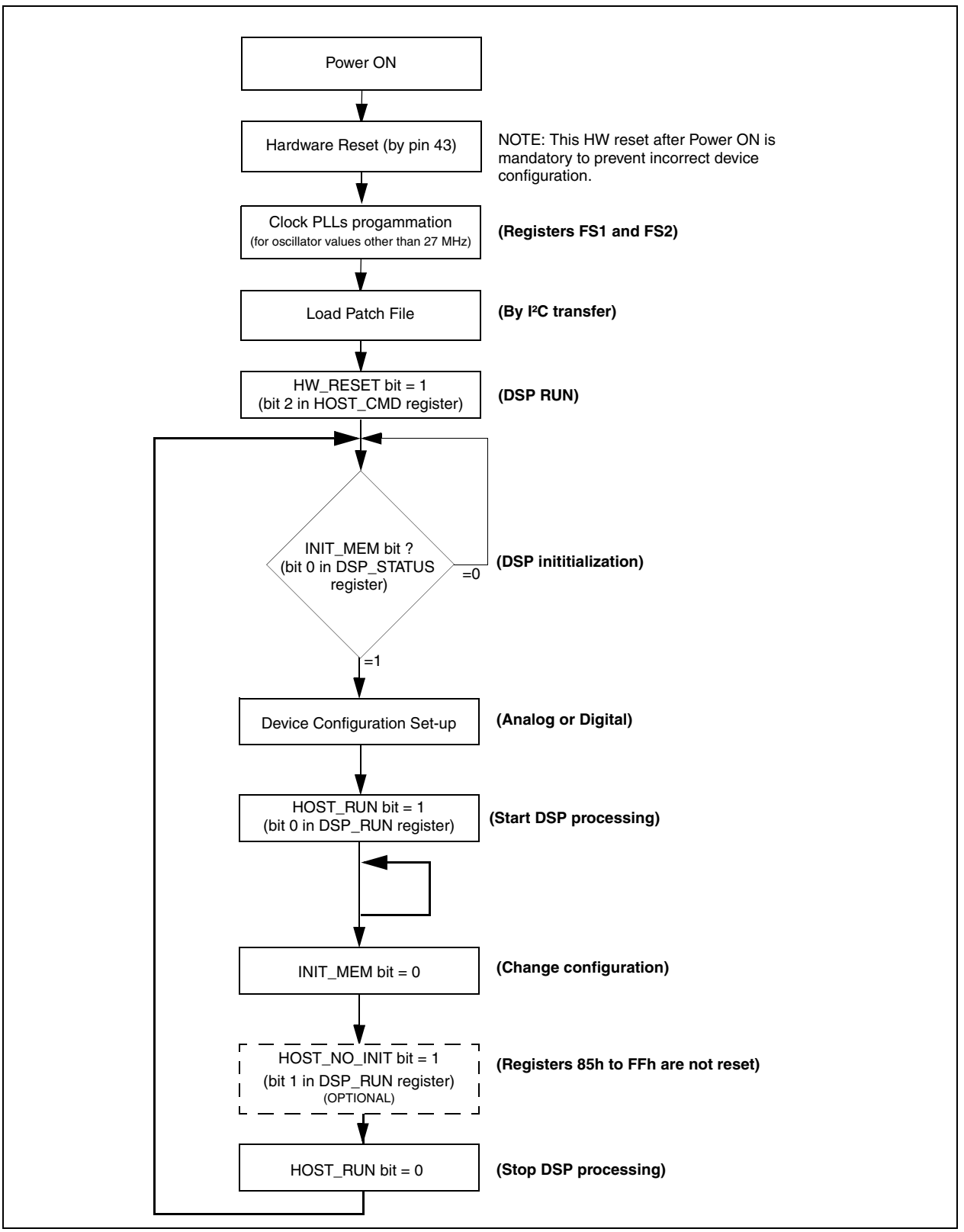
- Read Protocol



- W = Write address,
- R = Read address,
- A = Acknowledge,
- N = No acknowledge.
- Sub-address is the register address pointer; this value auto-increments for both write and read.

11.2 Start-up and Configuration Change Procedure

Figure 30: Flowchart



12 Register List

Note: The unused bits (defined as 'Reserved') in the I²C registers must be kept to zero.

The system clock registers (from address 08h to 0Bh and from address 5Ah to 5Dh) do not need to be modified if a standard 27 MHz crystal oscillator is used.

The default values of the demodulator registers (from address 0Ch to 55h) are for optimum performances and any change is not recommended, except for:

- CAROFFSET1 (22h) to compensate IF carrier frequency with an out-of-standard offset.
- Soundlevel Prescaling PRESCALE_DEMOD_MONO (94h), PRESCALE_DEMOD_STEREO (95h), PRESCALE_DEMOD_SAP (96h), PRESCALE_SCART (97h), PRESCALE_I2S0 (98H), PRESCALE_I2S1 (99H), PRESCALE_I2S2 (9AH) to equalize demodulated or external audio signal before audio processing.
- Peak detector registers PEAK_DETECTOR (9Bh), PEAK_L (9Ch), PEAK_R (9Dh), PEAK_L_R (9Eh) can be used to measure internal sound level.

Sound source selection for each audio output channel to be done using AUDIO_MATRIX1 (A2h), AUDIO_MATRIX2 (A3h) and AUDIO_MATRIX3 (A4h).

Register AUTOSTD_CTRL (8Ah) is used to select the list of mono, stereo and SAP signals to be recognized automatically.

Note: () used in reset value column means that the bit or the byte is read-only.
(S) symbol indicates that the field value is represented in signed binary format.

12.1 I²C Register Map

By default, all I²C registers controlled by Automatic Standard Recognition System (Autostandard) are forced to Read-only mode for the user. These registers and bits are shaded in Table 1.

Table 7: List of I²C Registers (Sheet 1 of 2)

Name	Ad.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IC General Control										
CUT_ID	00h	(0000 0001)	0	0	CUT_NUMBER[5:0]					
RESET	01h	0000 0000	BUS_EXP	I2S_CO_EN	I2S_DO_EN	EN_STBY	CLOCK_ DOWN	0	SOFT_ LRST1	SOFT_RST
I2S_CTRL	04h	0000 0001	I2S_PLL	SYNC_ SIGN	I2S_SRC	LOCK_TH[1:0]		LOCK_ MODE	SYNC_CST[1:0]	
I2S_STAT	05h	(0000 0000)	0	0	0	0	0	0	LR_OFF	LOCK_ FLAG
I2S_SYNC_OFFSET	06h	(0000 0000)	I^2S_SFO[7:0]							
Clocking 1										
SYS_CONFIG	07h	0000 1010	SYNC_PLL	OPEN_PLL	INPUT_FREQ[3:0]				BIT[1:0]	
FS1_DIV	08h	0001 0011	EN_PROG	0	NDIV1[1:0]		0	SDIV1[2:0]		
FS1_MD	09h	0001 0001	0	0	0	MD1[4:0]				
FS1_PE_H	0Ah	0011 0110	PE_H1[7:0]							
FS1_PE_L	0Bh	0000 0000	PE_L1[7:0]							
Demodulator										
DEMOD_CTRL	0Ch	0000 0001	0	0	0	0	0	DEMOD_MODE[2:0]		
DEMOD_STAT	0Dh	(0000 0000)	0	0	0	0	0	0	FM1_CAR	FM1_SQ
AGC_CTRL	0Eh	0001 0001	0	0	IF_SELECT	AGC_REF[2:0]			AGC_CST[1:0]	
AGC_GAIN	0Fh	(0000 0000)	0	**AGC_ERR[4:0]**					SIG_OVER	SIG_ UNDER
DC_ERR_IF	10h	(0000 0000)	DC_ERR[7:0]							
Demodulator Channel 1										
CARFQ1H	12h	0010 1110	CARFQ1[23:16]							
CARFQ1M	13h	1110 0000	CARFQ1[15:8]							
CARFQ1L	14h	0000 0000	CARFQ1[7:0]							
FIR1C0	15h	0000 0001	FIR1C0[7:0] (S)							
FIR1C1	16h	0000 0000	FIR1C1[7:0] (S)							
FIR1C2	17h	1111 1110	FIR1C2[7:0] (S)							
FIR1C3	18h	1111 1100	FIR1C3[7:0] (S)							
FIR1C4	19h	0000 0000	FIR1C4[7:0] (S)							
FIR1C5	1Ah	0000 1011	FIR1C5[7:0] (S)							
FIR1C6	1Bh	0001 1001	FIR1C6[7:0]6 (S)							
FIR1C7	1Ch	0010 0100	FIR1C7[7:0] (S)							
ACOEFF1	1Dh	0010 0010	ACOEFF1[7:0]							
BCOEFF1	1Eh	0000 1001	BCOEFF1[7:0]							
CRF1	1Fh	(0000 0000)	CRF1[7:0] (S)							
CETH1	20h	0010 0000	CETH1[7:0]							
SQTH1	21h	0011 1100	SQTH1[7:0]							
CAROFFSET1	22h	0000 0000	CAROFFSET1[7:0] (S)							
CHANNEL_GAIN	23h	0000 0010	0	0	0	0	0	0	CH_GAIN[1:0]	

Table 7: List of I²C Registers (Sheet 2 of 2)

Name	Ad.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BTSC Stereo and SAP										
STEREO_CONF	43h	00111000	LOCK_TH_STE[7:4]				LOOP_GAIN[1:0]		FREQ_PIL	RESET
STEREO_FSM_CONF	44h	00001110	0	0	BYPASS	FSM_OFF	GAIN_INI[2:0]			STE_DEM
STEREO_LEVEL_H	45h	00100000	STE_LEV_H[7:0]							
STEREO_LEVEL_L	46h	00010000	STE_LEV_L[7:0]							
SAP_CONF	47h	00000000	0	0	0	0	0	0	0	SAP_SEL
SAP_LEVEL_H	48h	00100000	SAP_LEV_H[7:0]							
SAP_LEVEL_L	49h	00010000	SAP_LEV_L[7:0]							
STE_CAR_LEVEL	4Ah	(00000000)	STE_CAR_LEV[7:0]							
STE_PLL_STATUS	4Bh	(00000000)	0	0	LOOP_GAIN[3:0]			OVER	LOCK_DET	STE_DET
STEREO_SAP_STATUS	4Ch	(00000000)	0	OVER	LOCK_DET	STE_DET	0	0	SQ_DET	SAP_DET
PLL_P_GAIN	4Dh	01101100	PLL_P_GAIN[7:0]							
PLL_I_GAIN	4Eh	0000011	0	0	0	0	PLL_I_GAIN[3:0]			
SAP_SQ_TH	4Fh	00110000	SAP_SQ_TH[7:0]							
Analog and I2S Out Control										
I2S_ADC_CTRL	56h	0000 1000	I2S_DATA0_CTRL			0	ADC_ POWER_UP	ADC_INPUT_SEL[2:0]		
SCART1_2_OUTPUT_CTRL	57h	1010 1000	SC2_MUTE	SC2_OUTPUT_SEL[2:0]			SC1_MUTE	SC1_OUTPUT_SEL[2:0]		
SCART3_OUTPUT_CTRL	58h	0000 1011	0	0	0	0	SC3_MUTE	SC3_OUTPUT_SEL[2:0]		
I2SO_DATA_CTRL	59h	0000 0000	0	I2SO_DATA1_CTRL			0	I2SO_DATA0_CTRL		
Clocking 2										
FS2_DIV	5Ah	0001 0001	0	NDIV2[1:0]			0	SDIV2[2:0]		
FS2_MD	5Bh	0001 0001	0	0	0	MD2[4:0]				
FS2_PE_H	5Ch	0101 1100	PE_H2[7:0]							
FS2_PE_L	5Dh	0010 1001	PE_L2[7:0]							

12.2 Software Registers

Table 8: List of I²C Registers (Sheet 1 of 5)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DSP Control										
HOST_CMD	80h	0000 0000	IT_IN_DSP	0	0	0	0	HW_RESET	PATCH_WRITE_ENABLE	EMUL_SW
IRQ_STATUS	81h	0000 0000	IRQ7	IRQ6	IRQ5 (HP/Srnd unmute ready)	IRQ4 (HP detected)	IRQ3 (I2S SRC input freq change)	IRQ2 (I2S sync found)	IRQ1 (I2S sync lost)	IRQ0 (AutoStandard)
FW_VERSION	82h	(0000 0001)	SOFT_VERSION[7:0]							
ONCHIP_ALGO	83h	(0000 0000)	0	0	PROLOGIC_TYPE	MULTI_I2S_IN	TRUBASS	TRUSURROUND	PROLOGIC	MULTICHANNEL_OUT
DSP_STATUS	84h	0000 0000	0	0	0	0	0	0	0	INIT_MEM
DSP_RUN	85h	0000 0000	0	TEST_MODE_INPUT	TEST_MODE		INPUT_CONFIG		REGISTERS_RESET	HOST_RUN
I2S_IN_CONFIG	86h	1000 1110	LOCK_MODE_EN	RESET_I2S	0	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE
I2S_IN_SHIFT_RIGHT	87h	0000 1000	0	0	0	SHIFT_RIGHT_RANGE				
I2S_IN_MASK	88h	0001 1111	0	0	0	WORD_MASK				
I2S_IN_STATUS	89h	1000 0(000)	AUTO_SRC_SYNC	ENABLE_IRQ_SRC_FREQ_CHANGE	ENABLE_IRQ_SYNC_FOUND	ENABLE_IRQ_SYNC_LOST	0	I2S_INPUT_FREQ		
Automatic Standard Detection										
AUTOSTD_CTRL	8Ah	0000 0000	SIHGLESHOT	MONO_SAP_MATRIX_CTRL	FORCE_SQ_SAP	FORCE_SQ_MONO	AUTO_MUTE	SAP_CHECK	STEREO_CHECK	MONO_CHECK
AUTOSTD_TIME	8Bh	0000 1010	0	0	0	STEREO_TIME			FM_TIME	
AUTOSTD_STATUS	8Ch	(0000 0000)	0	0	0	0	SAP_OK	STEREO_OK	MONO_OK	AUTOSTD_ON
AUTOSTD_DEM_STATUS	8Dh	(0000 0000)	0	OVERFLOW	LCK_DET	ST_DET	SAP_SQ	SAP_DET	FM1_CAR	FM1_SQ
DMA_FORCE_OFF	8Eh	0000 0000	0	0	0	*ADC*	*I2S2*	*I2S1*	*I2S0*	*DEMOD*
I2S_IN_DELAY_CONFIG	8Fh	0000 0111	0	0	SYNC	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE
Demodulator										
BTSC_FINE_PRESCALE_ST	90h	0000 0000	BTSC_FINE_PRESCALE_ST[7:0] (S)							
BTSC_FINE_PRESCALE_SAP	91h	0000 0000	BTSC_FINE_PRESCALE_SAP[7:0] (S)							
BTSC_CONTROL	92h	0010 0000	FINE_PRESCAL_SELECT_SAP	DBX_DEMATRIX		DBX_ON	DEEMPHASIS_CH1		DEEMPHASIS_CH0	
DCREMOVAL	93h	0011 0111	0	0	DBX_FILTER_SELECT	DEEMPHASIS_FILTER_SELECT	0	DC_DEMOD_POST_ON	DC_DEMOD_PRE_ON	DC_SCART_ON
Audio Preprocessing & Selection										
PRESCALE_DEMOD_MONO	94h	0000 0000	PRESCALE_DEMOD_SELECT_SAP	PRESCALE_DEMOD_MONO[6:0] (S)						
PRESCALE_DEMOD_STEREO	95h	0000 0000	0	PRESCALE_DEMOD_STEREO[6:0] (S)						
PRESCALE_DEMOD_SAP	96h	0000 0000	0	PRESCALE_DEMOD_SAP[6:0] (S)						
PRESCALE_SCART	97h	0000 0000	0	PRESCALE_SCART[6:0] (S)						

Table 8: List of I²C Registers (Sheet 2 of 5)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRESCALE_I2S0	98h	0000 0000	0	PRESCALE_I2S0[6:0] (S)						
PRESCALE_I2S1	99h	0000 0000	0	PRESCALE_I2S1[6:0] (S)						
PRESCALE_I2S2	9Ah	0000 0000	0	PRESCALE_I2S2[6:0] (S)						
PEAK_DETECTOR	9Bh	0000 0000	0	PEAK_L_R_RANGE[2:0]			PEAK_DET_INPUT[2:0]			PEAK_DETECTOR_ON
PEAK_L	9Ch	0(000 0000)	OVERLOAD_L	PEAK_L[6:0]						
PEAK_R	9Dh	0(000 0000)	OVERLOAD_R	PEAK_R[6:0]						
PEAK_L_R	9Eh	0(000 0000)	OVERLOAD_L_R	PEAK_L_R[6:0						

Matrixing

DOWNMIX_MODE	9Fh	0111 1111	LTRT_OUT_MODE	MIX_OUT_MODE[2:0]			LFE_IN	MIX_IN_MODE[2:0]		
DOWNMIX_DUAL_MODE	A0h	0000 0000	0	0	0	DUAL_ON	LS_DUAL_SELECT[1:0]		LTRT_DUAL_SELECT[1:0]	
DOWNMIX_CONFIG	A1h	0000 0001	0	0	SRND_FACTOR[1:0]		CENTER_FACTOR[1:0]		LR_UPMIX	NORMALIZE
AUDIO_MATRIX1	A2h	0001 0010	0	0	HP_OUT[2:0]			LS_OUT[2:0]		
AUDIO_MATRIX2	A3h	0000 0010	0	0	SCART2_OUT[2:0]			SCART1_OUT[2:0]		
AUDIO_MATRIX3	A4h	0001 0000	0	0	SPDIF_OUT[2:0]			DELAY_OUT[2:0]		
CHANNEL_MATRIX_LS	A5h	0000 0010	AUTOSTD_CONTROL_LS	AUTOSTD_CONTROL_SPDIF	0	0	0	CM_MATRIX_LS[2:0]		
CHANNEL_MATRIX_HP	A6h	0000 0000	AUTOSTD_CONTROL_HP	CM_SOURCE_HP[2:0]		CM_POSTION_HP[2:0]		CM_MATRIX_HP[2:0]		
CHANNEL_MATRIX_SCART1	A7h	0000 0000	AUTOSTD_CONTROL_SCART1	CM_SOURCE_SCART1[2:0]		CM_POSTION_SCART1[2:0]		CM_MATRIX_SCART1[2:0]		
CHANNEL_MATRIX_SCART2	A8h	0000 0000	AUTOSTD_CONTROL_SCART2	CM_SOURCE_SCART2[2:0]		CM_POSTION_SCART2[2:0]		CM_MATRIX_SCART2[2:0]		
CHANNEL_MATRIX_SPDIF	A9h	0000 0000	CM_SOURCE_SPDIF[3:0]			CM_POSTION_SPDIF[2:0]		CM_MATRIX_SPDIF[2:0]		
DEMOD_DC_LEVEL	AAh	(0000 0000)	DEMOD_DC_LEVEL[7:0] (S)							
	ABh	0000 0000	0	0	0	0	0	0	0	0
	ACh	0000 0000	0	0	0	0	0	0	0	0

Audio Processing

AV_DELAY_CONFIG	ADh	0000 0000	0	0	0	0	0	0	DOLBY_DELAY_ON	AV_DELAY_ON
AV_DELAY_TIME_LS	AEh	0000 0000	AV_DELAY_TIME_LS[7:0]							
AV_DELAY_TIME_HP	AFh	0000 0000	AV_DELAY_TIME_HP[7:0]							
PROLOGIC2_CONTROL	B0h	0111 0110	PL2_LFE	PL2_OUTPUT_DOWNMIX[2:0]			PL2_MODES[2:0]			PL2_ACTIVE
PROLOGIC2_CONFIG	B1h	0000 0000	0	0	0	PL2_SRND_FILTER[1:0]		PL2_RS_POLARITY	PL2_PANORAMA	PL2_AUTO BALANCE
PROLOGIC2_DIMENSION	B2h	0000 0000	0	PL2_C_WIDTH[2:0]			0	PL2_DIMENSION[2:0]		
PROLOGIC2_LEVEL	B3h	0000 0011	PL2_LEVEL[7:0]							
NOISE_GENERATOR	B4h	0000 0000	10_DB_ATTENUATE	SRIGHT_NOISE	SLEFT_NOISE	SUB_NOISE	CENTER_NOISE	RIGHT_NOISE	LEFT_NOISE	NOISE_ON
PCM_SRND_DELAY	B5h	0000 0000	0	0	0	DOLBY_DELAY_SRND[4:0]				
PCM_CENTER_DELAY	B6h	0000 0000	0	0	0	0	DOLBY_DELAY_CENTER[3:0]			

Table 8: List of I²C Registers (Sheet 3 of 5)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRUSRND_CONTROL	B7h	0000 1000	DIALOG_CLARITY_ON	HEADPHONE_ON	TRUSRND_INPUT_MODE[3:0]				TRUSRND_BYPASS	TRUSRND_ON
TRUSRND_DC_ELEVATION	B8h	0000 1100	TRUSRND_DC_ELEVATION[7:0]							
TRUSRND_INPUT_GAIN	B9h	0000 0000	TRUSRND_INPUT_GAIN[7:0]							
TRUBASS_LS_CONTROL	BAh	0000 0110	0	0	0	0	TRUBASS_LS_SIZE[2:0]			TRUBASS_LS_ON
TRUBASS_LS_LEVEL	BBh	00001 1001	TRUBASS_LS_LEVEL[7:0]							
TRUBASS_HP_CONTROL	BCh	0000 0110	SRS_TSXT_GAIN_ON	0	0	0	TRUBASS_HP_SIZE[2:0]			TRUBASS_HP_ON
TRUBASS_HP_LEVEL	BDh	0000 1001	TRUBASS_HP_LEVEL[7:0]							
SVC_LS_CONTROL	BEh	0000 0010	0	0	0	0	SVC_LS_INPUT[1:0]		SVC_LS_AMP	SVC_LS_ON
SVC_LS_TIME_TH	BFh	0000 0000	SVC_LS_TIME[2:0]			SVC_LS_THRESHOLD[4:0]				
SVC_LS_GAIN	C0h	0000 1111	0	0	SVC_LS_MAKE_UP_GAIN[5:0]					
SVC_HP_CONTROL	C1h	0000 0010	0	0	0	0	0	0	SVC_LHP_AMP	SVC_HP_ON
SVC_HP_TIME_TH	C2h	0000 0000	SVC_HP_TIME[2:0]			SVC_HP_THRESHOLD[4:0]				
SVC_HP_GAIN	C3h	0000 1111	0	0	SVC_HP_MAKE_UP_GAIN[5:0]					
WIDESRND_CONTROL	C4h	0000 0100	0	0	0	0	0	WIDESRND_STEREO	WIDESRND_MODE	WIDESRND_ON
WIDESRND_FREQ	C5h	0001 0101	0	0	WIDESRND_BASS[1:0]		WIDESRND_MEDIUM[1:0]		WIDESRND_TREBLE[1:0]	
WIDESRND_LEVEL	C6h	1000 0000	WIDESRND_GAIN[7:0]							
OMNISRND_CONTROL	C7h	0000 1100	ST_VOICE[1:0]		SRND_PHASE_INV	OMNISRND_INPUT_MODE[3:0]				OMNISRND_ON
DYNAMIC_BASS_LS	C8h	0110 0010	LS_BASS_LEVEL[4:0]					LS_BASS_FREQ[1:0]		LS_DYN_BASS_ON
DYNAMIC_BASS_HP	C9h	0110 0010	HP_BASS_LEVEL[4:0]					HP_BASS_FREQ[1:0]		HP_DYN_BASS_ON
BASS_ENHANCE_LS	CAh	0000 0000	0	0	LS_BASS_ENHANCE_HP_FILTER	LS_BASS_ENHANCE_SCALE[2:0]			LS_BASS_ENHANCE_CUTOFF	LS_BASS_ENHANCE_ON
	CBh	0000 0000	0	0	0	0	0	0	0	0
EQ_BT_CONTROL	CCh	0000 0000	0	0	0	0	0	HP_BT_ON	LS_EQ_BT_SW	LS_EQ_ON
LS_EQ_BAND1	CDh	0000 0000	EQ_BAND1[7:0] (S)							
LS_EQ_BAND2	CEh	0000 0000	EQ_BAND2[7:0] (S)							
LS_EQ_BAND3	CFh	0000 0000	EQ_BAND3[7:0] (S)							
LS_EQ_BAND4	D0h	0000 0000	EQ_BAND4[7:0] (S)							
LS_EQ_BAND5	D1h	0000 0000	EQ_BAND5[7:0] (S)							
LS_BASS_GAIN	D2h	0000 0000	LS_BASS[7:0] (S)							
LS_TREBLE_GAIN	D3h	0000 0000	LS_TREBLE[7:0] (S)							
HP_BASS_GAIN	D4h	0000 0000	HP_BASS[7:0] (S)							
HP_TREBLE_GAIN	D5h	0000 0000	HP_TREBLE[7:0] (S)							
OUTPUT_BASS_MNGT	D6h	1000 0000	BASS_MANAGE_ON	ST_LFE_ADD	DOLBY_PROLOGIC	SUB_ACTIVE	GAIN_SWITCH	OCFG_NUM[2:0]		
LS_LOUDNESS	D7h	0000 0100	0	LS_LOUD_THRESHOLD[2:0]			LS_LOUD_GAIN_HR[2:0]			LS_LOUD_ON
HP_LOUDNESS	D8h	0000 0100	0	HP_LOUD_THRESHOLD[2:0]			HP_LOUD_GAIN_HR[2:0]			HP_LOUD_ON

Volume

Table 8: List of I²C Registers (Sheet 4 of 5)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VOLUME_MODES	D9h	1101 1111	ANTCLIP_HP_VOL_CLAMP	ANTICLIP_LS_VOL_CLAMP	0	SCART2_VOLUME_MODE	SCART1_VOLUME_MODE	HP_VOLUME_MODE	SRND_VOLUME_MODE	LS_VOLUME_MODE
LS_L_VOLUME_MSB	DAh	1001 1000	LS_L_VOLUME_MSB[7:0]							
LS_L_VOLUME_LSB	DBh	0000 0000	0	0	0	0	0	0	LS_L_VOLUME_LSB[1:0]	
LS_R_VOLUME_MSB	DCh	0000 0000	LS_R_VOLUME_MSB[7:0]							
LS_R_VOLUME_LSB	DDh	0000 0000	0	0	0	0	0	0	LS_R_VOLUME_LSB[1:0]	
LS_C_VOLUME_MSB	DEh	1001 1000	LS_C_VOLUME_MSB[7:0]							
LS_C_VOLUME_LSB	DFh	0000 0000	0	0	0	0	0	0	LS_C_VOLUME_LSB[1:0]	
LS_SUB_VOLUME_MSB	E0h	1001 1000	LS_SUB_VOLUME_MSB[7:0]							
LS_SUB_VOLUME_LSB	E1h	0000 0000	0	0	0	0	0	0	LS_SUB_VOLUME_LSB[1:0]	
LS_SL_VOLUME_MSB	E2h	1001 1000	LS_SL_VOLUME_MSB[7:0]							
LS_SL_VOLUME_LSB	E3h	0000 0000	0	0	0	0	0	0	LS_SL_VOLUME_LSB[1:0]	
LS_SR_VOLUME_MSB	E4h	0000 0000	LS_SR_VOLUME_MSB[7:0]							
LS_SR_VOLUME_LSB	E5h	0000 0000	0	0	0	0	0	0	LS_SR_VOLUME_LSB[1:0]	
LS_MASTER_VOLUME_MSB	E6h	1110 1000	LS_MASTER_VOLUME_MSB[7:0]							
LS_MASTER_VOLUME_LSB	E7h	0000 0000	0	0	0	0	0	0	LS_MASTER_VOLUME_LSB[1:0]	
HP_L_VOLUME_MSB	E8h	1001 1000	HP_L_VOLUME_MSB[7:0]							
HP_L_VOLUME_LSB	E9h	0000 0000	0	0	0	0	0	0	HP_L_VOLUME_LSB[1:0]	
HP_R_VOLUME_MSB	EAh	0000 0000	HP_R_VOLUME_MSB[7:0]							
HP_R_VOLUME_LSB	EBh	0000 0000	0	0	0	0	0	0	HP_R_VOLUME_LSB[1:0]	
AUX_VOLUME_INDEX	ECh	0000 0001	0	0	0	0	0	0	AUX_VOLUME_SELECT[1:0]	
AUX_L_VOLUME_MSB	EDh	1101 1101	AUX_L_VOLUME_MSB[7:0]							
AUX_L_VOLUME_LSB	EEh	0000 0000	0	0	0	0	0	0	AUX_L_VOLUME_LSB[1:0]	
AUX_R_VOLUME_MSB	EFh	0000 0000	AUX_R_VOLUME_MSB[7:0]							
AUX_R_VOLUME_LSB	F0h	0000 0000	0	0	0	0	0	0	AUX_R_VOLUME_LSB[1:0]	
Mute										
MUTE_SOFTWARE	F1h	1111 1111	HP_D_MUTE	SPDIF_D_MUTE	SCART2_D_MUTE	SCART1_D_MUTE	SRND_D_MUTE	SUB_D_MUTE	C_D_MUTE	LS_D_MUTE
Beeper										
BEEPER_ON	F2h	0000 0000	0	0	0	0	0	BEEPER_SOUND_SELECT[1:0]		BEEPER_ON
BEEPER_MODE	F3h	0100 0011	BEEPER_DECAY[1:0]			BEEPER_DURATION[1:0]		BEEPER_CONTINUOUS	BEEPER_PATH[1:0]	
BEEPER_FREQ_VOL	F4h	0111 0110	BEEPER_FREQ[2:0]			BEEPER_VOLUME[4:0]				
SPDIF Out Configuration										
SPDIF_OUT_CHANNEL_STATUS	F5h	0000 0010	0	0	0	0	0	SPDIF_COPYRIGHT	SPDIF_NO_PCM	SPDIF_CONSUMER_PRO
Headphone Configuration										
HP_SCART2_CONFIG	F6h	0000 0010	0	KARAOKE_MIX	SCART2_OUT_SELECT		HP_FORCE	HP_LS_MUTE	HP_DET_ACTIVE	HP_DETECTED

Table 8: List of I²C Registers (Sheet 5 of 5)

Name	Addr.	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC Control										
DAC_CONTROL	F7h	0001 1111	0	0	SPDIF_MUX	DAC_SCART_MUTE	DAC_SHP_MUTE	DAC_CSUB_MUTE	DAC_LSLR_MUTE	POWER_UP
DAC_SW_CHANNELS	F8h	0000 0000	C_SUB_SW[1:0]		SUR_HP_SW[1:0]		SCART_SW[1:0]		SPDIF_SW[1:0]	
SPDIF_SW_CHANNELS	F9h	0000 0000	0	0	0	0	DELAY_SW[1:0]		L_R_SW[1:0]	
AutoStandard Coefficients Settings										
AUTOSTD_FSM	FAh	0000 0000	0	0	0	0	FSM_STATE			
AUTOSTD_COEFF_CTRL	FBh	0000 0001	0	0	0	0	0	0	AUTOSTD_COEFF_CTRL[1:0]	
AUTOSTD_COEFF_INDEX_MSB	FCh	0000 0000	0	0	0	0	0	0	0	AUTOSTD_COEFF_INDEX_MSB
AUTOSTD_COEFF_INDEX_LSB	FDh	0000 0000	AUTOSTD_COEFF_INDEX_LSB[7:0]							
AUTOSTD_COEFF_VALUE	FEh	0000 0000	AUTOSTD_COEFF_VALUE[7:0]							
PATCH_VERSION	FFh	0000 0000	PATCH_VERSION[7:0]							

12.3 STV82x8 General Control Registers

CUT_ID — Version Identification

Address: 00h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	CUT_NUMBER[5:0]					

Bit Name	Reset	Function
Bits[7:6]	00	Reserved
CUT_NUMBER[5:0]	000001	Dice Version Identification

RESET — Software Reset Register

Address: 01h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BUS_EXP	I2S_CO_EN	I2S_DO_EN	EN_STBY	CLOCK_DOWN	0	SOFT_LRST1	SOFT_RST

Description

The built-in Automatic Standard Recognition System (Autostandard) can be disabled. In this case, the Software Reset function (bits SOFT_LRST1 and SOFT_LRST2) can be used to implement the

Automatic Standard Recognition by I²C Software. This is not required if the built-in Automatic Standard Recognition System function is used (default).

Bit Name	Reset	Function
BUS_EXP	0	Static control by I2C of hardware pin BUS_EXP
I²2S_CO_EN	0	0 = I²2S Input (I2S_SCK , I2S_LR_CLK, I2S_PCM_CLK in input mode) 1 = I²2S Output (I2S_SCK , I2S_LR_CLK, I2S_PCM_CLK in output mode)
I²2S_DO_EN	0	0 = I²2S Input (I2S_DATA0 in input mode) 1 = I²2S Output (I2S_DATA0 in output mode)
EN_STBY	0	**Standby mode enabling** 0: Normal mode 1: To lock the digital signals before to settle the device in standby mode
CLOCK_DOWN	0	clock down of the dsp, decoder.
Bit [2]	0	Reserved
SOFT_LRST1	0	Softreset (active high) of Decoder..
SOFTR_RST	0	General softreset (active high) to reset all hardware registers except for I²2C data.

I2S_CTRL I²S Synchronization Control Register

Address: 04h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2S_PLL	SYNC_SIGN	I2S_SRC	LOCK_TH[1:0]		LOCK_MODE	SYNC_CST[1:0]	

Bit Name	Reset	Function
I2S_PLL	0	Selects the i2s source for the synchronization with the synthesizer (at 48KHz only) 0: I2S_LR_CLK selected 1: I2SA_LR_CLK selected
SYNC_SIGN	0	Reverse the sign of the loop - To be used in case of gain inversion of the Frequency Synthesizer
I2S_SRC	0	Selects the i2s source for the src 0: I2S_LR_CLK selected 1: I2SA_LR_CLK selected
LOCK_TH[1:0]	00	**Lock Detector Threshold Programming** 00: ±1 CLK period error of accumulation 01: ±2 CLK period error of accumulation 10: ±4 CLK period error of accumulation 11: ±8 CLK period error of accumulation
LOCK_MODE	0	**Lock Detector Mode** 0: Lock when accumulation error within lock threshold and LR detected (period counter not saturated) 1: Lock when only accumulation error within lock threshold. Don't care of the LR detection
SYNC_CST[1:0]	00	**Synchronization Time Constant** Defines the measurement period of LR 00: Half period measured (lowest accuracy) 01: One full period measured 10: Two full periods measured 11: Four full periods measured (highest accuracy)

I2S_STAT I²S Synchronization Status Register

Address: 05h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LR_OFF	LOCK_FLAG

Bit Name	Reset	Function
Bits[7:2]	0	Reserved.
LR_OFF	0	**LR Signal Detection** 0: LR signal detected and correct 1: Missing LR pulses detected
LOCK_FLAG	0	Lock Flag allowing unmute of Audio Output

I2S_SYNC_OFFSET I²S Synchronization Offset Frequency Register

Address: 06h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2S_SFO[7:0]							

Bit Name	Reset	Function
I2S_SFO[7:0]	0000 0000	I²S synchronization frequency offset (±450 ppm full scale)

12.4 Clocking 1

A low-jitter PLL Clock is integrated and can be fully reprogrammed using the registers described below. By default, the programming is defined for a 27-MHz crystal oscillator, which is the frequency recommended for reducing potential RF interference in the application. However, if necessary, the PLL Clock can be re-programmed for other crystal oscillator frequencies within a range from 23 to 30 MHz. Other crystal frequencies can be programmed on your demand.

Note: A Crystal Frequency change is compatible with other default I²C programming including the built-in Automatic Standard Recognition System.

SYS_CONFIG System Configuration Control Register

Address: 07h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC_PLL	OPEN_PLL	INPUT_FREQ[3:0]				BIT[1:0]	

Bit Name	Reset	Function
SYNC_PLL	0	**Status of the loop wyth the synthesizer** 0: Open 1: Closed
OPEN_PLL	0	**Force the loop with the synthesizer to be open** 0: No Action 1: Loop Open
INPUT_FREQ[3:0]	0010	**I2S Input frequency** 0010: 48 kHz
BIT[1:0]	10	Reserved

FS1_DIV FS1 I/O Divider Programming Register

Address: 08h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EN_PROG	0	NDIV1[1:0]		0	SDIV1[2:0]		

Bit Name	Reset	Function
EN_PROG	0	FS1 programmation enable 0: FS1 I2C registers programmation ignored by system - FS1 pre-programmed automatically by SYS-CONFIG register (normal use with standard oscillator of 27 MHz) 1: FS1 I2C registers programmation used by system - FS1 pre-programmation by SYS-CONFIG desactivated (to be used in case of no standard oscillator, other than 27 MHz)
Bit 6	0	Reserved.
NDIV1[1:0]	01	FS1 Input clock divider selection
Bit 3	0	Reserved.
SDIV1[2:0]	011	FS1 Output clock divider selection

FS1_MD FS1 Coarse Selection Register

Address: 09h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	MD1[4:0]				

Bit Name	Reset	Function
Bits[7:5]	000	Reserved.
MD1[4:0]	10001	FS1 Coarse Selection

FS1_PE_H FS1 Fine Selection Register (MSBs)

Address: 0Ah

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PE_H1[7:0]							

Bit Name	Reset	Function
PE_H1[7:0]	0011 0110	FS1 Fine Selection (MSBs)

FS1_PE_L FS1 Fine Selection Register (LSBs)

Address: 0Bh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PE_L1[7:0]							

Bit Name	Reset	Function
PE_L1[7:0]	0000 0000	FS1 Fine Selection (LSBs)

12.5 Demodulator

DEMOD_CTRL Demodulator Control Register

Address: 0Ch

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	DEMOD_MODE[2:0]		

Bit Name	Reset	Function
Bits [7:3]	00000	Reserved
DEMOD_MODE[2:0]	001	**Demodulator Mode Select** Demod FM 000: Normal 001: Wide other configuration: Reserved

DEMOD_STAT Demodulator Detection Status Register

Address: 0Dh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0				FM1_CAR	FM1_SQ

Bit Name	Reset	Function
Bits [7:2]	000	Reserved.
FM1_CAR	0	**Channel 1 FM Carrier Detector Flag** 0: Not detected 1: Detected
FM1_SQ	0	**Channel 1 FM Squelch Detector Flag** 0: Not detected 1: Detected

Note: These registers allow direct access to the demodulator signal detectors.

AGC_CTRL IF AGC Control Register

Address: 0Eh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	IF_SELECT	AGC_REF[2:0]			AGC_CST[1:0]	

Bit Name	Reset	Function
Bits[7:5]	00	Reserved.
IF_SELECT	0	Selection of the IF input. 0: IF input SIF 1 1: IF input SIF 2
AGC_REF[2:0]	100	This bitfield is used to defines the clipping level which adjusts the allowable proportion of samples at the input of the ADC which will be clipped. The AGC tries to maximize the use of the full scale range of the ADC. The default setting gives a ratio of 1/256. 000: 1/16 (Single carrier) — 100: 1/256 (Default) 001: 1/32 — 101: 1/512 010: 1/64 — 110: 1/1024 011: 1/128 — 111: 1/2048 (Multiple carriers)
AGC_CST[1:0]	01	**AGC Time Constant** This is the time constant between each step of 1.5 dB by the AGC. 00 1.33 01 2.66 10 5.33 11 10.66

AGC_GAIN IF AGC Control and Status Register

Address: 0Fh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	AGC_ERR[4:0]					SIG_OVER	SIG_UNDER

Bit Name	Reset	Function
Bit 7	0	Reserved.
AGC_ERR[4:0]	00000	**Amplifier Gain Control** This is the Gain Control value of AGC. There are 20 steps of +1.5 dB (see Note below). 00000: Gain-min 10100: Gain-min + 30 dB 11111: Gain-min + 30 dB
SIG_OVER	0	**AGC Input SIgnal Upper Threshold** 0: Normal signal 1: Signal too large and AGC is overloaded
SIG_UNDER	0	**AGC Input SIgnal Lower Threshold** 0: Normal signal 1: Signal too small and AGC is underloaded When the AGC is in Automatic mode (AGC_CMD = 0), bits SIG_OVER and SIG_UNDER indicate if the input signal is too small/large and the AGC is under/overloaded. This is useful when setting the STV82x7 SIF input level.

*Note: When **AGC_CMD = 0**, **AGC_ERR[4:0]** can be read -- indicating the input level. It can also be written to -- presetting the AGC level which will then adjust itself to the final value.*

*When **AGC_CMD = 1**, the AGC is off and writing to **AGC_ERR[4:0]** directly controls the AGC amplifier gain. Reading AGC_ERR just confirms the fixed value.*

DC_ERR_IF DC Offset Status for IF ADC

Address: 10h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DC_ERR[7:0]							

Bit Name	Reset	Function
DC_ERR[7:0]	00000000	DC offset error of IF ADC output

12.6 Demodulator Channel 1

CARFQ1H, CARFQ1M, CARFQ1L Channel 1 Carrier DCO Frequency

Address: 12h to 14h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CARFQ1[23:16], CARFQ1[15:8], CARFQ1[7:0]							

Bit Name	Reset	Function
CARFQ1[23:16]	00101110	Channel 1 DCO Carrier Frequency (8 MSBs)
CARFQ1[15:8]	11100000	Channel 1 DCO Carrier Frequency
CARFQ1[7:0]	00000000	Channel 1 DCO Carrier Frequency (8 LSBs), see Table 2.

Table 9: Mono Carrier Frequencies by System

System	Mono Carrier Freq. (MHz)	CARFQ1[23:0] (dec)	CARFQ1[23:0]
M/N	4.5	3072000	2EE000h

Note: Carrier Freq: CARFQ1(dec).f_S / 2^{24} with f_S = 24.576 MHz (crystal oscillator frequency independent)

FIR1C[0:7] Channel 1 FIR Coefficients

Address: 15h to 1Ch

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIR1C0[7:0] to FIR1C7[7:0]							

Bitfield	Description					
						(reset state)
	FM 27 kHz	FM 50 kHz	FM 200 kHz	FM 350 kHz	FM 500 kHz	BTSC
FIR1C0[7:0]	FFh	00h	00h	02h	01h	01h
FIR1C1[7:0]	FEh	FEh	01h	01h	00h	00h
FIR1C2[7:0]	FEh	FCh	01h	FCh	04h	FEh
FIR1C3[7:0]	00h	FDh	FCh	03h	FAh	FCh
FIR1C4[7:0]	06h	02h	08h	04h	05h	00h
FIR1C5[7:0]	0Eh	0Dh	F6h	F2h	00h	0Bh
FIR1C6[7:0]	16h	18h	F8h	06h	F2h	19h

Bitfield	Description					
						(reset state)
	FM 27 kHz	FM 50 kHz	FM 200 kHz	FM 350 kHz	FM 500 kHz	BTSC
FIR1C7[7:0]	1Bh	1Fh	4Ah	43h	4Dh	24h

ACOEFF1 Channel 1 Baseband PLL Loop Filter Proportional Coefficient

Address: 1Dh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACOEFF1[7:0]							

Bit Name	Reset	Function
ACOEFF1[7:0]	00100010	Used to program the Proportional Coefficient of the baseband PLL loop filter (Channel 1) Defines the damping factor of the loop. For values, refer to Table 3.

BCOEFF1 Channel 1 Baseband PLL Loop Filter Integral Coefficient & DCO Gain

Address: 1Eh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BCOEFF1[7:0]							

Bit Name	Reset	Function
BCOEFF1[7:0]	00001001	Used to program the Integral Coefficient of the baseband PLL loop filter and DCO gain Defines the bandwidth of the loop. For values, refer to Table 3.

Table 10: Baseband PLL Loop Filter Adjustment (FM Mode)

FM Mode	Small	Standard	Medium	Wide*	BTSC
ACOEFF	10h	22h	2Ch	2Ch	22h
BCOEFF	1Ah	12h	0Ah	0Ah	09h
FM_DEV max (kHz)	62.5	125	250	500	500
DCO Range (kHz)	96	192	384	768	768

(*) Refer to DEMOD_CTRL (DEMOD_MODE[2:0])

CRF1 Channel 1 Baseband PLL Demodulator Offset

Address: 1Fh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRF1[7:0]							

Bit Name	Reset	Function
CRF1[7:0]	(00000000)	**Channel 1 Carrier Recovery Frequency** Displays the instantaneous frequency offset of the Channel 1 Baseband PLL Demodulator.

CETH1 Channel 1 FM Carrier Level Threshold

Address: 20h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CETH1[7:0]							

Bit Name	Reset	Function
CETH1[7:0]	00100000	This register is used to compare the carrier level in the channel and the threshold value. This level is measured after the channel filter and is relative to the full scale reference level (0 dB). This is used as part of the validation of an FM signal, if the carrier level is below the threshold, the signal is considered to be non-valid. Recommended value is 10h. CETH — Threshold (dB) — CETH — Threshold (dB) FFh — -6 — 10h — -32 (Recommended Value) 80h — -12 — 08h — -38 40h — -18 — 00h — OFF (all carrier levels are accepted) 20h — -24 (Default)

SQTH1 Channel 1 FM Squelch Threshold Register

Address: 21h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SQTH1[7:0]							

Bit Name	Reset	Function
SQTH1[7:0]	00111100	The squelch detector measures the level of high frequency noise (> 40 kHz) and compares it to the threshold level (SQTH). If the level is below this value, the S/N of the FM signal is considered to be acceptable. Values are given for FM with standard deviation. SQTH S/N (dB) FAh 0 77h 10 3Ch 15 (Default) 23h 20 19h 25

CAROFFSET1 Channel 1 DCO Carrier Offset Compensation

Address: 22h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CAROFFSET1[7:0] (S)							

Bit Name	Reset	Function
CAROFFSET1[7:0]	00000000	This value is used to correct the carrier frequency offset of the incoming IF signal. Automatic frequency control in FM mode can be implemented by registers DC_REMOVAL_L and DC_REMOVAL_R. A DCO frequency offset (in two's complement format) is added to the pre-programming value by AUTOTSD in the CARFQ1 registers (corresponding to the standard IF carrier frequency). The programmable carrier offset ranges from -192 kHz to +190.5 kHz with a resolution of 1.5 kHz. For standard FM deviation, the value displays by DC_REMOVAL_L and DC_REMOVAL_R can be directly loaded in CAROFFSET1 to exactly compensate the carrier offset on Channel 1

CHANNEL_GAIN Demodulator channel gain

Address:45h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	CH_GAIN[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
CH_GAIN[1:0]	10	**Channel 1 Gain after the FM Demodulation** 00: Gain 01: Gain * 2 10: Gain*4 (Default) 11: Gain *8

STEREO_CONF BTSC Stereo Configuration

Address:43h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOCK_TH_STE[7:4]				LOOP_GAIN[1:0]		FREQ_PIL	RESET

Bit Name	Reset	Function
LOCK_TH_STE[7:4]	0011	**BTSC Lock Stereo Threshold**
LOOP_GAIN[1:0]	10	**Gain of Stereo PLL** 00: Gain * 4 01: Gain * 2 10: Gain (Default) 11: Gain / 2
FREQ_PIL	0	**Pilot Frequency Selection** 0: 15.625-15.734 kHz 1: Reserved
RESET	0	**Stereo Reset** 1: Reset Active

STEREO_FSM_CONF BTSC Finite State Machine Configuration

Address:44h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	BYPASS	FSM_OFF	GAIN_INI[2:0]			STE_DEM

Bit Name	Reset	Function
BIT[7:6]	00	Reserved.
BYPASS	0	**Bypass of the Stereo Block** 0: Stereo Block is On 1: Stereo Block is Bypassed
FSM_OFF	0	**FSM Switch Off** 0: FSM is On 1: FSM is Off. Gain set by I²C
GAIN_INI[2:0]	111	**Initial loop gain for FSM**
STE_DEM	0	**Stereo dematrix inside the stereo block (before DBX)** 1: reset active

STEREO_LEVEL_H BTSC Threshold High for Stereo Detection

Address:45h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STE_LEV_H[7:0]							

Bit Name	Reset	Function
STE_LEV_H[7:0]	00100011	**Threshold High for Stereo Detection** If carrier level is > STE_LEV_H, stereo is detected

STEREO_LEVEL_L BTSC Threshold Low for Stereo Detection

Address:46h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STE_LEV_L[7:0]							

Bit Name	Reset	Function
STE_LEV_L[7:0]	00001100	**Threshold Low for Stereo Detection** If carrier level is <STE_LEV_L, stereo is not longer detected

SAP_CONF BTSC SAP Selection

Address:47h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	SAP_SEL

Bit Name	Reset	Function
bit[7:1]	0000000	Reserved.
SAP_SEL	0	**Selection of the SAP** 0: Stereo selected 1: SAP is selected on second channel

SAP_LEVEL_H BTSC Threshold High for SAP Detection

Address:48h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAP_LEV_H[7:0]							

Bit Name	Reset	Function
SAP_LEV_H[7:0]	01010000	**Threshold high for SAP detection** If SAP signal level is > SAP_LEV_H, SAP is detected

SAP_LEVEL_L BTSC Threshold Low for SAP Detection

Address:49h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAP_LEV_L[7:0]							

Bit Name	Reset	Function
SAP_LEV_L[7:0]	00110000	**Threshold low for SAP detection** If sap signal level is <STE_LEV_L, SAP is not longer detected

STE_CAR_LEV BTSC Stereo Carrier Level

Address:4Ah

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STE_CAR_LEV[7:0]							

Bit Name	Reset	Function
STE_CAR_LEV[7:0]	00000000	**Stereo carrier level**

STE_PLL_STAT BTSC Stereo PLL Status

Address:4Bh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	LOOP_GAIN[3:0]			OVER	LOCK_DET	STE_DET

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
LOOP_GAIN[3:0]	000	**Final FSM gain at the end of the stereo search process**
OVER	0	**Overflow append in stereo search process** 1: overflow
LOCK_DET	0	**Stereo PLL lock status** 0: no lock on pilot 1: lock on pilot or no pilot detected (no stereo)
STE_DET	0	**Stereo Detection** 0: no stereo dectected 1: stereo detected

STE_SAP_STAT BTSC Stereo SAP Status

Address:4Ch

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	OVER	LOCK_DET	STE_DET	0	0	SQ_DET	SAP_DET

Bit Name	Reset	Function
Bit 7	0	Reserved.
OVER	0	**Overflow append in stereo search process** 1: overflow
LOCK_DET	0	**Stereo PLL lock status** 0: no lock on pilot 1: lock on pilot or no pilot detected (no stereo)
STE_DET	0	**Stereo detection** 0: no stereo dectected 1: stereo detected
bit[3:2]	00	Reserved.
SQ_DET	0	**Squelch detection of SAP** 0: problem of noise 1: level of noise is good
SAP_DET	0	**Signal detection of SAP** 0: SAP not detected 1: SAP detected

PLL_P_G BTSC PLL Proportionnal Gain

Address:4Dh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_P_G[7:0]							

Bit Name	Reset	Function
PLL_P_G[7:0]	01101100	**PLL Proportional Gain**

PLL_I_G BTSC PLL Integral Gain

Address:4Eh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	PLL_I_G[3:0]			

Bit Name	Reset	Function
Bits [7:4]	0000	Reserved.
PLL_I_G[3:0]	0011	**PLL integral Gain**

SAP_SQ_TH SAP Squelch Threshold

Address:4Fh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAP_SQ_TH[7:0]							

Bit Name	Reset	Function
SAP_SQ_TH[7:0]	00110000	**SAP squelch threshold**

12.7 I2S and Analog Control

I2S_ADC_CTRL I2S_DATA0 and ADC Input Selection and Power-up

Address: 56h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2S_DATA0_CTRL[2:0]			0	ADC_ POWER_UP	ADC_INPUT_SEL[2:0]		

Bit Name	Reset	Function
I2S_DATA0_CTRL[2:0]	000	**Source selection for output I2S_DATA0** 000: LR 001: HP_LSS 010: LS_C and LS_SUB 011: SCART DAC 100: S/PDIF_OUT 101: DELAY 110: reserved 111: reserved
Bit[4]	0	Reserved.
ADC_POWER_UP	1	**Control of the power up of the Audio ADC** 0: ADC in power down mode 1: Wake up of the ADC
ADC_INPUT_SEL[2:0]	000	**Selection of the ADC input signal** 000: Input SCART 1 (Default) (B SDIP64) 001: Input SCART 2 (res. SDIP 64) 010: Input SCART 3 (res. SDIP 64) 011: Input SCART 4 (res. SDIP 64) 100: Input Mono 101: Input SCART (res. TQFP) (A SDIP64) (1_BIS) 110: Input SCART (5 TQFP100) (C SDIP64) (3_BIS) 111: reserved (mute)

SCART1_2_OUTPUT_CTRL SCART 1_2 Input Selection and Mute

Address: 57h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SC2_MUTE	SC2_OUTPUT_SEL[2:0]			SC1_MUTE	SC1_OUTPUT_SEL[2:0]		

Bit Name	Reset	Function
SC2_MUTE	1	**Mute command for the output SCART 2** 0: output not muted 1: output muted
SC2_OUTPUT_SEL[2:0]	010	**Selection of the output SCART 2 configuration:** 000: DSP 001: Input Mono 010: Input SCART 1 (Def) (B SDIP 64) 011: Input SCART 2 (res. SDIP 64) 100: Input SCART 3 (res. SDIP 64) 101: Input SCART 4 (res. SDIP 64) 110: Input SCART (res. TQFP) (A SDIP 64) (1_BIS) 111: Input SCART (5 TQFP 100) (C SDIP 64) (3_BIS)
SC1_MUTE	1	**Mute command for the output SCART 1** 0: output not muted 1: output muted
SC1_OUTPUT_SEL[2:0]	000	**Selection of the output SCART 1 configuration:** 000: DSP (Default) 001: Input Mono 010: Input SCART 1 (B SDIP 64) 011: Input SCART 2 (res SDIP 64) 100: Input SCART 3 (res. SDIP 64) 101: Input SCART 4 (res. SDIP 64) 110: Input SCART (res. TQFP) (A SDIP 64) (1_BIS) 111: Input SCART (5 TQFP100) (C SDIP64) (3_BIS)

SCART3_OUTPUT_CTRL SCART 3 Input Selection and Mute

Address: 58h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	SC3_MUTE	SC3_OUTPUT_SEL[2:0]		

Bit Name	Reset	Function
Bits[7:4]	0000	Reserved.
SC3_MUTE	1	**Mute command for the output SCART 3** 0: output not muted 1: output muted
SC3_OUTPUT_SEL[2:0]	011	**Selection of the output SCART 3 configuration:** 000: DSP 001: Input Mono 010: Input SCART 1 (B SDIP) 011: Input SCART 2 (Default) (res. SDIP 64) 100: Input SCART 3 (res. SDIP 64) 101: Input SCART 4 (res. SDIP 64) 110: Input SCART (res. TQFP) (A SDIP64) (1_BIS) 111: Input SCART (5 TQFP 100) (C SDIP 64) (3_BIS)

I2SO_DATA_CTRL I2S Data Source Control

Address: 59h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	I2SO_DATA1_CTRL[2:0]			0	I2SO_DATA0_CTRL[2:0]		

Bit Name	Reset	Function
Bit [7]	0	Reserved.
I2SO_DATA1_CTRL [2:0]	000	**Source Selection for I2SO_DATA1 Output** 000: Mute 001: LR 010: HP_LSS 011: LS_C and LS_SUB 100: SCART DAC 101: S/PDIF_OUT 110: Delay 111: Mute
Bit [3]	0	Reserved.
I2SO_DATA0_CTRL [2:0]	000	**Source Selection for I2SO_DATA0 Output** 000: Mute 001: LR 010: HP_LSS 011: LS_C and LS_SUB 100: SCART DAC 101: S/PDIF_OUT 110: Delay 111: Mute

12.8 Clocking 2

FS2_DIV FS2 I/O Divider Programming Register

Address: 5Ah

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	NDIV2[1:0]			SDIV2[2:0]		

Bit Name	Reset	Function
Bit [7:6]	0	Reserved.
NDIV2[1:0]	01	FS2 Input clock divider selection
Bit 4	0	Reserved.
SDIV2[2:0]	001	FS2 Output clock divider selection

FS2_MD FS2 Coarse Selection Register

Address: 5Bh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	MD2[4:0]				

Bit Name	Reset	Function
Bits[7:5]	000	Reserved.
MD2[4:0]	10001	FS2 Coarse Selection

FS2_PE_H FS2 Fine Selection Register (MSBs)

Address: 5Ch

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PE_H2[7:0]							

Bit Name	Reset	Function
PE_H2[7:0]	0101 1100	FS2 Fine Selection (MSBs)

FS2_PE_L FS2 Fine Selection Register (LSBs)

Address: 5Dh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PE_L2[7:0]							

Bit Name	Reset	Function
PE_L2[7:0]	0010 1001	FS2 Fine Selection (LSBs)

12.9 DSP Control

HOST_CMD DSP Hardware Control

Address: 80h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IT_IN_DSP	0	0	0	0	HW_RESET	PATCH_WRITE_ENABLE	EMUL_SW

Bit Name	Reset	Function
IT_IN_DSP	0	Valid I2C table.
Bits[6:3]	0000	Reserved.
HW_RESET	0	DSP Hardware reset when set.
Bits[1:0]	00	Reserved.

IRQ_STATUS IRQ Status

Address: 81h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
IRQ5	0	Hp/Srnd DAC unmute ready
IRQ4	0	HP detected

Bit Name	Reset	Function
IRQ3	0	I2S SRC freq change detected
IRQ2	0	I2S sync found IRQ
IRQ1	0	I2S sync lost IRQ
IRQ0	0	Auto-Standard IRQ

FW_VERSION Embedded Firmware Version

Address: 82h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FW_VERSION[7:0]							

Bit Name	Reset	Function
SOFT_VERSION [7:0]	0000 0011	Version of the Embedded software.

ONCHIP_ALGOS Display Algorithms available on the chip

Address: 83h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	PROLOGIC_TYPE	MULTI_I2S_IN	TRUBASS	TRU SURROUND	PROLOGIC	MULTICHANNEL_OUT

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
PROLOGIC_TYPE	0	0: ProLogic 1 1: ProLogic 2
MULTI_I2S_IN	0	0: 1 I2S input 1: 3 I2S inputs
TRUBASS	0	SRS TruBass algorithm is present when set.
TRUSURROUND	0	SRS TruSurround algorithm is present when set.
PROLOGIC	0	Dolby Pro Logic algorithm is present when set.
MULTICHANNEL_OUT	0	Multi-Channel output is present when set.

DSP_STATUS DSP Status

Address: 84h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	INIT_MEM

Bit Name	Reset	Function
Bits[7:1]	0000000	Reserved.
INIT_MEM	0	DSP Initialization 0: DSP is not initialized. 1: DSP is initialized.

DSP_RUN DSP Configuration and Run

Address: 85h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	TEST_MODE_INPUT	TEST_MODE		INPUT_CONFIG		REGISTERS_RESET	HOST_RUN

Bit Name	Reset	Function
Bits[7]	0	Reserved.
TEST_MODE_INPUT	0	active in TEST_MODE = 1 (bypass processing) 0: I2S_0 input -> L/R output I2S_1 input -> C/LFE output I2S_2 input -> Ls/Rs output I2S_0 input -> SCART output (-6dB) 1: I2S_0 input -> L/R output I2S_0 input -> C/LFE output I2S_0 input -> Ls/Rs output I2S_0 input -> SCART output (-6dB)
TEST_MODE[5:4]	00	00: standard configuration 01: bypass processing configuration 10: Clock Loop test 11: Not Used
INPUT_CONFIG	00	00: BTSC + I2S SRC + I2S DELAY + ADC 01: BTSC + I2S 48K + I2S DELAY + ADC 10: Not Used 11: BTSC + MULTI I2S 48K + ADC
RESGISTERS_RESET	0	0: I2C register table is not initialized when we soft reset 1: I2C register table is initialized when we soft reset
HOST_RUN	0	0: Soft Reset DSP 1: Start DSP

I2S_IN_CONFIG I2S Configuration

Address: 86h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOCK_MODE_EN	RESET_I2S	SYNC	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE

Bit Name	Reset	Function
LOCK_MODE_EN	1	0: Disable Lock Mode for external I2S input 1: Enable Lock Mode for external I2S input
RESET_I2S	0	Reset I2S input sync when set
SYNC	0	I2S Synchronisation: 0: Direct Capture 1: Wait for Sync signal
LRCLK_START	0	according to LRCLK POLARITY, first data take: 0: Left 1: Right
LRCLK_POLARITY	0	Polarity of the left data
SCLK_POLARITY	1	0: Falling Edge 1: Rising Edge
DATA_CFG	1	0: LSB First 1: MSB First
I2S_MODE	1	0: Not Standard Mode 1: Standard Mode

Note: This register must be set before the Start of the Software (85h: HOST_RUN = 1).

I2S_IN_SHIFT_RIGHT I2S Shift Right

Address: 87h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	SHIFT_RIGHT_RANGE[4:0]				

Bit Name	Reset	Function
Bits [7:5]	000	Reserved
SHIFT_RIGHT_RANGE[4:0]	01000	Define the shift right to apply to 32-bit input samples. Range: 0 to 31

Note: This register has to be set before the Start of the Software (0x85 : HOST_RUN = 1).

I2S_IN_MASK I2S Mask

Address: 88h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	WORD_MASK[4:0]				

Bit Name	Reset	Function
Bits [7:5]	000	Reserved
WORD_MASK[4:0]	11111	Define the mask to apply to 32-bit input samples. Range: 0 to 31

Note: This register has to be set before the Start of the Software (0x85 : HOST_RUN = 1).

I2S_IN_STATUS SRC I2S Input Behaviour

Address: 89h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTO_SRC_SYNC	ENABLE_IRQ_SRC_FREQ_CHANGE	ENABLE_IRQ_SYNC_FOUND	ENABLE_IRQ_SYNC_LOST		I2S_INPUT_FREQ		

Bit Name	Reset	Function
AUTO_SRC_SYNC	0	Allow the DSP to reset the SRC input DMA when an input freq change is detected. (Working in SRC mode only) 0: no reset on input frequency change 1: reset on input frequency change
ENABLE_IRQ_SRC_FREQ_CHANGE	0	Generate an IRQ3 when a frequency change is detected on SRC input. (Working in SRC mode only) 0: IRQ3 generation not active 1: IRQ3 generation active
ENABLE_IRQ_SYNC_FOUND	0	Generate an IRQ2 when a signal is synchronized on SRC input. (Working in SRC mode only) 0: IRQ2 generation not active 1: IRQ2 generation active
ENABLE_IRQ_SYNC_LOST	0	Generate an IRQ1 when a signal is lost on SRC input. (Working in SRC mode only) 0: IRQ1 generation not active 1: IRQ1 generation active
Bits [3]	0	Reserved
I2S_INPUT_FREQ	(000)	Display the frequency detected on SRC input 000: no signal locked on SRC input 001: 32 kHz 010: 44.1 kHz 011: 48 kHz 100: signal locked but frequency unknown 101: not used 110: not used 111: not used

12.10 Automatic Standard Recognition

AUTOSTD_CTRL Automatic Standard Recognition Control

Address: 8Ah

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SINGLE_SHOT	MONO_SAP_CTRL_MATRIX	FORCE_SQ_SAP	FORCE_SQ_MONO	AUTO_MUTE	SAP_CHECK	STEREO_CHECK	MONO_CHECK

Bit Name	Reset	Function
SINGLE_SHOT	0	Single-shot mode (To be selected whith any of the Mono/Stereo or Sap check bits): 0: Single Shot mode is not selected 1: Single Shot mode is selected[1]
MON_SAP_CONTROL_MATRIX	0	Change the behaviour of the automatic matrix control for SAP language 0: When SAP signal is detected, SAP signal is outputed on both Left and Right channels 1: When SAP signal is detected, Mono signal is outputed on the Left channel and SAP signal is outputed on the Right channe
FORCE_SQ_SAP	0	Force the squelch status during SAP detection by autostandard. 0: SAP squelch from demod status 1: SAP squelch forced to 1
FORCE_SQ_MONO	0	Force the squelch status during MONO detection by autostandard. 0: MONO squelch from demod status 1: MONO squelch forced to 1
AUTO_MUTE	0	0: Output channels are never mutted 1: Output channels are automaticly muted when no signal is detected
SAP_CHECK	0	0: No SAP standard research 1: SAP standard research
STEREO_CHECK	0	0: No STEREO standard research 1: STEREO standard research (priority is given to SAP if selected)
MONO_CHECK	0	0: No MONO standard research (AutoStandard OFF) 1: MONO standard research (mandatory to activate Autostandard)

1. ***Single_Shot*** *mode will pre-program demodulator registers in a choosen standard (bits b2, b1, b0). Autostandard will be switched OFF (Mono_check = 0) after the programation of the registers.*

AUTOSTD_TIME Detection Time Out

Address: 8Bh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	STEREO_TIME[2:0]			FM_TIME[1:0]	

Bit Name	Reset	Function
Bits [7:5]	000	Reserved
STEREO_TIME[2:0]	000	**Stereo Detection Time-out** 000: 20 ms (Default) 100: 400 ms 001: 40 ms 101: 800 ms 010: 100 ms 110: 1200 ms 011: 200 ms 111: 1600 ms
FM_TIME[1:0]	10	**FM Detection Time-out** 00: 16 ms 10: 48 ms (Default) 01: 32 ms 11: 64 ms

Note: The time-out default value is optimum and does not normally need to be changed.

AUTOSTD_STATUS Detection Standard Status

Address: 8Ch

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	SAP_OK	STEREO_OK	MONO_OK	AUTOSTD_ON

Bit Name	Reset	Function
Bits[7:4]	0000	Reserved.
SAP_OK	0	SAP Standard Recognition Status 0: SAP Standard not detected 1: SAP Standard detected
STEREO_OK	0	Stereo Standard Recognition Status 0: Stereo Standard not detected 1: Stereo Standard detected
MONO_OK	0	Mono Standard Recognition Status 0: Mono Standard not detected 1: Mono Standard detected
AUTOSTD_ON	0	Automatic Standard Recognition System Status 0: Automatic Standard Recognition System is OFF 1: Automatic Standard Recognition System is ON

AUTOSTD_DEM_STATUS Demodulator Status

Address: 8Dh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	OVERFLOW	LCK_DET	ST_DET	SAP_SQ	SAP_DET	FM1_CAR	FM1_SQ

Bit Name	Reset	Function
Bits[7]	0	Reserved.
LCK_DET	0	0: Stereo Lock Not Detected 1: Stereo Lock Detected
ST_DET	0	0: Stereo Not Detected 1: Stereo Detected
SAP_SQ	0	0: SAP Squelch Not Detected 1: SAP Squelch Detected
SAP_DET	0	0: SAP Not Detected 1: SAP Detected
FM1_CAR	0	0: FM1 Carrier Not Detected 1: FM1 Carrier Detected
FM1_SQ	0	0: FM1 Squelch Not Detected 1: FM1 Squelch Detected

DMA_FORCE_OFF Input DMA disable

Address: 8Eh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADC	I2S2	I2S1	I2S0	DEMOD

Bit Name	Reset	Function
Bits[7:5]	000	Reserved.
ADC	0	0: ADC input DMA active 1: ADC input DMA not active
I2S2	0	0: I2S2 input DMA active 1: I2S2 input DMA not active
I2S1	0	0: I2S1 input DMA active 1: I2S1 input DMA not active
I2S0	0	0: I2S0 input DMA active 1: I2S0 input DMA not active
DEMOD	0	0: Demod input DMA active 1: Demod input DMA not active

Note: This register must be set before the Start of the Software (85h: HOST_RUN = 1).

I2S_IN_DELAY_CONFIG I2S Configuration for Delay Input

Address: 8Fh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SYNC	LRCLK_START	LRCLK_POLARITY	SCLK_POLARITY	DATA_CFG	I2S_MODE

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
SYNC	0	I²S Synchronisation: 0: Direct Capture 1: Wait for Sync signal
LRCLK_START	0	according to LRCLK POLARITY, first data take: 0: Left 1: Right
LRCLK_POLARITY	0	polarity of the left data
SCLK_POLARITY	1	0: Falling Edge 1: Rising Edge
DATA_CFG	1	0: LSB First 1: MSB First
I2S_MODE	1	0: Not Standard Mode 1: Standard Mode

Note: For this input, the SHIFT_RIGHT and MASK of the I2S input are set.
SHIFT_RIGHT = 0x08
MASK = 0x1F

12.11 Demodulator

BTSC_FINE_PRESCALE_ST BTSC input prescale for Stereo Mode

Address: 90h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BTSC_FINE_PRESCALE_ST[7:0] (S)							

Bit Name	Reset	Function
BTSC_FINE_PRESCALE_ST[7:0]	0000 0000	Set the prescale of the signal coming from the demodulator when STEREO is demodulated in order to optimize the signal level at DBX block input (steps of 0.02 dB): 1000 0000: -2.56 dB ... 0000 0000: 0 dB 0000 0001: 0.02 dB ... 0111 1111: 2.54 dB

BTSC_FINE_PRESCALE_SAP BTSC Input Prescale for SAP Mode

Address: 91h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BTSC_FINE_PRESCALE_SAP[7:0] (S)							

Bit Name	Reset	Function
BTSC_FINE_PRESCALE_SAP[7:0]	0000 0000	Set the prescale of the signal coming from the demodulator when SAP is demodulated in order to optimize the signal level at DBX block input (steps of 0.02 dB): 1000 0000: -2.56 dB ... 0000 0000: 0 dB 0000 0001: 0.02 dB ... 0111 1111: 2.54 dB

BTSC_CONTROL BTSC Back-end Decoder Control

Address: 92h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FINE_PRESCALE_SELECT_SAP	DBX_DEMATRIX[1:0]		DBX_ON	DEEMPHASIS_CH1[1:0]		DEEMPHASIS_CH0[1:0]	

Bit Name	Reset	Function
FINE_PRESCALE_SELECT_SAP	0	Select the prescale value to apply on second channel before DBX 0: STEREO prescale (register 90h) 1: SAP prescale (register 91h)
DBX_DEMATRIX[1:0]	00	Select L/R Dematrix for STEREO standard 00: No dematrixing (Mono or SAP) 10: Reserved 01: L/R Dematrix (STEREO): L=Ch0+(Ch1)/2, R=Ch0-(Ch1)/2 11: Reserved
DBX_ON	0	0: DBX noise reductor not active 1: DBX noise reductor active on second channel (STEREO or SAP)

Bit Name	Reset	Function
DEEMPHASIS_CH1[1:0]	00	Select the demmphasis for demodulator second channel : 00: No De-emphasis 10: 50 µs De-emphasis 01: 25 µs De-emphasis 11: 75 µs De-emphasis
DEEMPHASIS_CH0[1:0]	00	Select the demmphasis for demodulator first channel : 00: No De-emphasis 10: 50 µs De-emphasis 01: 25 µs De-emphasis 11: 75 µs De-emphasis

DC_REMOVAL DC Removal

Address: 93h

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	DBX_FILTER_SELECT	DEEMPHASIS_FILTER_SELECT	0	DC_DEMOD_POST_ON	DC_DEMOD_PRE_ON	DC_SCART_ON

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
DBX_FILTER_SELECT	1	Select the type of filter used in the DBX block 0: 1st Order Filter De-emphasis 1: 2nd Order Filter De-emphasis
DEMPHASIS_FILTER_SELECT	1	Select the type of filter used in the De-emphasis block 0: 1st Order Filter De-emphasis 1: 2nd Order Filter De-emphasis
Bit[3]	0	Reserved
DC_DEMOD_POST_ON	0	Control the DC removal placed on the demod path, AFTER the DBX block: 0: DC removal OFF 1: DC Removal ON
DC_DEMOD_PRE_ON	0	Control the DC removal placed on the demod path, BEFORE the DBX block: 0: DC removal OFF 1: DC Removal ON
DC_SCART_ON	0	Control the DC removal placed on the SCART path: 0: DC removal OFF 1: DC Removal ON

12.12 Audio PreProcessing & Selection

PRESCALE_DEMOD_MONO Prescale for Demod MONO

Address: 94h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRESCALE_DEMOD_SELECT_SAP	PRESCALE_DEMOD_MONO[6:0] (S)						

Bit Name	Reset	Function
PRESCALE_DEMOD_SELECT_SAP	0	Select the prescale value to apply on channel 0 (Mono/Stereo): 0: Apply STEREO Prescale (95h) to the demodulated signal. To be used in case of STEREO demodulation. 1: Apply MONO Prescale (94h) on left channel and SAP Prescale (96h) on right channel to the demodulated signal. To be used in case of MONO or SAP demodulation.
PRESCALE_DEMOD_MONO[6:0]	000 0000	Set the prescale of the signal coming from the demodulator when MONO (Channel 0): 101 0000: -12 dB ... 000 0000: 0 dB 000 0001: 0.5 dB ... 011 0000: 24 dB

PRESCALE_DEMOD_STEREO Prescale for Stereo Demodulation

Address: 95h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PRESCALE_DEMOD_STEREO[6:0] (S)						

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PRESCALE_DEMOD_STEREO[6:0]	000 0000	Sets the prescale value of the Stereo signal coming from the demodulator (Channels 0 and 1): 101 0000: -12 dB ... 000 0000: 0 dB 000 0001: 0.5 dB ... 011 0000: 24 dB

PRESCALE_DEMOD_SAP Prescale for SAP Demodulation I

Address: 96h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PRESCALE_DEMOD_SAP[6:0] (S)						

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PRESCALE_DEMOD_SAP[6:0]	000 0000	Set the prescale of the signal coming from the demodulator when SAP (channel 0): 101 0000: -12dB ... 000 0000: 0dB 000 0001: 0.5dB ... 011 0000: 24dB

PRESCALE_SCART Prescale for SCART

Address: 97h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PRESCALE_SCART[6:0] (S)						

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PRESCALE_SCART[6:0]	000 0000	Set the prescale of the signal coming from the SCART ADC: 101 0000: -12dB ... 000 0000: 0dB 000 0001: 0.5dB ... 011 0000: 24dB

PRESCALE_I2S0 Prescale for I2S0

Address: 98h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PRESCALE_I2S0[6:0] (S)						

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PRESCALE_I2S0[6:0]	000 0000	Set the prescale of the signal coming from the I2S0 (SRC input or I2S0 in multichannel input mode): 101 0000: -12dB ... 000 0000: 0dB 000 0001: 0.5dB ... 011 0000: 24dB

PRESCALE_I2S1 Prescale for I2S1

Address: 99h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PRESCALE_I2S1[6:0] (S)						

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PRESCALE_I2S1[6:0]	000 0000	Set the prescale of the signal coming from the I2S1 (I2S1 in multichannel input mode): 101 0000: -12dB ... 000 0000: 0dB 000 0001: 0.5dB ... 011 0000: 24dB

PRESCALE_I2S2 Prescale for I2S2

Address: 9Ah

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PRESCALE_I2S2[6:0] (S)						

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PRESCALE_I2S2[6:0]	000 0000	Set the prescale of the signal coming from the I2S2 (delay input or I2S2 in multichannel input mode): 101 0000: -12dB ... 000 0000: 0dB 000 0001: 0.5dB ... 011 0000: 24dB

PEAK_DETECTOR Peak Detector

Address: 9Bh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PEAK_L_R_RANGE[2:0]			PEAK_DET_INPUT[2:0]			PEAK_DETECTOR_ON

Bit Name	Reset	Function
Bits[7]	0	Reserved.
PEAK_L_R_RANGE[2:0]	000	Control the sensitivity of the “Left - Right” peak measurement (register 0x9E). The difference between Left and Right signal is sometime very small (in case of mono input for example), so we can multiply the “Left - Right” peak measurement in order to add precision: 000: Left - Right 100: (Left - Right) x 16 001: (Left - Right) x 2 101: (Left - Right) x 32 010: (Left - Right) x 4 110: (Left - Right) x 64 011: (Left - Right) x 8 111: (Left - Right) x 128
PEAK_DETECTOR_INPUT[2:0]	000	Select the input on which the peak detector makes the measurement: 000: demod signal 100: SCART signal 001: I2S0 signal 101: reserved 010: I2S1 signal 110: reserved 011: I2S2 signal 111: reserved
PEAK_DETECTOR_ON	0	Control the Peak detector: 0: Peak detector OFF 1: Peak detector ON

PEAK_L Peak Detector Left Channel

Address: 9Ch

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OVERLOAD_L	PEAK_L[6:0] (S)						

Bit Name	Reset	Function
OVERLOAD_L	0	This bit is set to 1 by the DSP when the Left peak detector reaches its maximum value (0x7F). It can be reset to 0.
PEAK_L[6:0]	000 0000	Displays the Absolute Peak Level of the Left channel of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB). 000 0000:<-36dBFS 000 1111:-18dBFS ... ... 000 0001:-36dBFS 001 1111:-12dBFS ... ... 000 0011:-30dBFS 011 1111:-6dBFS ... ... 000 0111:-24dBFS 111 1111:0dBFS ...

PEAK_R Peak Detector Right Channel

Address: 9Dh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OVERLOAD_R	PEAK_R[6:0] (S)						

Bit Name	Reset	Function
OVERLOAD_R	0	This bit is set to 1 by the DSP when the Right peak detector reaches its maximum value (0x7F). It can be reset to 0.
PEAK_R[6:0]	000 0000	Displays the Absolute Peak Level of the Right channel of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB). 000 0000:<-36dBFS 000 1111:-18dBFS ... ... 000 0001:-36dBFS 001 1111:-12dBFS ... ... 000 0011:-30dBFS 011 1111:-6dBFS ... ... 000 0111:-24dBFS 111 1111:0dBFS ...

PEAK_L_R Peak Detector Left Minus Right Channel

Address: 9Eh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OVERLOAD_L_R	PEAK_L_R[6:0] (S)						

Bit Name	Reset	Function
OVERLOAD_L_R	0	This bit is set to 1 by the DSP when the “Left-Right” peak detector reaches its maximum value (0x7F). It can be reset to 0.
PEAK_L_R[6:0]	000 0000	Displays the Difference between L and R (L - R) channels for the audio source selected: 000 0000:<-36dBFS 000 1111:-18dBFS ... ... 000 0001:-36dBFS 001 1111:-12dBFS ... ... 000 0011:-30dBFS 011 1111:-6dBFS ... ... 000 0111:-24dBFS 111 1111:0dBFS ...

12.13 Matrixing

DOWNMIX_MODE Downmix Mode Configuration

Address: 9Fh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LT_RT_OUT_MODE	MIX_OUT_MODE[2:0]			LFE_IN	MIX_IN_MODE[2:0]		

Bit Name	Reset	Function
LT_RT_OUT_MODE	0	Define to format for downmix Lt/Rt output: 0: Lt/Rt Prologic compatible mode 1: L/R stereo mode
MIX_OUT_MODE[2:0]	111	Select output channels configuration for downmix: see table 3.
LFE_IN	1	To select if LFE is inputed on I2S1 in multichannel input mode: 0: No LFE on I2S1 input 1: LFE on I2S1 input
MIX_IN_MODE[2:0]	111	Select input channels configuration for downmix: see table 2.

Table 11: DownMix IN modes

Parameter Coding (bin)	Parameter Field Lebel	Function
000	MODE11	not used
001	MODE10	1/0 (C)
010	MODE20	2/0 (L,R)
011	MODE30	3/0 (L,R,C)
100	MODE21	2/1 (L,R,S)
101	MODE31	3/1 (L,R,C,S)
110	MODE22	2/2 (L,R,Ls,Rs)
111	MODE32	3/2 (L,R,C,Ls,Rs)

Table 12: DownMix OUT modes

Parameter Coding (bin)	Parameter Field Lebel	Function
000	MODE20t	2/0 Dolby Surround (Lt,Rt)
001	MODE10	1/0 (C)
010	MODE20	2/0 (L,R)

Table 12: DownMix OUT modes (Continued)

Parameter Coding (bin)	Parameter Field Lebel	Function
011	MODE30	3/0 (L,R,C)
100	MODE21	2/1 (L,R,S)
101	MODE31	3/1 (L,R,C,S)
110	MODE22	2/2 (L,R,Ls,Rs)
111	MODE32	3/2 (L,R,C,Ls,Rs)

DOWNMIX_DUAL_MODE Downmix Dual Mode Configuration

Address: A0h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	DUAL_ON	LS_DUAL_SELECT[1:0]		LTRT_DUAL_SELECT[1:0]	

Bit Name	Reset	Function
Bits[7:5]	000	Reserved.
DUAL_ON	0	Select dual mode for DownMix bloc in case of dual language (in dual mode, Input and output mode are forced to 2_0): 0: Standard DownMix 1: DownMix in Dual Mode
LS_DUAL_SELECT [1:0]	00	Select the language for LS output in case of Dual mode: 00: Stereo 10: Right mono 01: Left mono 11: Left + Right mix
LTRT_DUAL_SELECT[1:0]	00	Select the language for LtRt output in case of Dual mode: 00: Stereo 10: Right mono 01: Left mono 11: Left + Right mix

DOWNMIX_CONFIG Downmix Configuration

Address: A1h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SRND_FACTOR[1:0]		CENTER_FACTOR[1:0]		LR_UPMIX	NORMALIZE

Bit Name	Reset	Function
Bits[7:6]	00	Reserved
SRND_FACTOR [1:0]	00	00: -3 dB 10: -6 dB 01: -4.5 dB 10: -6 dB

Bit Name	Reset	Function
CENTER_FACTOR [1:0]	00	00: -3 dB 10: -6 dB 01: -4.5 dB 11: -4.5 dB
LR_UPMIX	0	0: Upmixing disabled 1: Upmixing enabled (DTS specified)
NORMALIZE	1	0: Normalization disabled 1: Nnormalization enabled

AUDIO_MATRIX1 AudioMatrix Configuration Register

Address: A2h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	HP_OUT			LS_OUT		

Bit Name	Reset	Function
Bits[7:6]	00	Reserved
HP_OUT[1:0]	010	Select the source to output on HP. See table 4.
LS_OUT[1:0]	010	Select the source to output on LS. See table 4.

AUDIO_MATRIX2 AudioMatrix part configurationr

Address: A3h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SCART2_OUT			SCART1_OUT		

Bit Name	Reset	Function
Bits[7:6]	00	Reserved
SCART2_OUT [1:0]	010	Select the source to output on SCART2: see table 4.
SCART1_OUT [1:0]	010	Select the source to output on SCART1: see table 4.

AUDIO_MATRIX3 AudioMatrix part configuration

Address: A4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SPDIF_OUT			DELAY_OUT		

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
SPDIF_OUT[1:0]	010	Select the source to output on SPDIF. See table 4.
DELAY_OUT[1:0]	010	Select the source to output on DELAY. See table 4.

Table 13: AudioMatrix Input Sources

Parameter Coding (bin)	Parameter Field Lebel	Function
000	MUTE	Mute Output
001	DELAY	Delay Input
010	DEMOD	BTSC Demod Input
011	LtRt	Downmix LtRt Input
100	I2S	I2S Input
101	SCART	SCART Input
110	-	Reserved
111	-	Reserved

CHANNEL_MATRIX_LS Channel Matrix Configuration

Address: A5h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTOSTD_CTRL_LS	AUTOSTD_CTRL_SPDIF	0	0	0	CM_MATRIX_LS[2:0]		

Bit Name	Reset	Function
AUTOSTD_CTRL_LS	0	If this bit is activated, Autostandard algorithm will select automaticaly the appropriate matrixing (Bits[2:0]) for LS output channels depending on the detected standard (see table 6). 0: Manual Matrix Selection 1: Automatic Matrix Selection if AutoStandard is ON *Note: Automatic Matrix Selection must be used only when DEMOD signal is directed to the Matrix.*

Bit Name	Reset	Function
AUTOSTD_CTRL_SPDIF	0	If this bit is activated, Autostandard algorithm will select automaticaly the appropriate matrixing (bits[2:0]) for SPDIF output channels depending on the detected standard (see table 6). 0: Manual Matrix Selection 1: Automatic Matrix Selection if AutoStandard is ON *Note: Automatic Matrix Selection must be used only when DEMOD signal is directed to the Matrix.*
Bits[5:3]	000	Reserved
CM_MATRIX_LS[2:0]	0000	Select the matrixing for the LS channels. See table 5.

CHANNEL_MATRIX_HP Channel Matrix Configuration

Address: A6h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTOSTD_CTRL_HP	CM_SOURCE_HP[1:0]		CM_POSITION_HP[1:0]		CM_MATRIX_HP[2:0]		

Bit Name	Reset	Function
AUTOSTD_CTRL_HP	0	If this bit is activated, Autostandard algorithm will select automaticaly the appropriate matrixing (bits[2:0]) for HP output channels depending on the detected standard (see table 6). 0: Manual Matrix Selection 1: Automatic Matrix Selection if AutoStandard is ON *Note: Automatic Matrix Selection must be used only when DEMOD signal is directed to the Matrix.*
CM_SOURCE_HP[2:0]	00	Select the source to copy on HP channel. See table 7.
CM_POSITION_HP[1:0]	00	Select the position for the HP matrix. See block diagram
CM_MATRIX_HP[2:0]	0000	Select the matrixing for the HP channels. See table 5.

CHANNEL_MATRIX_SCART1 Channel Matrix configuration

Address: A7h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTOSTD_CTRL_SCART1	CM_SOURCE_SCART1[1:0]		CM_POSITION_SCART1[1:0]		CM_MATRIX_SCART1[2:0]		

Bit Name	Reset	Function
AUTOSTD_CTRL_SCART1	0	If this bit is activated, Autostandard algorithm will select automaticaly the appropriate matrixing (Bits[2:0]) for SCART1 output channels depending on the detected standard (see table 6). 0: Manual Matrix Selection 1: Automatic Matrix Selection if AutoStandard is ON *Note: Automatic Matrix Selection must be used only when DEMOD signal is directed to the Matrix.*
CM_SOURCE_SCART1[2:0]	00	Select the source to copy on SCART1 channel. See table 7.
CM_POSITION_SCART1[1:0]	00	Select the position for the SCART1 matrix. See block diagram
CM_MATRIX_SCART1[2:0]	0000	Select the matrixing for the SCART1 channels. See table 5.

CHANNEL_MATRIX_SCART2 Channel Matrix configuration

Address: A8h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTOSTD_CTRL_SCART2	CM_SOURCE_SCART2[1:0]		CM_POSITION_SCART2[1:0]		CM_MATRIX_SCART2[2:0]		

Bit Name	Reset	Function
AUTOSTD_CTRL_SCART2	0	If this bit is activated, Autostandard algorithm will select automaticaly the appropriate matrixing (Bits[2:0]) for SCART2 output channels depending on the detected standard (see table 6). 0: Manual Matrix Selection 1: Automatic Matrix Selection if AutoStandard is ON *Note: Automatic Matrix Selection must be used only when DEMOD signal is directed to the Matrix.*
CM_SOURCE_SCART2[2:0]	00	Select the source to copy on SCART2 channel. See table 7.
CM_POSITION_SCART2[1:0]	00	Select the position for the SCART2 matrix. See block diagram
CM_MATRIX_SCART2[2:0]	0000	Select the matrixing for the SCART2 channels. See table 5.

CHANNEL_MATRIX_SPDIF Channel Matrix Configuration

Address: A9h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM_SOURCE_SPDIF[2:0]			CM_POSITION_SPDIF[1:0]		CM_MATRIX_SPDIF[2:0]		

Bit Name	Reset	Function
CM_SOURCE_SPDIF[2:0]	000	Select the source to copy on SPDIF channel. See table 7.
CM_POSITION_SPDIF[1:0]	00	Select the position for the SPDIF matrix. See block diagram.
CM_MATRIX_SPDIF[2:0]	0000	Select the matrixing for the SPDIF channels. See table 5.

Table 14: Channel Matrix Modes

Parameter Coding (Bin)	Parameter Field Lebel	Function
000	BYPASS	Bypass Stereo Signal
001	LEFT ONLY	Copy Left Signal On Both Channels
010	RIGHT ONLY	Copy Right Signal On Both Channels
011	LEFT + RIGHT MIX	Copy (Left + Right)/2 On Both Channels
100	SWAP	Swap Channel (Left = Right, Right = Left)
101	-	Reserved
110	-	Reserved
111	-	Reserved

Table 15: Automatic Channel Matrix Modes

Standard Detected by Autostandard	MONO_SAP_CTRL_MATRIX reg 0x8A, bit[6] value = 0		MONO_SAP_CTRL_MATRIX reg 0x8A, bit[6] value = 1	
	Left Output	Right Output	Left Output	Right Output
Mono	Mono Signal	Mono Signal	Mono Signal	Mono Signal
Stereo	Left Signal	Right Signal	Left Signal	Right Signal
SAP	SAP Signal	SAP Signal	Mono Signal	SAP Signal

Table 16: Channel Matrix Source Selection

Parameter Coding (Bin)	Parameter Field Lebel	Function
000	BYPASS	bypass stereo signal coming from Audiomatrix
001	LS Channels	copy signal from LS channels
010	HP Channels	copy signal from HP channels
011	C/Sub Channels	copy signal from C/Sub channels (ONLY AVAILABLE ON SPDIF CHANNEL MATRIX)
100	Ls/Rs Channels	copy signal from Ls/Rs channels (ONLY AVAILABLE ON SPDIF CHANNEL MATRIX)
101	-	Reserved

Table 16: Channel Matrix Source Selection (Continued)

Parameter Coding (Bin)	Parameter Field Lebel	Function
110	-	Reserved
111	-	Reserved

DEMOD_DC_LEVEL DC Level on Demod FM Mono Input

Address: AAh

Type: R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEMOD_DC_LEVEL[7:0] (S)							

Bit Name	Reset	Function
DEMOD_DC_LEVEL[7:0]	(0000 0000)	Display the amount of the DC component in the signal comming from the FM mono channel. This DC Level can be used to implement a Carrier Offset compensation.

12.14 Audio Processing

AV_DELAY_CONFIG AV Delay Configuration

Address: ADh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	DOLBY_DELAY_ON	AV_DELAY_ON

Bit Name	Reset	Function
Bits[7:2]	0000 00	Reserved
DOLBY_DELAY_ON	0	Must be set to 1 to use the Center, Left Srnd and Right Srnd delays for ProLogic decoder multi-channel output. *Note: This value must be updated when AV_DELAY_ON = 0..*
AV_DELAY_ON	0	0: No AV delay 1: AV delay is active

AV_DELAY_TIME_LS AV Delay LS Configuration

Address: AEh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AV_DELAY_TIME_LS[7:0]							

Bit Name	Reset	Function
AV_DELAY_TIME_LS[7:0]	0000 0000	Set the delay time for LS channel. 0000 0000: 0 ms 0000 0001: 0.66 ms ... 1011 0001: 116.82 ms (max) *Note: this value must be updated when AV_DELAY_ON = 0..*

AV_DELAY_TIME_HP AV Delay HP Configuration

Address: AFh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AV_DELAY_TIME_HP[7:0]							

Bit Name	Reset	Function
AV_DELAY_TIME_HP[7:0]	0000 0000	Set the delay time for HP channel. 0000 0000: 0 ms 0000 0001: 0.66 ms ... 1011 0001: 116.82 ms (max) *Note: this value must be updated when AV_DELAY_ON = 0..*

Note: The sum of AV_DELAY_TIME_LS and AV_DELAY_TIME_HP must not exceed:
- *177 (116.82 ms) if DOLBY_DELAY_ON = 0*
- *100 (66.66 ms) if DOLBY_DELAY_ON = 1*

PRO_LOGIC2_CONTROL Dolby ProLogic 2 Mode Configuration

Address: B0h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL2_LFE	PL2_OUTPUT_DOWNMIX[2:0]			PL2_MODES[2:0]			PL2_ACTIVE

Bit Name	Reset	Function
PL2_LFE	0	0: Reset the LFE channel 1: Bypass the LFE channel
PL2_OUTPUT_DOWNMIX[2:0]	000	000: not applicable 001: not applicable 010: not applicable 011: 3/0 output mode (L,R,C) 100: 2/1 output mode (L,R,Ls - phantom) 101: 3/1 output mode (L,R,C,Ls) 110: 2/2 output mode (L,R,Ls,Rs - phantom) 111: 3/2 output mode (L,R,C,Ls,Rs)
PL2_MODES[2:0]	000	000: Pro Logic 1 Emulation 001: Virtual 010: Music 011: Movie (standard) 100: Matrix 101: Custom 110: not applicable 111: not applicable
PL2_ACTIVE	0	0: Dolby Prologic 2 is not active 1: Dolby Prologic 2 is active

PRO_LOGIC2_CONFIG Dolby ProLogic 2 Configuration

Address: B1h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	PL2_SRND_FILTER[1:0]		PL2_RS_POLARITY	PL2_PANORAMA	PL2_AUTOBALANCE

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
PL2_SRND_FILTER[1:0]	00	00: Off 01: Shelf 10: 7-kHz LP 11: not applicable
PL2_RS_POLARITY	0	0: Rs polarity normal 1: Rs polarity inverted
PL2_PANORAMA	0	0: Panorama Off 1: Panorama On
PL2_AUTOBALANCE	0	0: Autobalance Off 1: Autobalance On

PRO_LOGIC2_DIMENSION Dolby ProLogic 2 Dimension

Address: B2h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PL2_C_WIDTH			0	PL2_DIMENSION		

Bit Name	Reset	Function
Bit 7	0	Reserved.
PL2_C_WIDTH[2:0]	000	ProLogic 2 center width: 000: 0, no spread 100: 54 001: 20 101: 62 010: 28 110: 69 011: 36 111: 90, phantom
Bit 3	0	Reserved.
PL2_DIMENSION [2:0]	000	ProLogic 2 dimension: 000: -3, most surround 100: 1 001: -2 101: 2 010: -1 110: 3, most center 011: 0, neutral 111: not used

PRO_LOGIC2_LEVEL Dolby ProLogic 2 Input Level

Address: B3h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL2_LEVEL							

Bit Name	Reset	Function
PL2_LEVEL[7:0]	00000000	Input Gain attenuation: 0000 0000: 0 dB 0000 0001: -0.5 dB ... 1111 1111: -127.5 dB

NOISE_GENERATOR Pink Noise Generator

Address: B4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10_DB_ATTENUATE	SRIGHT_NOISE	SLEFT_NOISE	SUB_NOISE	CENTER_NOISE	RIGHT_NOISE	LEFT_NOISE	NOISE_ON

Bit Name	Reset	Function
10_DB_ATTENUATE	0	0: noise is output with full range 1: noise is output with a 10dB attenuation
SRIGHT_NOISE	0	1: Generates noise on LS right surround output
SLEFT_NOISE	0	1: Generates noise on LS left surround output
SUB_NOISE	0	1: Generates noise on LS subwoofer output

Bit Name	Reset	Function
CENTER_NOISE	0	1: Generates noise on LS center output
RIGHT_NOISE	0	1: Generates noise on LS right output
LEFT_NOISE	0	1: Generates noise on LS left output
NOISE_ON	0	0: Noise Generation not active 1: Noise Generation active

PCM_SRND_DELAY Dolby Surround Delay

Address: B5h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	DOLBY_DELAY_SRND[4:0]				

Bit Name	Reset	Function
Bits[7:5]	000	Reserved.
DOLBY_DELAY_SRND[4:0]	00000	Surround Channel Delay Range: 0 to 30 (in ms)

Note: To use this feature, set the DOLBY_DELAY_ON bit to 1 in register AV_DELAY_CONFIG (ADh).

PCM_CENTER_DELAY Dolby Center Delay Register

Address: B6h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	DOLBY_DELAY_CENTER[3:0]			

Bit Name	Reset	Function
Bits[7:4]	0000	Reserved.
DOLBY_DELAY_CENTER[3:0]	0000	Center Channel Delay Range: 0 to 10 (in ms)

Note: To use this feature, set the DOLBY_DELAY_ON bit to 1 in register AV_DELAY_CONFIG (ADh).

TRUSRND_CONTROL SRS TruSurround Control

Address: B7h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIALOG_CLARITY_ON	HEADPHONE_ON	TRUSRND_INPUT_ MODE[3:0]				TRUSRND_BYPASS	TRUSRND_ON

Bit Name	Reset	Function
DIALOG_CLARITY_ON	0	0: Dialog Clarity OFF 1: Dialog Clarity ON *Note: The Dialog Clarity Level is set in register 0xB8: TRUSRND_DC_ELEVATION*
HEADPHONE_ON	0	Process the sound espacialy for Headphone. This option must be selected only if the TruSurround sound is redirected to the headphone output thanks to the HP channel matrix. 0: Standard mode for Loudspeaker output 1: Headphone mode for Headphone output only
TRUSRND_INPUT_MODE[3:0]	0000	0000: Mono on Center channel 0001: Mono on Left channel 0010: L/R stereo (SRS mode) 0011: L/R/S (SRS mode, Prologic 1 Process) 0100: L/R/Ls/Rs (SRS mode) 0101: L/R/C (TruSurround mode) 0110: L/R/C/S (TruSurround mode, Prologic 1 Process) 0111: L/R/C/Ls/Rs (TruSurround mode) 1000: Lt/Rt (TruSurround mode) 1001: L/R/C/Ls/Rs (SRS mode, BS Digital Broadcast) 1010: L/R/C/Ls/Rs (TruSurround, Prologic 2 Music mode)
TRUSRND_BYPASS	0	Bypass the TruSurround effect by applying a simple donwmix on input channels. 0: TruSurround mode 1: Bypass mode (downmix to 2 channels)
TRUSRND_ON	0	0: TruSurround OFF 1: TruSurround ON

TRUSRND_DC_ELEVATION Set Dialog Clarity Level

Address: B8h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRUSRND_DC_ELEVATION[7:0]							

Bit Name	Reset	Function
TRUSRND_DC_ELEVATION[7:0]	0000 1100	Dialog Clarity Elevation: 0000 0000: 0 dB 0000 0001: -0.5 dB ... 1111 1111: -127.5 dB

TRUSRND_INPUT_GAIN Input Gain for TruSurround

Address: B9h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRUSRND_INPUT_GAIN[7:0]							

Bit Name	Reset	Function
TRUSRND_INPUT_GAIN[7:0]	0000 0000	Input Gain attenuation: 0000 0000: 0 dB 0000 0001: -0.5 dB ... 1111 1111: -127.5 dB

TRUBASS_LS_CONTROL SRS TruBass for LS Configuration

Address: BAh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	TRUBASS_LS_SIZE[2:0]			TRUBASS_LS_ON

Bit Name	Reset	Function
Bits[7:3]	0000	Reserved.
TRUBASS_LS_SIZE[2:0]	011	000: LF response at 40 Hz 001: LF response at 60 Hz 010: LF response at 100 Hz 011: LF response at 150 Hz 100: LF response at 200 Hz 101: LF response at 250 Hz 110: LF response at 300 Hz 111: LF response at 400 Hz
TRUBASS_LS_ON	0	0: LS TruBass OFF 1: LS TruBass ON

TRUBASS_LS_LEVEL SRS TruBass for LS Level

Address: BBh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRUBASS_LS_LEVEL[7:0]							

Bit Name	Reset	Function
TRUBASS_LS_LEVEL[7:0]	0000 1001	Define the amount of SRS TruBass effect for LS outputs: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB

TRUBASS_HP_CONTROL SRS TruBass for HP Configuration

Address: BCh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRS_TSXT_GAIN_ON	0	0	0	TRUBASS_HP_SIZE[2:0]			TRUBASS_HP_ON

Bit Name	Reset	Function
SRS_TSXT_GAIN_ON	0	Apply the TruSurround Gain (register 0xB9) to the TruBass input block. This gain must be applied only if the TruSurround signal have been redirected to the TruBass HP thanks to the HP Channel Matrix. 0: TSXT input gain is not applied 1: TSXT input gain is applied. (this configuration must be used if the LS signal processed with TSXT is redirected to the HP channel)
Bits[6:3]	000	Reserved.
TRUBASS_HP_SIZE[2:0]	011	000: LF response at 40 Hz 100: LF response at 200 Hz 001: LF response at 60 Hz 101: LF response at 250 Hz 010: LF response at 100 Hz 110: LF response at 300 Hz 011: LF response at 150 Hz 111: LF response at 400 Hz
TRUBASS_HP_ON	0	0: HP TruBass OFF 1: HP TruBass ON

TRUBASS_HP_LEVEL SRS TruBass for HP Level

Address: BDh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRUBASS_HP_LEVEL[7:0]							

Bit Name	Reset	Function
TRUBASS_HP_LEVEL[7:0]	0000 1001	Define the amount of SRS TruBass effect for HP outputs: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB

SVC_LS_CONTROL Smart Volume Control for LS

Address: BEh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	SVC_LS_INPUT[1:0]		SVC_LS_AMP	SVC_LS_ON

Bit Name	Reset	Function
Bits[7:4]	0000	Reserved.
SVC_LS_INPUT[1:0]	00	Select input for peak detection in multichannel mode: 00: Left/Right 01: Center 10: Left/Right/Center 11: Not Used
SVC_LS_AMP	1	0: 0 dB amplification in auto-mode 1: +6 dB amplification in auto-mode
SVC_LS_ON	0	0: Manual mode(simple prescaler) 1: Automatic mode

SVC_LS_TIME_TH Smart Volume Control Parameters for LS

Address: BFh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SVC_LS_TIME[2:0]			SVC_LS_THRESHOLD[4:0]				

Bit Name	Reset	Function
SVC_LS_TIME[2:0]	100	Time Constant for Amplification (6-dB gain step) in Automatic mode: 000: 30 ms 100: 16 s 001: 200 ms 101: 32 s 010: 500 ms 110: 64 s 011: 1 s 111: 128 s
SVC_LS_THRESHOLD[4:0]	11000	See tables 8 and 9

Table 17: Gain (Threshold Field) Values in Manual mode

Manual Mode	Gain (dB)
00101	+15.5
00100	+12
00011	+9.5
00010	+6

Table 17: Gain (Threshold Field) Values in Manual mode (Continued)

Manual Mode	Gain (dB)
00001	+3.5
00000	0
11111	-2.5
11110	-6
11101	-8.5
11100	-12
11011	-14.5
11010	-18
11001	-20.5
11000	-24
10111	-26.5
10110	-30

Table 18: Threshold values in Automatic mode

Automatic Mode	Threshold (dB)
11111	-2.5
11110	-6
11101	-8.5
11100	-12
11011	-14.5
11010	-18
11001	-20.5
11000	-24
10111	-26.5
10110	-30

SVC_LS_GAIN Make-up Gain for SVC LS

Address: C0h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SVC_LS_GAIN[5:0]					

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.

Bit Name	Reset	Function
SVC_LS_GAIN[5:0]	000000	Set “make-up” gain applied at SVC LS output: 000000: +0 dB 000001: +0.5 dB ... 101110: +23 dB 101111: +23.5 dB 110000: +24 dB

SVC_HP_CONTROL Smart Volume Control for HP

Address: C1h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	SVC_HP_AMP	SVC_HP_ON

Bit Name	Reset	Function
Bits[7:2]	0000 00	Reserved.
SVC_HP_AMP	1	0: 0 dB amplification in auto-mode 1: +6 dB amplification in auto-mode
SVC_HP_ON	0	0: Manual mode (simple prescaler) 1: Automatic mode

SVC_HP_TIME_TH Smart Volume Control Parameters for HP

Address: C2h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SVC_HP_TIME[2:0]			SVC_HP_THRESHOLD[4:0]				

Bit Name	Reset	Function
SVC_HP_TIME[2:0]	100	Time Constant for Amplification (6-dB gain step) in Automatic mode: 000: 30 ms 100: 16 s 001: 200 ms 101: 32 s 010: 500 ms 110: 64 s 011: 1 s 111: 128 s
SVC_HP_THRESHOLD[4:0]	11000	See tables 8 and 9

SVC_HP_GAIN Make-up Gain for SVC HP

Address: C3h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SVC_HP_GAIN[5:0]					

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
SVC_HP_GAIN[5:0]	000000	Set “make-up” gain applied at SVC HP output: 000000: +0 dB 000001: +0.5 dB ... 101110: +23 dB 101111: +23.5 dB 110000: +24 dB

WIDESRND_CONTROL ST Wide Surround Control

Address: C4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	WIDESRND_STEREO	WIDESRND_MODE	WIDESRND_ON

Bit Name	Reset	Function
Bits[7:3]	00000	Reserved.
WIDESRND_STEREO	0	ST Wide Surround Sound Stereo Mode 0: ST Wide Surround Sound in Mono mode (Default) 1: ST Wide Surround Sound in Stereo mode
WIDESRND_MODE	0	ST Wide Surround Sound Stereo Mode 0: Movie Mode 1: Music Lode
WIDESRND_ON	0	ST Wide Surround Sound Enable 0: ST Wide Surround Sound is disabled 1: ST Wide Surround Sound is enabled

WIDESRND_FREQ ST Wide Surround Sound Frequency

Address: C5h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	WIDESRND_BASS[1:0]		WIDESRND_MEDIUM[1:0]		WIDESRND_TREBLE[1:0]	

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
WIDESRND_BASS[1:0]	01	Defines the bass frequency effect for ST Wide Surround Sound. Programmable values are listed in Table 10.
WIDESRND_MEDIUM[1:0]	01	Defines the medium frequency effect for ST Wide Surround Sound in Movie or Mono mode (no effect in Music mode). Programmable values are listed in Table 10.
WIDESRND_TREBLE[1:0]	01	Defines the treble frequency effect for ST Wide Surround Sound in Movie or Mono mode (no effect in Music mode). Programmable values are listed in Table 10.

Table 19: Phase Shifter Center Frequencies

	Phase Shifter Center Frequency		
	BASS_FREQ[1:0]	MEDIUM_FREQ[1:0]	TREBLE_FREQ[1:0]
00	40 Hz	202 Hz	2 kHz
01 (Default)	90 Hz	416 Hz	4 kHz
10	120 Hz	500 Hz	5 kHz
11	160 Hz	588 Hz	6 kHz

WIDESRND_LEVEL ST Wide Surround Gain

Address: C6h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WIDESRND_GAIN[7:0]							

Bit Name	Reset	Function			
WIDESRND_GAIN[7:0]	10000000	Defines the ST Wide Surround Sound component gain in linear scale.			
			Level (%)		Level (%)
		1000 0000 (Default)	100%	0000 0100	3.1%
		0111 1111	99.2%	0000 0011	2.3%
		0111 1110	98.4%	0000 0010	1.6%
		0111 1101	97.6%	0000 0001	0.8%
		.....		0000 0000	0%

OMNISURROUND_CONTROL ST Omnisurround Configuration

Address: C7h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ST_VOICE[1:0]		SRND_PHASE_INV	OMNISRND_INPUT_MODE[3:0]				OMNISRND_ON

Bit Name	Reset	Function
ST_VOICE[1:0]	00	00: OFF 01: Low 10: Mid 11: High
SRND_PHASE_INV	0	Invert Right Surround phase in 2_2 or 3_2 input mode: 0: Right Surround phase not inverted 1: Right Surround phase invertedl
OMNISRND_INPUT_ MODE[3:0]	0000	0000: Mono on center channel 0001: Mono on left channel 0010: L/R stereo 0011: L/R/S 0100: L/R/Ls/Rs 0101: L/R/C 0110: L/R/C/S 0111: L/R/C/Ls/Rs 1000: Lt/Rt (Passive matrix)
OMNISRND_ON	0	0: OmniSurround OFF 1: OmniSurround ON

DYNAMIC_BASS_LS ST Dynamic Bass for LS

Address: C8h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_BASS_LEVEL[4:0]					LS_BASS_FREQ[1:0]		LS_DYN_BAS S_ON

Bit Name	Reset	Function
LS_BASS_LEVEL [4:0]	00000	ST Dynamic Bass output gain: 00000: +0dB 00001: +0.5dB ... 11101: +14.5dB 11110: +15dB 11111: +15.5dB
LS_BASS_FREQ [1:0]	00	00: 100-Hz Cut-Off frequency 01: 150-Hz Cut-Off frequency 10: 200-Hz Cut-Off frequency 11: 250-Hz Cut-Off frequency
LS_DYN_BASS_O N	0	0: ST Dynamic Bass OFF 1: ST Dynamic Bass ON

DYNAMIC_BASS_HP ST Dynamic Bass for HP

Address: C9h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP_BASS_LEVEL[4:0]					HP_BASS_FREQ[1:0]		HP_DYN_BAS S_ON

Bit Name	Reset	Function
HP_BASS_LEVEL[4:0]	00000	ST Dynamic Bass output gain: 00000: +0dB 00001: +0.5dB ... 11101: +14.5dB 11110: +15dB 11111: +15.5dB
HP_BASS_FREQ[1:0]	00	00: 100-Hz Cut-Off frequency 10: 200-Hz Cut-Off frequency 01: 150-Hz Cut-Off frequency 11: 250-Hz Cut-Off frequency
HP_DYN_BASS_ON	0	0: ST Dynamic Bass OFF 1: ST Dynamic Bass ON

BASS_ENHANCE_LS ST Bass Enhancer for LS

Address: CAh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	LS_BASS_ENHANCE_HP_FILTER	LS_BASS_ENHANCE_SCALE[2:0]			LS_BASS_ENHANCE_CUTOFF	LS_BASS_ENHANCE_ON

Bit Name	Reset	Function
Bits[7:6]	00	Reserved.
LS_BASS_ENHANCE_HP_FILTER	0	Add an High Pass Filter in order to reduce the lower bass content in the signal in order to reduce the constraint on small speakers. 0: No High Pass Filter. To be used on wide band speakers 1: High Pass Filter. To be used on narrow band speakers.
LS_BASS_ENHANCE_SCALE[2:0]	000	Set the amount of bass generated by the processing: 000: Light Bass Content ... 111: Stong Bass Content
LS_BASS_ENHANCE_CUTOFF	0	Define the corner frequency for the bass generation: 0: Cuttoff Frequency = 80 Hz 1: Cutoff Frequency = 120 Hz
LS_DYN_BASS_ON	0	0: ST Bass Enhancer OFF 1: ST Bass Enhancer ON

EQ_BT_CTRL Loudspeakers Equalizer Control

Address: CCh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	HP_BT_ON	LS_EQ_BT_SW	LS_EQ_ON

Bit Name	Reset	Function
Bits[7:3]	00000	Reserved.
HP_BT_ON	0	Bass-Treble for HP Enable 0: Bass-Treble is disabled 1: Bass-Treble is enabled
LS_EQ_BT_SW	0	5-Band Equalizer or Bass-Teble for LS selection 0: 5-Band Equalizer is selected for Loudspeakers. 1: Bass-Treble is selected for Loudspeakers.
LS_EQ_ON	1	5-Band Equalizer/Bass-Treble for LS Enable 0: 5-Band Equalizer/Bass-Treble is disabled 1: 5-Band Equalizer/Bass-Treble is enabled

LS_EQ_BANDX Loudspeakers Equalizer Gain for BandX

Address: CDh to D1h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EQ_BANDX[7:0]							

Bit Name	Reset	Function
EQ_BANDX[7:0]	0000 0000	BandX gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB. Band1: 100 Hz, Band2: 330 Hz, Band3: 1 kHz, Band4: 3.3 kHz, Band5: 10 kHz.

Table 20: Loudspeakers Equalizer/Bass-Treble Gain Values (and Headphone Bass-Treble Gain Values)

Value	Gain G (dB)
00110000	+12
00101111	+11.75
00101110	+11.50
.....	.....
00000000 (Default)	0
.....	.....
10101110	-11.50
10101111	-11.75
10110000	-12

LS_BASS_GAIN Loudspeakers Bass Gain Register

Address: D2h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_BASS[7:0]							

Bit Name	Reset	Function
LS_BASS[7:0]	0000 0000	Gain Tuning of Loudspeakers Bass Frequency Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB. Programmable values are listed in Table 11.

LS_TREBLE_GAIN Loudspeakers Treble Gain Register

Address: D3h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_TREBLE							

Bit Name	Reset	Function
LS_TREBLE[7:0]	0000 0000	Gain Tuning of Loudspeakers Treble Frequency Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB. Programmable values are listed in Table 11.

HP_BASS_GAIN Headphone Bass Gain

Address: D4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP_BASS[7:0]							

Bit Name	Reset	Function
HP_BASS[7:0]	00000000	Gain Tuning of Headphone Bass Frequency Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB. Programmable values are listed in Table 11.

HP_TREBLE_GAIN Headphone Treble Gain

Address: D5h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP_TREBLE							

Bit Name	Reset	Function
HP_TREBLE[7:0]	0000 0000	Gain Tuning of Headphone Treble Frequency Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB. Programmable values are listed in Table 11.

OUTPUT_BASS_MNGT Bass Redirection

Address: D4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BASS_MANAGE_ON	ST_LFE_ADD	DOLBY_PROLOGIC	SUB_ACTIVE	GAIN_SWITCH	OCFG_NUM[2:0]		

Bit Name	Reset	Function
BASS_MANAGE_ON	0	0: BassManagement disabled 1: BassManagement enabled
ST_LFE_ADD	0	Add the signal comming from the LFE input (MULTI_I2S mode only) to the calculated Subwoofer signal: 0: No LFE channel to add 1: Add LFE signal to the Subwoofer computed signal
DOLBY_PROLOGIC	0	If the BassManagement is used with Dolby Prologic decoder, the surround channels must not be added to generate the Subwoofer channel: 0: Standard configuration (Dolby Digital compliant), surround channels are used to generate the Subwoofer channel. 1: Dolby Prologic configuration, surround channels are not used to generate the Subwoofer channel.
SUB_ACTIVE	0	In some configurations the Subwoofer signal can be redirected to L/R channels if there is no Subwoofer output:. 0: No Subwoofer output, the Sub signal is added to L/R channels 1: Subwoofer signal is outputed on Subwoofer output.
GAIN_SWITCH	0	Gain Switch available in some configurations: 0: Level Adjustment ON 1: Level Adjustment OFF

Bit Name	Reset	Function
OCFG_NUM[2:0]	000	Select Bass Management configuration: 000: Output Configuration 0 001: Output Configuration 1 010: Output Configuration 2 011: Output Configuration 3 100: Output Configuration 4 (Simplified Configuration) 101: Output Configuration 5 (Stereo Full Bandwith Speakers) 110: Output Configuration 6 (Stereo Narrow Bandwith Speakers) 111: Not Used

LS_LOUDNESS Loudness Configuration for LS

Address: D7h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	LS_LOUD_THRESHOLD[2:0]			LS_LOUD_GAIN_HR[2:0]			LS_LOUD_ON

Bit Name	Reset	Function
Bit 7	0	Reserved.
LS_LOUD_THRESHOLD[2:0]	000	Define the volume threshold level since which loudness effect is applied: 000: 0 dB 100: -24 dB 001: -6 dB 101: -32 dB 010: -12 dB 110: -36 dB 011: -18 dB 111: -42 dB
LS_LOUD_GAIN_HR[2:0]	010	Define the amount of Treble added by loudness effect: 000: 0 dB 100: 12 dB 001: 3 dB 101: 15 dB 010: 6 dB 110: 18 dB 011: 9 dB 111: Not Used
LS_LOUD_ON	0	0: Loudness is not active on LS output 1: Loudness is active on LS output

HP_LOUDNESS Loudness Configuration for HP

Address: D8h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	HP_LOUD_THRESHOLD[2:0]			HP_LOUD_GAIN_HR[2:0]			HP_LOUD_ON

Bit Name	Reset	Function
Bit 7	0	Reserved.

Bit Name	Reset	Function
HP_LOUD_THRESHOLD[2:0]	000	Define the volume threshold level since which loudness effect is applied : 000: 0 dB 100: -24 dB 001: -6 dB 101: -32 dB 010: -12 dB 110: -36 dB 011: -18 dB 111: -42 dB
HP_LOUD_GAIN_HR[2:0]	010	Define the amount of Treble added by loudness effect: 000: 0 dB 100: 12 dB 001: 3 dB 101: 15 dB 010: 6 dB 110: 18 dB 011: 9 dB 111: not used
HP_LOUD_ON	0	0: Loudness is not active on HP output 1: Loudness is active on HP output

VOLUME_MODES Set the Volume Modes

Address: D9h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ANTICLIP_HP_VOL_CLAMP	ANTICLIP_LS_VOL_CLAMP	0	SCART2_VOLUME_MODE	SCART1_VOLUME_MODE	HP_VOLUME_MODE	SRND_VOLUME_MODE	LS_VOLUME_MODE

Bit Name	Reset	Function
ANTICLIP_HP_VOL_CLAMP	1	The output level is clamped depending on the HP Bass-Treble value to avoid any possible signal clipping on HP output. 0: Volume clamp on HP output is not active 1: Volume clamp on HP output is active
ANTICLIP_LS_VOL_CLAMP	1	The output level is clamped depending on the LS Equalizer or LS Bass-Treble value to avoid any possible signal clipping on LS output. 0: Volume clamp on LS output is not active 1: Volume clamp on LS output is active
Bits[5]	0	Reserved.
SCART2_VOLUME_MODE	1	Volume mode for SCART2 output: 0: Independant 1: Differential
SCART1_VOLUME_MODE	1	Volume mode for SCART1 output: 0: Independant 1: Differential
HP_VOLUME_MODE	1	Volume mode for Headphone output: 0: Independant 1: Differential
SRND_VOLUME_MODE	1	Volume mode for Surround output: 0: Independant 1: Differential

Bit Name	Reset	Function
LS_VOLUME_ MODE	1	Volume mode for LS output: 0: Independant 1: Differential

LS_L_VOLUME_MSB Loudspeaker Left Volume MSB

Address: DAh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_L_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_L_VOLUME_M SB[7:0]	1001 1000	8 MSBs of the 10-bit Left Loudspeaker Volume

LS_L_VOLUME_LSB Loudspeaker Left Volume LSB

Address: DBh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_L_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
LS_L_VOLUME_LS B[1:0]	00	2 LSBs of the 10-bit Left Loudspeaker Volume

LS_R_VOLUME_MSB Loudspeaker Right Volume MSB

Address: DCh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_R_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_R_VOLUME_M SB[7:0]	0000 0000	8 MSBs of the 10-bit Right Loudspeaker Volume

LS_R_VOLUME_LSB Loudspeaker Right Volume LSB

Address: DDh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_R_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
LS_R_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Right Loudspeaker Volume

LS_C_VOLUME_MSB Loudspeaker Center Volume MSB

Address: DEh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_C_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_C_VOLUME_MSB[7:0]	1001 1000	8 MSBs of the 10-bit Center Loudspeaker Volume

LS_C_VOLUME_LSB Loudspeaker Center Volume LSB

Address: DFh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_C_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	0000 00	Reserved.
LS_C_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Center Loudspeaker Volume

LS_SUB_VOLUME_MSB Loudspeaker Subwoofer Volume MSB

Address: E0h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_SUB_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_SUB_VOLUME_MSB[7:0]	1001 1000	8 MSBs of the 10-bit Subwoofer Loudspeaker Volume

LS_SUB_VOLUME_LSB Loudspeaker Subwoofer Volume LSB

Address: E1h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_SUB_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
LS_SUB_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Subwoofer Loudspeaker Volume

LS_SL_VOLUME_MSB Loudspeaker Left Surround Volume MSB

Address: E2h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_SL_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_SL_VOLUME_MSB[7:0]	1001 1000	8 MSBs of the 10-bit Left Surround Loudspeaker Volume

LS_SL_VOLUME_LSB Loudspeaker Surround Left Volume LSB

Address: E3h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_SL_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
LS_SL_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Left Surround Loudspeaker Volume

LS_SR_VOLUME_MSB Louspeaker Surround Right Volume MSB

Address: E4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_SR_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_SR_VOLUME_MSB[7:0]	0000 0000	8 MSBs of the 10-bit Right Surround Loudspeaker Volume

LS_SR_VOLUME_LSB Loudspeaker Surround Right Volume LSB

Address: E5h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_SR_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
LS_SR_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Right Surround Loudspeaker Volume

LS_MASTER_VOLUME_MSB Loudspeaker Master Volume MSB

Address: E6h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS_MASTER_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
LS_MASTER_ VOLUME_MSB[7:0]	1110 1000	8 MSBs of the 10-bit Master Loudspeaker Volume

LS_MASTER_VOLUME_LSB Loudspeaker Master Volume LSB

Address: E7h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	LS_MASTER_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
LS_MASTER_VOL UME_LSB[1:0]	00	2 LSBs of the 10-bit Master Loudspeaker Volume

HP_L_VOLUME_MSB Headphone Left Volume MSB

Address: E8h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP_L_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
HP_L_VOLUME_M SB[7:0]	1001 1000	8 MSBs of the 10-bit Left Headphone Volume

HP_L_VOLUME_LSB Headphone Left Volume LSB

Address: E9h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	HP_L_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
HP_L_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Left Headphone Volume

HP_R_VOLUME_MSB Headphone Right Volume MSB

Address: EAh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP_R_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
HP_R_VOLUME_MSB[7:0]	00000000	8 MSBs of the 10-bit Right Headphone Volume

HP_R_VOLUME_LSB Headphone Right Volume LSB

Address: EBh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	HP_R_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
HP_R_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Right Headphone Volume

AUX_VOLUME_INDEX Select the AUX to apply Volume

Address: ECh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	AUX_VOLUME_SELECT[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
AUX_VOLUME_SELECT[1:0]	00	Select the output on which the AUX_VOLUME values will be applied: 00: No volume applied (*mandatory step to change selection from 01 to 10*) 01: Volume applied to SCART1 output 10: Volume applied to SCART2 output 11: Not used

AUX_L_VOLUME_MSB Auxiliary Left Volume MSB

Address: EDh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX_L_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
AUX_L_VOLUME_MSB[7:0]	1001 1000	8 MSBs of the 10-bit Left Auxiliary Volume

AUX_L_VOLUME_LSB Auxiliary Left Volume LSB

Address: EEh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	AUX_L_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
AUX_L_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Left Auxiliary Volume

AUX_R_VOLUME_MSB Auxiliary Right Volume MSB

Address: EFh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX_R_VOLUME_MSB[7:0]							

Bit Name	Reset	Function
AUX_R_VOLUME_MSB[7:0]	0000 0000	8 MSBs of the 10-bit Right Auxiliary Volume

AUX_R_VOLUME_LSB Auxiliary Right Volume LSB

Address: F0h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	AUX_R_VOLUME_LSB[1:0]	

Bit Name	Reset	Function
Bits[7:2]	000000	Reserved.
AUX_R_VOLUME_LSB[1:0]	00	2 LSBs of the 10-bit Right Auxiliary Volume

12.15 Mute

MUTE_SOFTWARE Soft Mute Output by DSP

Address: F1h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HP_D_MUTE	SPDIF_D_MUTE	SCART2_D_MUTE	SCART1_D_MUTE	SRND_D_MUTE	SUB_D_MUTE	C_D_MUTE	LS_D_MUTE

Bit Name	Reset	Function
HP_D_MUTE	1	Digital Soft Mute for HP output: 0: Soft Mute not active 1: Soft Mute active
SPDIF_D_MUTE	1	Digital Soft Mute for SPDIF output: 0: Soft Mute not active 1: Soft Mute active

Bit Name	Reset	Function
SCART2_D_MUTE	1	Digital Soft Mute for SCART2 output: 0: Soft Mute not active 1: Soft Mute active
SCART1_D_MUTE	1	Digital Soft Mute for SCART1 output: 0: Soft Mute not active 1: Soft Mute active
SRND_D_MUTE	1	Digital Soft Mute for SURROUND output: 0: Soft Mute not active 1: Soft Mute active
SUB_D_MUTE	1	Digital Soft Mute for SUBWOOFER output: 0: Soft Mute not active 1: Soft Mute active
C_D_MUTE	1	Digital Soft Mute for CENTER output: 0: Soft Mute not active 1: Soft Mute active
LS_D_MUTE	1	Digital Soft Mute for LOUDSPEAKER output: 0: Soft Mute not active 1: Soft Mute active

12.16 Beeper

BEEPER_ON **Set Beeper On**

Address: F2h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	BEEPER_SOUND_SELECT[1:0]		BEEPER_ON

Bit Name	Reset	Function
Bits[7:3]	00000	Reserved.
BEEPER_SOUND_SELECT[1:0]	00	Select the kind of sound generated by the beeper when BEEPER_ON is set to 1: 00: Square Wave Signal. Frequency and Decay can be set in Register 0xf4. 01: Wood Block Natural Sound 10: Clic Natural Sound 11: Bleep Natural Sound.
BEEPER_ON	0	Control Beeper Sound Start/Stop: 0: Start Beeper 1: Stop Beeper

Note: if BEEPER_SOUND_SELECT = 0 and BEEPER_CONTINUOUS(reg 0xF3) is set to 1, the BEEPER_ON needs to be set to 0 to stop the beeper sound ; otherwise, the beeper is stopped automaticaly.

On beeper STOP, the register 0xF2 is reset to 0. Take care to set bit[2:1] on each BEEPER_ON action.

BEEPER_MODE Beeper Control

Address: F3h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BEEPER_DECAY[2:0]			BEEPER_DURATION[1:0]		BEEPER_CONTINUOUS	BEEPER_PATH	

Bit Name	Reset	Function
BEEPER_DECAY [2:0]	000	Control the decay of the envelope of the Beeper sound: 000: Short Decay (sounds dry) ... 111: Very Long Decay (sounds wet)
BEEPER_DURATION [1:0]	00	Define Beeper Duration when BEEPER_CONTINUOUS is set to 0: 00: 0.1 sec. 01: 0.25 sec. 10: 0.5 sec. 11: 1 sec.
BEEPER_CONTINUOUS	0	Set Beeper Pulse Mode 0: Pulse mode selected, the BEEPER_ON is automaticaly reset to 0. 1: Continuous mode selected, the BEEPER_ON must be set to 0 to stop the beeper sound.
BEEPER_PATH [1:0]	11	Set the output channels when beeper is active 00: no channels. 01: Loudspeakers only. 10: Headphone only. 11: Loudspeakers and Headphone selected.

BEEPER_FREQ_VOL Beeper Frequency and Volume Settings

Address: F4h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BEEP_FREQ[2:0]			BEEP_VOL[4:0]				

Bit Name	Reset	Function
BEEP_FREQ[2:0]	011	Defines the frequency of the beeper tone from 62.5 Hz to 8 kHz in octaves 000: 62.5 Hz 100: 1 kHz 001: 125 Hz 101: 2 kHz 010: 250 Hz 110: 4 kHz 011: 500 Hz (Default) 111: 8 kHz

Bit Name	Reset	Function
BEEP_VOL[4:0]	10000	Defines the Beeper volume from 0 to -93 dB in steps of 3 dB. 11111: 0 dB (1 V_{RMS}) ... 11110: -3 dB 00011: -84 dB 11101: -6 dB 00010: -87 dB ... 00001: -90 dB 10000: -48 dB (Default) 00000: -93 dB

12.17 SPDIF Output Configuration

SPDIF_OUT_CHANNEL_STATUS

Address: F5h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	SPDIF_COPYRIGHT	SPDIF_NO_PCM	SPDIF_CONSUMER_PRO

Bit Name	Reset	Function
Bits[7:3]	00000	Reserved.
SPDIF_COPYRIGHT	0	0: Copyright 1: No Copyright
SPDIF_NO_PCM	0	0: PCM Format 1: No PCM Format
SPDIF_CONSUMER_PRO	0	0: Consumer Format 1: Professional Format

12.18 Headphone Configuration

HEADPHONE_CONFIG Headphone Configuration

Address: F6h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	KARAOKE_MIX	SCART2_OUT_SELECT[1:0]		HP_FORCE	HP_LS_MUTE	HP_DET_ACTIVE	HP_DETECTED

Bit Name	Reset	Function
Bits [7]	0	Reserved.
KARAOKE_MIX	0	When set, mix the HP channel signal with the LS channel signal. The mixed signal is output on the LS channel.

Bit Name	Reset	Function
SCART2_OUT_SELECT[1:0]	00	Select SCART2 output: 00: SCART2 not output 01: SCART2 signal output on C/Sub DAC 10: SCART2 signal output on Srnd/HP DAC 11: not used
HP_FORCE	0	1: force to output the HP signal (bypass surround) *Note: when HP is forced, IRQ5 and HP/Srnd DAC automatic mute are not active.*
HP_LS_MUTE	0	0: when HP is detected and active, LS are not muted 1: when HP is detected and active, LS are muted
HP_DET_ACTIVE	1	0: HP detection is not active 1: HP detection is active, when HP detected, Surround signal is bypassed and HP signal is outputed on HP
HP_DETECTED	0	1: When a signal is detected on HP_DET pin

12.19 DAC Control

DAC_CONTROL DAC Control Register

Address: F7h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	SPDIF_MUX	DAC_SCART_MUTE	DAC_SHP_MUTE	DAC_CSUB_MUTE	DAC_LSLR_MUTE	POWER_UP

Bit Name	Reset	Function
Bits [7:6]	00	Reserved.
SPDIF_MUX	0	Redirect external or internal source i2s to i2s output : 0: Internal I²S 1: External I²S
DAC_SCART_MUTE	1	SCART Left/Right Analog Soft Mute 0: Soft Mute not active 1: Soft Mute active
DAC_SHP_MUTE	1	Surround/HP Left/Right Analog Soft Mute 0: Soft Mute not active 1: Soft Mute active
DAC_CSUB_MUTE	1	Center/Subwoofer Analog Soft Mute 0: Soft Mute not active 1: Soft Mute active
DAC_LSLR_MUTE	1	LS Left/Right Analog Soft Mute 0: Soft Mute not active 1: Soft Mute active
POWER_UP	1	0: DACs Power OFF 1: Power ON

DAC_SW_CHANNELS DAC SW Channel Register

Address: F8h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C_SUB_SW		SUR_HP_SW		SCART_SW		SPDIF_SW	

Bit Name	Reset	Function
C_SUB_SW	00	Center/Sub DAC: 00: Left/Right channels inverted 11: Left/Right channels non inverted
SUR_HP_SW	00	Surround/HP DAC: 00: Left/Right channels inverted 11: Left/Right channels non inverted
SCART_SW	00	SCART DAC: 00: Left/Right channels inverted 11: Left/Right channels non inverted
SPDIF_SW	00	SPDIF: 00: Left/Right channels inverted 11: Left/Right channels non inverted

SPDIF_SW_CHANNELS SPDIF SW Channel Register

Address: F9h

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	DELAY_SW		LS_L_R_SW	

Bit Name	Reset	Function
Bits [7:4]	0000	Reserved.
DELAY_SW	00	Delay output: 00: Left/Right channels inverted 11: Left/Right channels non inverted
LS_L_R_SW	00	Loudspeaker L/R output: 00: Left/Right channels inverted 11: Left/Right channels non inverted

12.20 AutoStandard Coefficients Settings

AUTOSTD_COEFF_CTRL Autostd Control Register Coefficients

Address: FBh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	AUTOSTD_COEFF_CTRL[1:0]	

Bit Name	Reset	Function
Bits [7:2]	000000	Reserved.
AUTOSTD_COEFF_CTRL[1:0]	01	Control the Demod filter coeff table settings 01: init Coeffs to ROM values 10: Update Coeffs with I2C value

AUTOSTD_COEFF_INDEX_MSB

Address: FCh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	AUTOSTD_COEFF_INDEX_MSB

Bit Name	Reset	Function
Bits [7:2]	0000000	Reserved.
AUTOSTD_COEFF_INDEX_MSB	0	FIR Coefficients table index (MSB)

AUTOSTD_COEFF_INDEX_LSB

Address: FDh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTOSTD_COEFF_INDEX_LSB[7:0]							

Bit Name	Reset	Function
AUTOSTD_COEFF_INDEX_LSB[7:0]	0000 0000	FIR Coefficients table index (LSB)

AUTOSTD_COEFF_VALUE

Address: FEh

Type: R/W

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUTOSTD_COEFF_VALUE[7:0]							

Bit Name	Reset	Function
AUTOSTD_COEFF_VALUE[7:0]	0000 0000	FIR Coefficients table value to update

13 Pin Descriptions

13.1 TQFP 80-pin Package

- AP = Analog Power
- DP = Digital Power
- I = Input
- O = Output
- OD = Open-Drain
- B = Bi-Directional
- A = Analog

Table 21: TQFP80 Pin Description (Sheet 1 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8 (Function for STV82x6 in italic characters)	STV82x6 Pin Name
1	SC1_OUT_L	A	SCART1 Audio Output Left	AO1L
2	SC1_OUT_R	A	SCART1 Audio Output Right	AO1R
3	VCC_H	AP	8V Power for Audio I/O & ESD	*Not connected*
4	GND_H	AP	High Current Ground for Audio Outputs	*Connected to Ground*
5	SC3_OUT_L	A	SCART3 Audio Output Left	*Not connected*
6	SC3_OUT_R	A	SCART3 Audio Output Right	*Not connected*
7	VCC33_SC	AP	3.3V Power for Audio Buffers & DAC / ADC	VDDC
8	GND33_SC	AP	Ground for Audio Buffers & DAC / ADC	GNDC
9	SC1_IN_L	A	SCART1 Audio Input Left	AI1L
10	SC1_IN_R	A	SCART1 Audio Input Right	AI1R
11	VREFA	A	Audio Bias Voltage Decoupling 1.55V *(Switched V_{REF} decoupling pin for Audio Converters (VMCP))*	VMC1
12	NC (GND_SA in STV82x7)	AP		*Connected to Ground*
13	VBG	A	Bandgap Voltage Reference Decoupling 1.2V *(V_{REF} decoupling pin for Audio Converters (VMC))*	VMC2
14	SC2_IN_L	A	SCART 2 Audio Input Left	AI2L
15	SC2_IN_R	A	SCART 2 Audio Input Right	AI2R
16	VCC33_LS	AP	3.3V Power for Audio DACs *(3.3V Power Supply for Audio Buffers and SCART)*	VDDA
17	GND33_LS	AP	Ground for Audio DACs *(Ground for Audio Buffers and SCART)*	GNDAH
18	SC2_OUT_L	A	SCART 2 Audio Output Left	AO2L
19	SC2_OUT_R	A	SCART 2 Audio Output Right	AO2R
20	GND_SA (VCC_NISO in STV82x7)	AP	Ground for DACs	VDDH

Table 21: TQFP80 Pin Description (Sheet 2 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8 (Function for STV82x6 in italic characters)	STV82x6 Pin Name
21	VSS33_CONV	AP	Ground for DAC 1.8 to 3.3V Converters	*Connected to Ground*
22	VDD33_CONV	AP	3.3V Power for DAC 1.8 to 3.3V Converters *(Voltage Reference for Audio buffers)*	VREFA
23	SC3_IN_L	A	SCART 3 Audio Input Left	AI3L
24	SC3_IN_R	A	SCART 3 Audio Input Right	AI3R
25	SCL_FLT	A	SCART Filtering Left	*Not connected*
26	SCR_FLT	A	SCART Filtering Right *(Bandgap Voltage Source Decoupling)*	BGAP
27	LS_C	A	Center Output	*Not connected*
28	LS_L	A	Left Loudspeaker Output	LSL
29	LS_R	A	Right Loudspeaker Output	LSR
30	LS_SUB	A	Subwoofer Output	SW
31	HP_LSS_L	A	Left Headphone Output or Left Surround Output	HPL
32	HP_LSS_R	A	Right Headphone Output or Right Surround Output	HPR
33	VSS18_CONV	DP	Ground for Digital part of the DAC/ADC *(Substrate Analog/Digital Shield)*	GNDSA
34	VDD18_CONV	DP	1.8V Power for Digital part of the DAC/ADC	*Not connected*
35	$\overline{\text{HP\_DET}}$	I	Headphone Detection	$\overline{\text{HPD}}$
36	ADR_SEL	I	Hardware Address selection for I²C Bus	ADR
37	VSS18	DP	Ground for Digital part	*Connected to Ground*
38	VDD18	DP	1.8V Power for Digital part	*Not connected*
39	SCL	OD	I²C Clock Input	SCL
40	SDA	OD	I²C Data I/O	SDA
41	VSS18	DP	Ground for Digital part	*Connected to Ground*
42	VDD18	DP	1.8V Power for Digital part *(5V Power Regulator Control)*	REG
43	$\overline{\text{RST\_N}}$	I	Main Reset Input	$\overline{\text{RESET}}$
44	S/PDIF_IN	I	Serial Audio Data Input *(System Clock output)*	SYSCK
45	S/PDIF_OUT	O	Serial Audio Data Output *(I²S Master Clock output)*	MCK
46	VDD33_IO1	DP	3.3V power for Digital IO	VDD1
47	VSS33_IO1	DP	Ground for Digital IO	GND1
48	CK_TST_CTRL	D	To be Grounded	*Not connected*
49	VSS18	DP	Ground for Digital part	GNDSP
50	VDD18	DP	1.8V Power for Digital part	*Not connected*
51	CLK_SEL	I	Clock Input Format Selection	*Not connected*

Table 21: TQFP80 Pin Description (Sheet 3 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8 (Function for STV82x6 in italic characters)	STV82x6 Pin Name
52	XTALIN_CLKXTP	I	Crystal Oscillator Input or Differential Input Positive *(Crystal Oscillator Input)*	XTI
53	XTALOUT_CLKXTM	O	Crystal Oscillator Output or Differential Input Negative *(Crystal Oscillator Output)*	XTO
54	VCC18_CLK1	AP	1.8V Power for Clock PLL Analog & Crystal Oscillator 1/2 *(3.3V Power supply for Analog PLL Clock)*	VDDP
55	GND18_CLK1	AP	Ground for Clock PLL Analog & Crystal Oscillator 1/2	GNDP
56	GND18_CLK2	AP	Ground for Clock PLL Digital 1/2	GND2
57	VCC18_CLK2	DP	1.8V Power for Clock PLL Digital 1/2 *(3.3V Power supply for Digital core, DSPs & IO Cells)*	VDD2
58	VSS33_IO2	DP	Ground for Digital IO	*Connected to Ground*
59	VDD33_IO2	DP	3.3V power for Digital IO	*Not connected*
60	I2S_PCM_CLK	I/O	I²S Master Clock Input/Output Channel 0, 1 & 2	*Not connected*
61	I2S_SCLK	I/O	I²S Serial Clock Input/Output Channel 0, 1& 2 (I²S bus data output)	SDO
62	I2S_LR_CLK	I/O	I²S Word Select Input/Output Channel 0 , 1 & 2 *(Stereo Detection output / I²S Bus Data input)*	ST/SDI
63	I2S_DATA0	I/O	I²S Data Input/Output Stereo Channel 0 *(I²S Bus Word Select output)*	WS
64	I2S_DATA1	I	I²S Data Input Stereo Channel 1 *(I²S Bus Clock output)*	SCK
65	I2S_DATA2	I	I²S Data Input Stereo Channel 2 *(Bus Expander Output 1)*	BUS1
66	VDD18	DP	1.8V Power for Digital Core & I/O Cells Pin	*Not connected*
67	VSS18	DP	Ground for Digital Core & I/O Cells Pin	*Connected to Ground*
68	BUS_EXP	O	Bus Expander Function *(Bus Expander Output 2)*	BUS0
69	IRQ	O	Interrupt Request to Microprocessor	IRQ
70	GND_PSUB	AP	Ground Substrate Connection	*Connected to Ground*
71	VDD18_ADC	DP	VDD 1.8V for ADC (Digital Part)	*Not connected*
72	VSS18_ADC	DP	Ground to Complement 1.8V VDD for ADC	*Connected to Ground*
73	SIF_P	A	Sound IF input	SIF
74	SIF_N	A	ADC V_{TOP} Decoupling pin	VTOP
75	GNDPW_IF	AP	Polarization for the IF block *(Voltage Reference for AGC Decoupling pin)*	VREFIF
76	VCC18_IF	AP	1.8V Power for IF AGC & ADC	VDDIF
77	GND18_IF	AP	Ground for IF AGC & ADC	GNDIF
78	MONO_IN	A	Mono Input (for AM Mono)	MONOIN
79	SC4_IN_L	A	SCART4 Audio Input Left	*Not connected*

Table 21: TQFP80 Pin Description (Sheet 4 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8 (Function for STV82x6 in italic characters)	STV82x6 Pin Name
80	SC4_IN_R	A	SCART4 Audio Input Right	*Not connected*

13.2 TQFP 100-pin Package

- AP = Analog Power
- DP = Digital Power
- I = Input
- O = Output
- OD = Open-Drain
- B = Bi-Directional
- A = Analog

Table 22: TQFP100 Pin Description (Sheet 1 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8
1	SC1_OUT_L	A	SCART1 Audio Output Left
2	SC1_OUT_R	A	SCART1 Audio Output Right
3	VCC_H	AP	8V Power for Audio I/O & ESD
4	GND_H	AP	High Current Ground for Audio Outputs
5	SC3_OUT_L	A	SCART3 Audio Output Left
6	SC3_OUT_R	A	SCART3 Audio Output Right
7	VCC33_SC	AP	3.3V Power for Audio Buffers & DAC / ADC
8	GND33_SC	AP	Ground for Audio Buffers & DAC / ADC
9	SC1_IN_L	A	SCART1 Audio Input Left
10	SC1_IN_R	A	SCART1 Audio Input Right
11	VREFA	A	Audio Bias Voltage Decoupling 1.55V
12	VBG	A	Bandgap Voltage Reference Decoupling 1.2V
13	SC2_IN_L	A	SCART 2 Audio Input Left
14	SC2_IN_R	A	SCART 2 Audio Input Right
15	VCC33_LS	AP	3.3V Power for Audio DACs
16	GND33_LS	AP	Ground for Audio DACs
17	SC2_OUT_L	A	SCART 2 Audio Output Left
18	SC2_OUT_R	A	SCART 2 Audio Output Right
19	SC5_IN_L	A	SCART 5 Audio Input Left
20	SC5_IN_R	A	SCART 5 Audio Input Right
21	NC		

Table 22: TQFP100 Pin Description (Sheet 2 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8
22	NC		
23	GND_SA	AP	Ground for DACs
24	NC		
25	NC		
26	VSS33_CONV	AP	Ground for DAC 1.8 to 3.3V Converters
27	VDD33_CONV	AP	3.3V Power for DAC 1.8 to 3.3V Converters
28	SC3_IN_L	A	SCART 3 Audio Input Left
29	SC3_IN_R	A	SCART 3 Audio Input Right
30	SCL_FLT	A	SCART Filtering Left
31	SCR_FLT	A	SCART Filtering Right
32	LS_C	A	Center Output
33	NC		
34	LS_L	A	Left Loudspeaker Output
35	NC		
36	LS_R	A	Right Loudspeaker Output
37	NC		
38	LS_SUB	A	Subwoofer Output
39	NC		
40	HP_LSS_L	A	Left Headphone Output or Left Surround Output
41	NC		
42	HP_LSS_R	A	Right Headphone Output or Right Surround Output
43	NC		
44	NC		
45	VSS18_CONV	DP	Ground for Digital part of the DAC/ADC
46	VDD18_CONV	DP	1.8V Power for Digital part of the DAC/ADC
47	$\overline{\text{HP\_DET}}$	I	Headphone Detection
48	ADR_SEL	I	Hardware Address selection for I²C Bus
49	VSS18	DP	Ground for Digital part
50	VDD18	DP	1.8V Power for Digital part
51	SCL	OD	I²C Clock Input
52	SDA	OD	I²C Data I/O
53	$\overline{\text{RST\_N}}$	I	Main Reset Input
54	I2SD_DATA	I	I²S Data Delay Input Stereo Channel
55	I2SO_DATA1	O	I²S Data Output Stereo Channel O_1

Table 22: TQFP100 Pin Description (Sheet 3 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8
56	I2SO_LR_CLK	O	I²S Word Select Output Channel O_0 & O_1
57	I2SO_SCLK	O	I²S Serial Clock Output Channel O_0 & O_1
58	I2SO_DATAO	O	I²S Data Output Stereo Channel O_0
59	S/PDIF_IN	I	Serial Audio Data Input
60	S/PDIF_OUT	O	Serial Audio Data Output
61	VDD33_IO1	DP	3.3V power for Digital IO
62	VSS33_IO1	DP	Ground for Digital IO
63	CK_TST_CTRL	D	To be Grounded
64	VSS18	DP	Ground for Digital part
65	VDD18	DP	1.8V Power for Digital part
66	CLK_SEL	I	Clock Input Format Selection
67	XTALIN_CLKXTP	I	Crystal Oscillator Input or Differential Input Positive
68	XTALOUT_CLKXTM	O	Crystal Oscillator Output or Differential Input Negative
69	VCC18_CLK1	AP	1.8V Power for Clock PLL Analog & Crystal Oscillator 1/2
70	GND18_CLK1	AP	Ground for Clock PLL Analog & Crystal Oscillator 1/2
71	GND18_CLK2	AP	Ground for Clock PLL Digital 1/2
72	VCC18_CLK2	DP	1.8V Power for Clock PLL Digital 1/2
73	VSS33_IO2	DP	Ground for Digital IO
74	VDD33_IO2	DP	3.3V power for Digital IO
75	I2S_PCM_CLK	I/O	I²S Master Clock Input/Output Channel 0, 1 & 2
76	I2S_SCLK	I/O	I²S Serial Clock Input/Output Channel 0, 1 & 2
77	I2S_LR_CLK	I/O	I²S Word Select Input/Output Channel 0,1 & 2
78	I2S_DATA0	I/O	I²S Data Input/Output Stereo Channel 0
79	I2S_DATA1	I	I²S Data Input Stereo Channel 1
80	I2S_DATA2	I	I²S Data Input Stereo Channel 2
81	NC		
82	I2SA_SCLK	I	I²S Serial Clock Input Channel Auxiliary
83	I2SA_LR_CLK		I²S Word Select Input Channel Auxiliary
84	I2SA_DATA		I²S Data Input Stereo Channel Auxiliary
85	VDD18	DP	1.8V Power for Digital Core & I/O Cells Pin
86	VSS18	DP	Ground for Digital Core & I/O Cells Pin
87	BUS_EXP	O	Bus Expander Function
88	IRQ	O	Interrupt Request to Microprocessor
89	GND_PSUB	AP	Ground Substrate Connection

Table 22: TQFP100 Pin Description (Sheet 4 of 4)

Pin No.	STV82x8 Pin Name	Type (STV82x8)	Function for STV82x8
90	VDD18_ADC	DP	VDD 1.8V for ADC (Digital Part)
91	VSS18_ADC	DP	Ground to Complement 1.8V VDD for ADC
92	SIF_P	A	Sound IF input 1
93	SIF_N	A	ADC V_{TOP} Decoupling pin
94	SIF2_P	A	Sound IF input 2
95	GNDPW_IF	AP	Polarization for the IF block
96	VCC18_IF	AP	1.8V Power for IF AGC & ADC
97	GND18_IF	AP	Ground for IF AGC & ADC
98	MONO_IN	A	Mono Input (for AM Mono)
99	SC4_IN_L	A	SCART 4 Audio Input Left
100	SC4_IN_R	A	SCART 4 Audio Input Right

14 Application Diagrams

Figure 31: STV82x8 TQFP80 Application Diagram

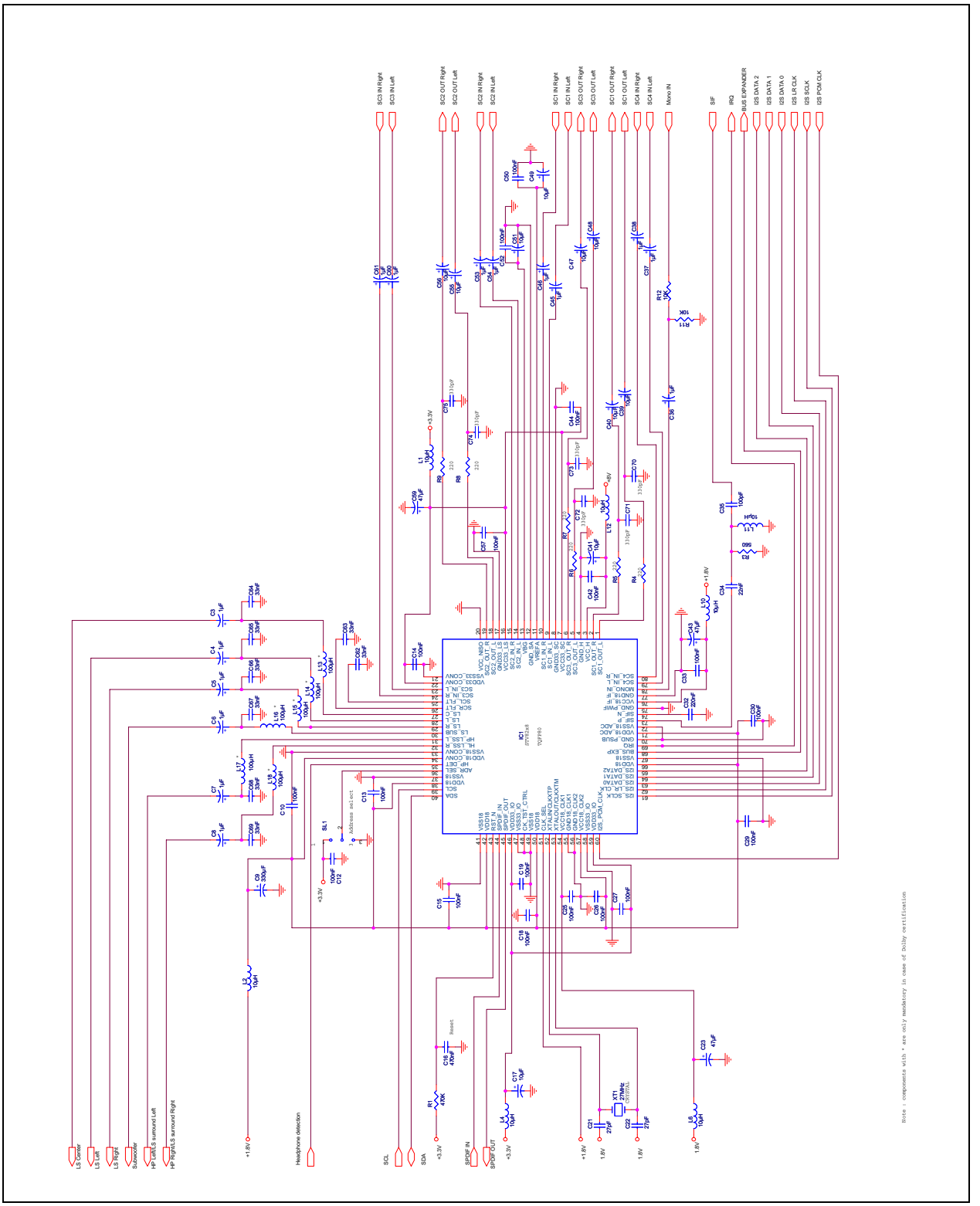


Figure 32: STV82x8 TQFP100 Application Diagram

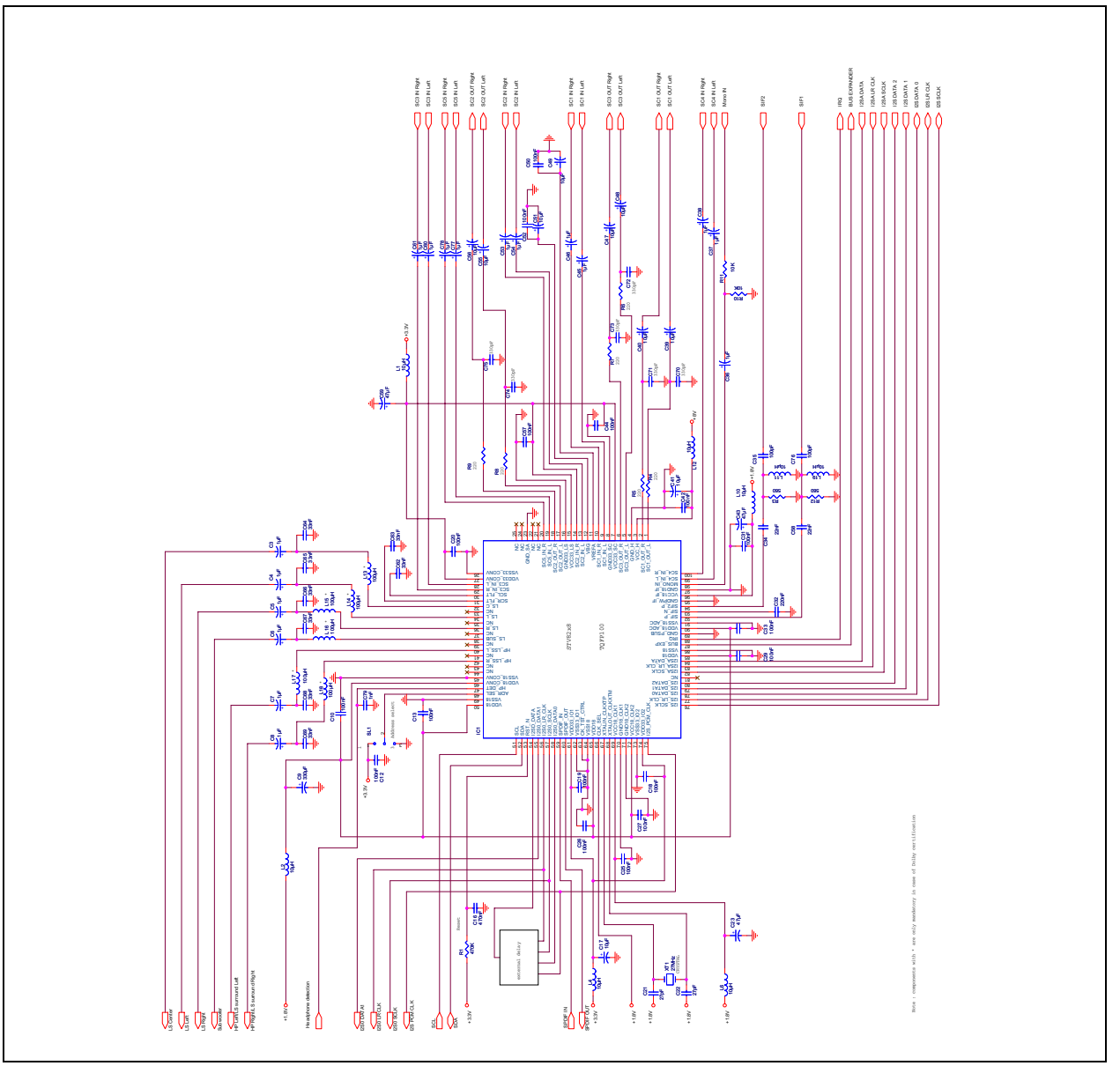
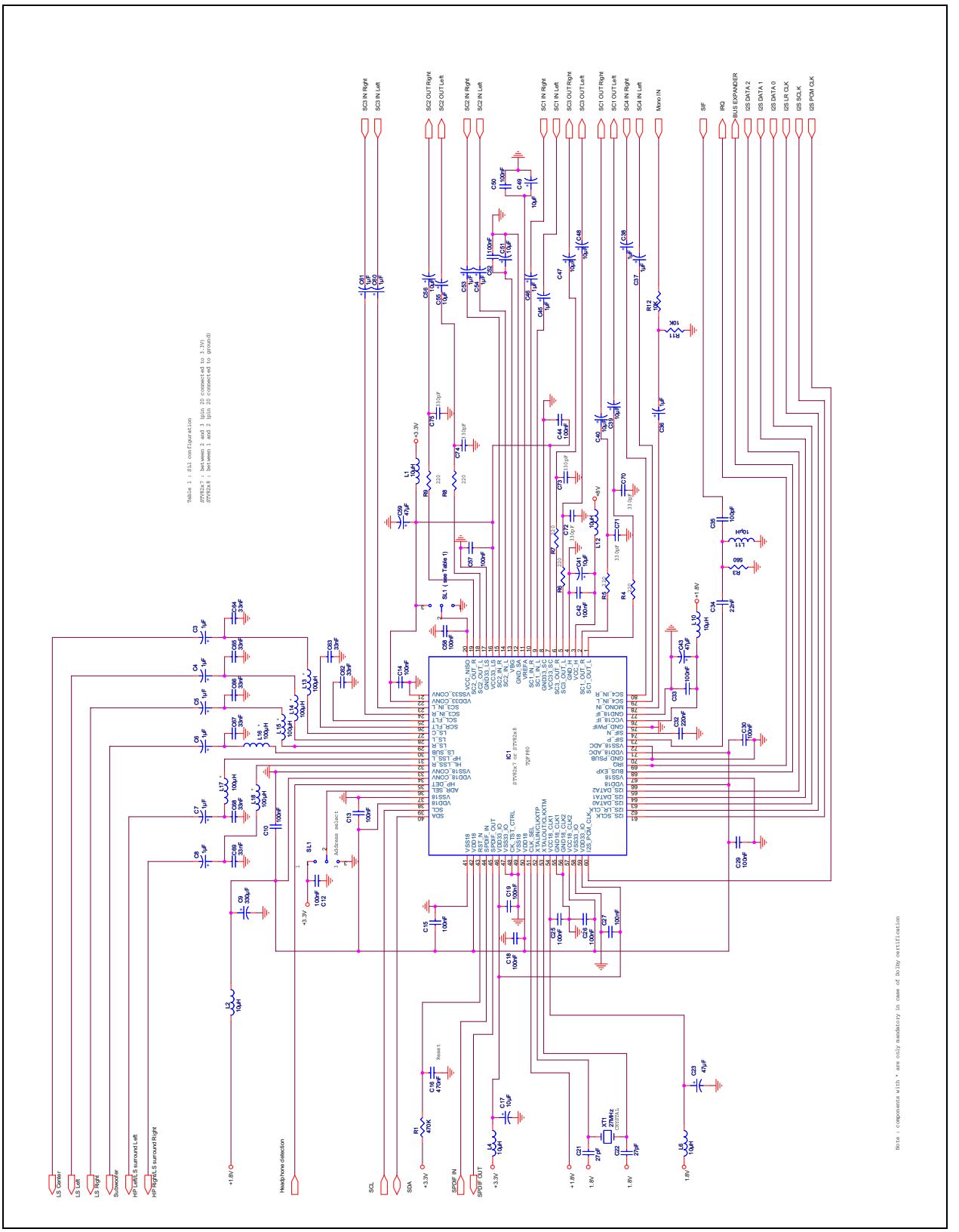
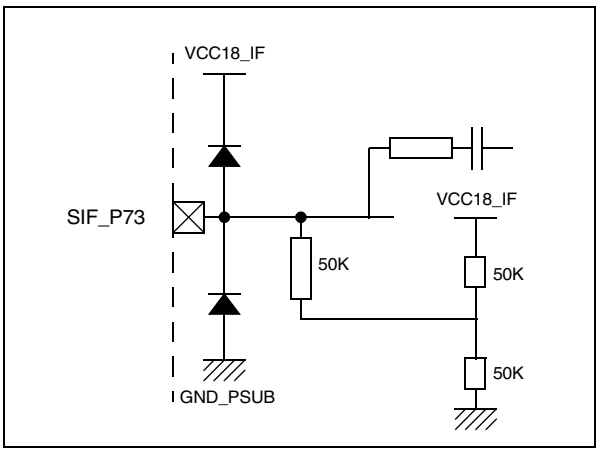


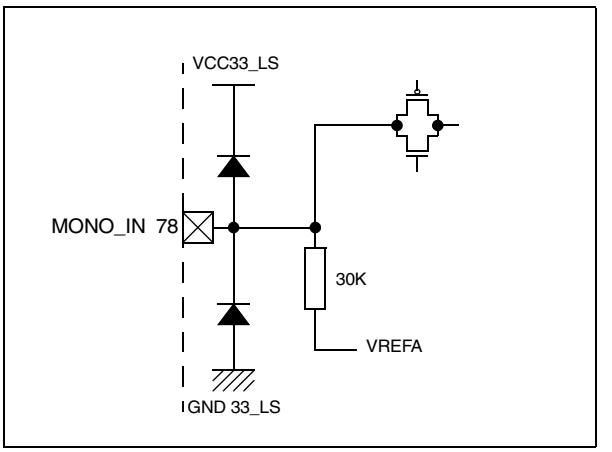
Figure 33: STV82x7/STV82x8 TQFP80 Compatiblity Application Diagram

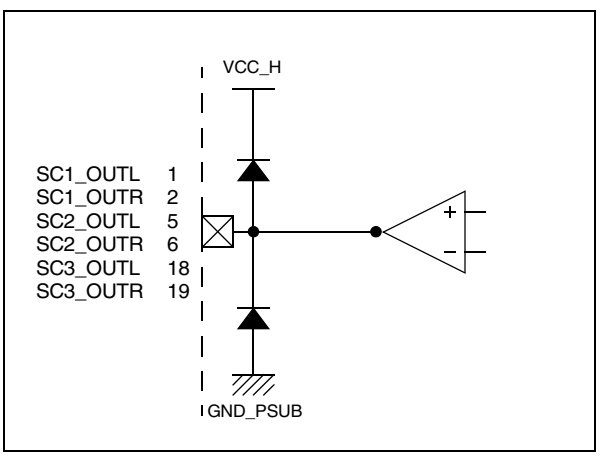


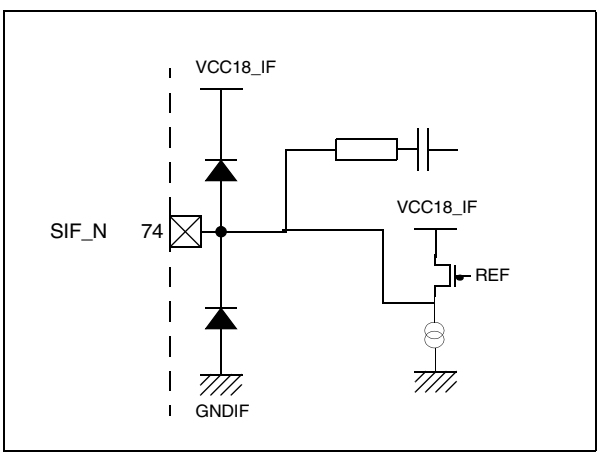
15 Input/Output Groups

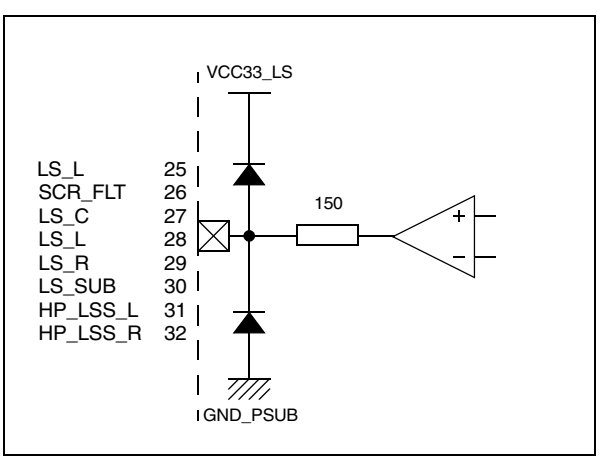
Pin numbers apply to SDIP package only.

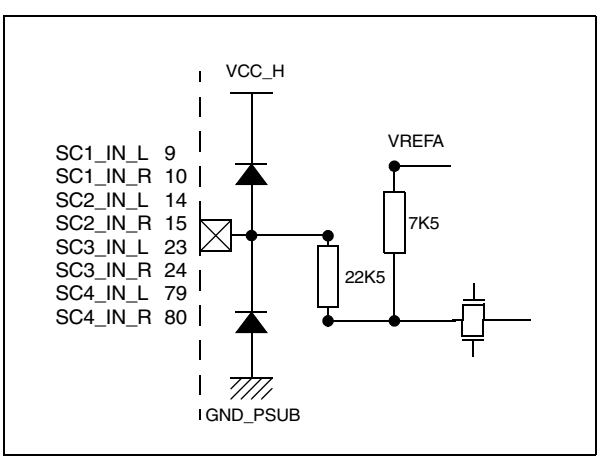


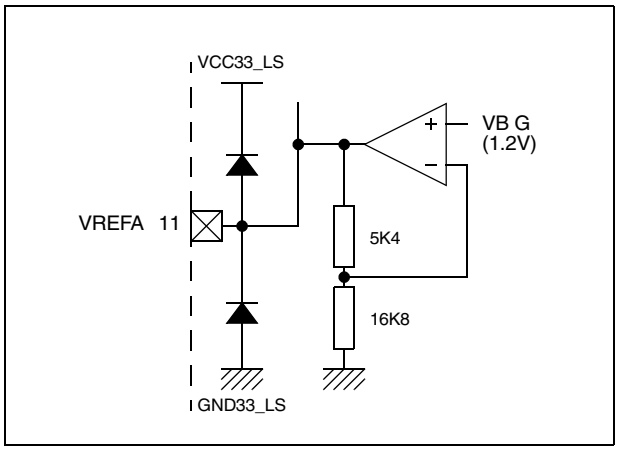


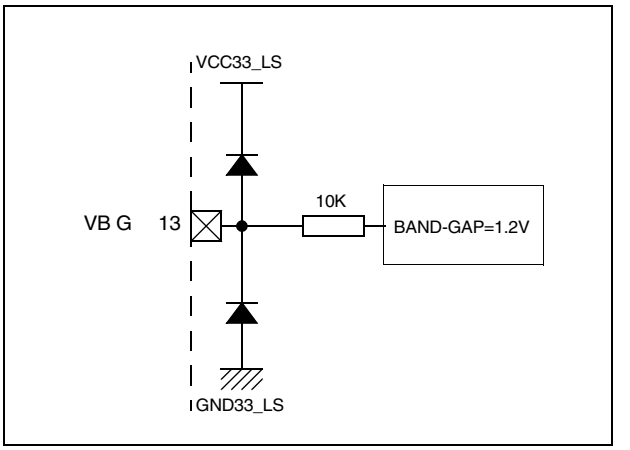


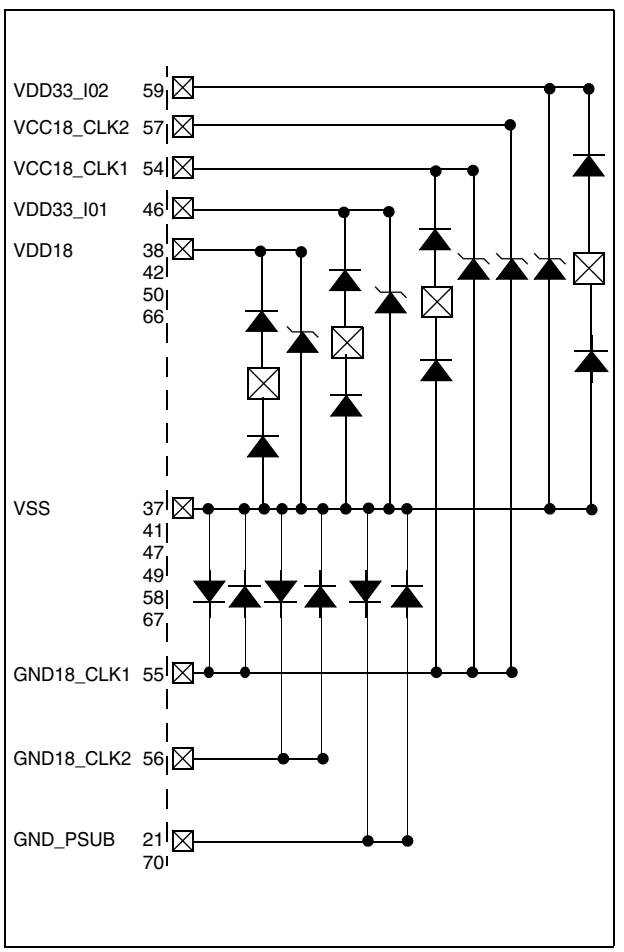


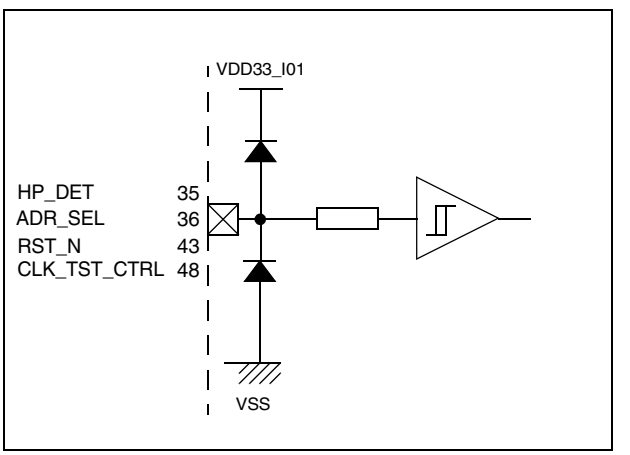


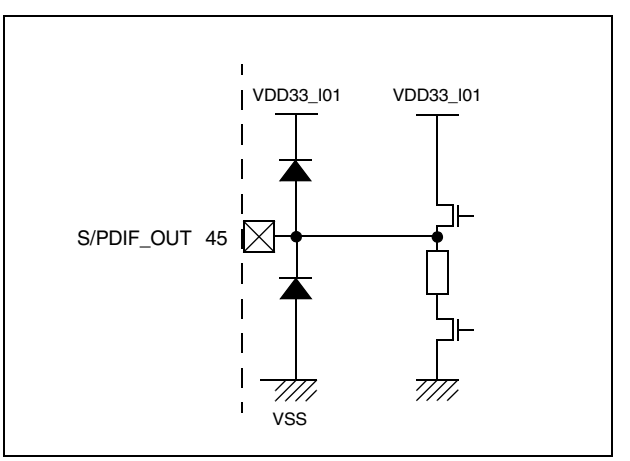


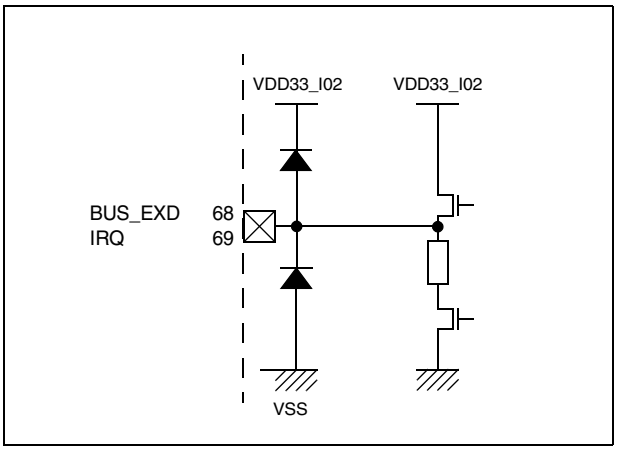

VCC33_LS
VB G
(1.2V)
VREFA 11
5K4
16K8
GND33_LS

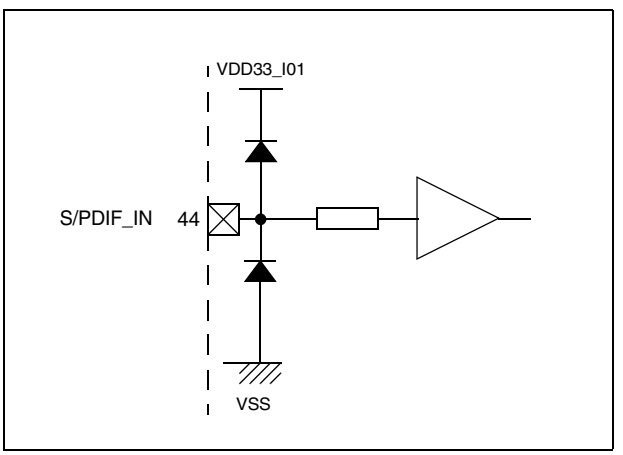

VCC33_LS
10K
VB G 13
BAND-GAP=1.2V
GND33_LS

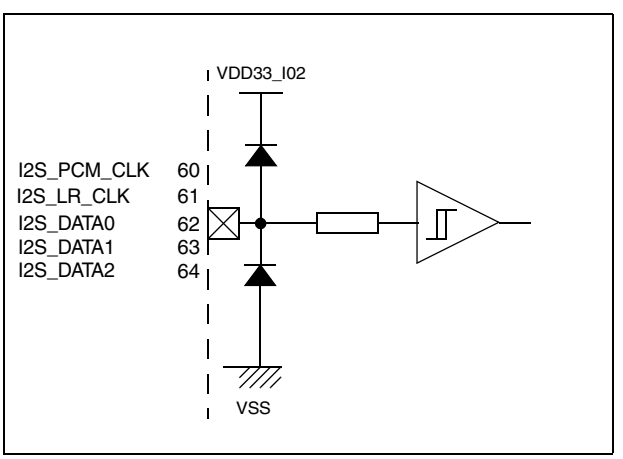

VDD33_I02 59
VCC18_CLK2 57
VCC18_CLK1 54
VDD33_I01 46
VDD18 38
42
50
66
VSS 37
41
47
49
58
67
GND18_CLK1 55
GND18_CLK2 56
GND_PSUB 21
70

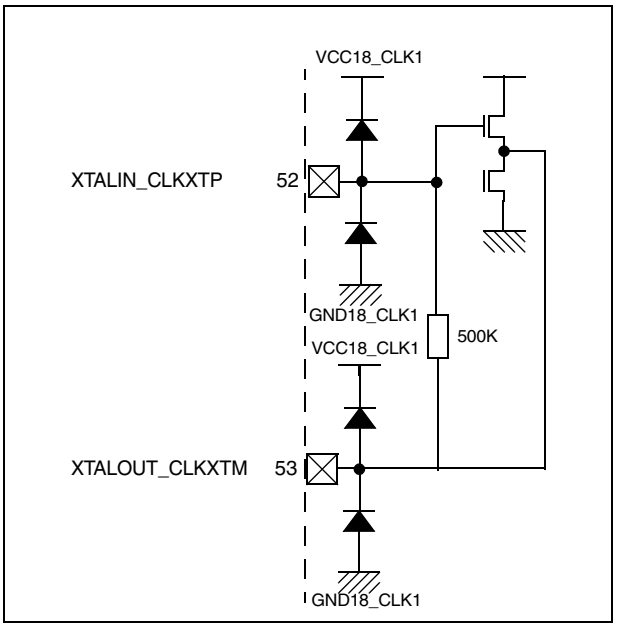

VDD33_I01
HP_DET 35
ADR_SEL 36
RST_N 43
CLK_TST_CTRL 48
VSS

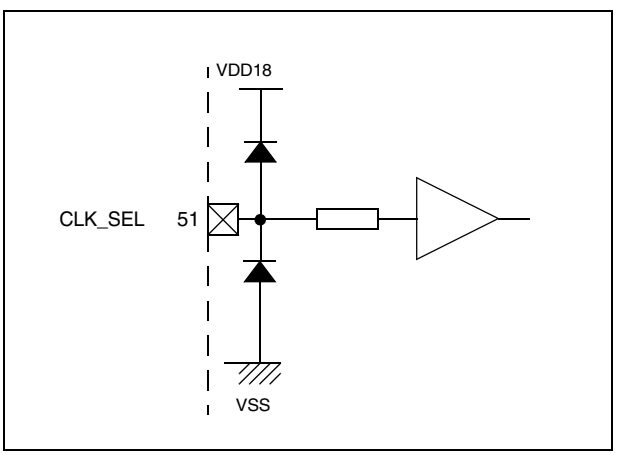

VDD33_I01
VDD33_I01
S/PDIF_OUT 45
VSS

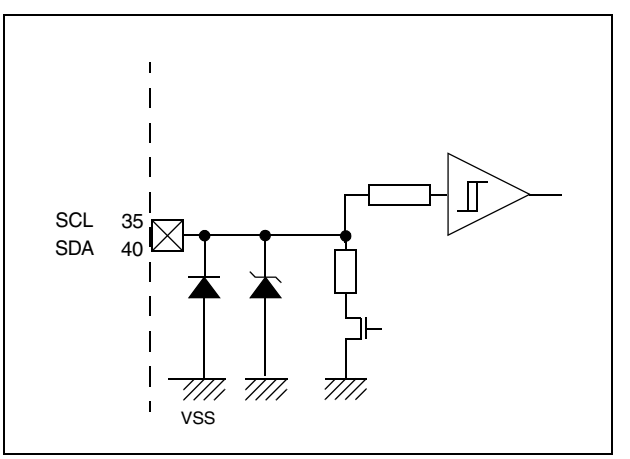

VDD33_I02
VDD33_I02
BUS_EXD 68
IRQ 69
VSS

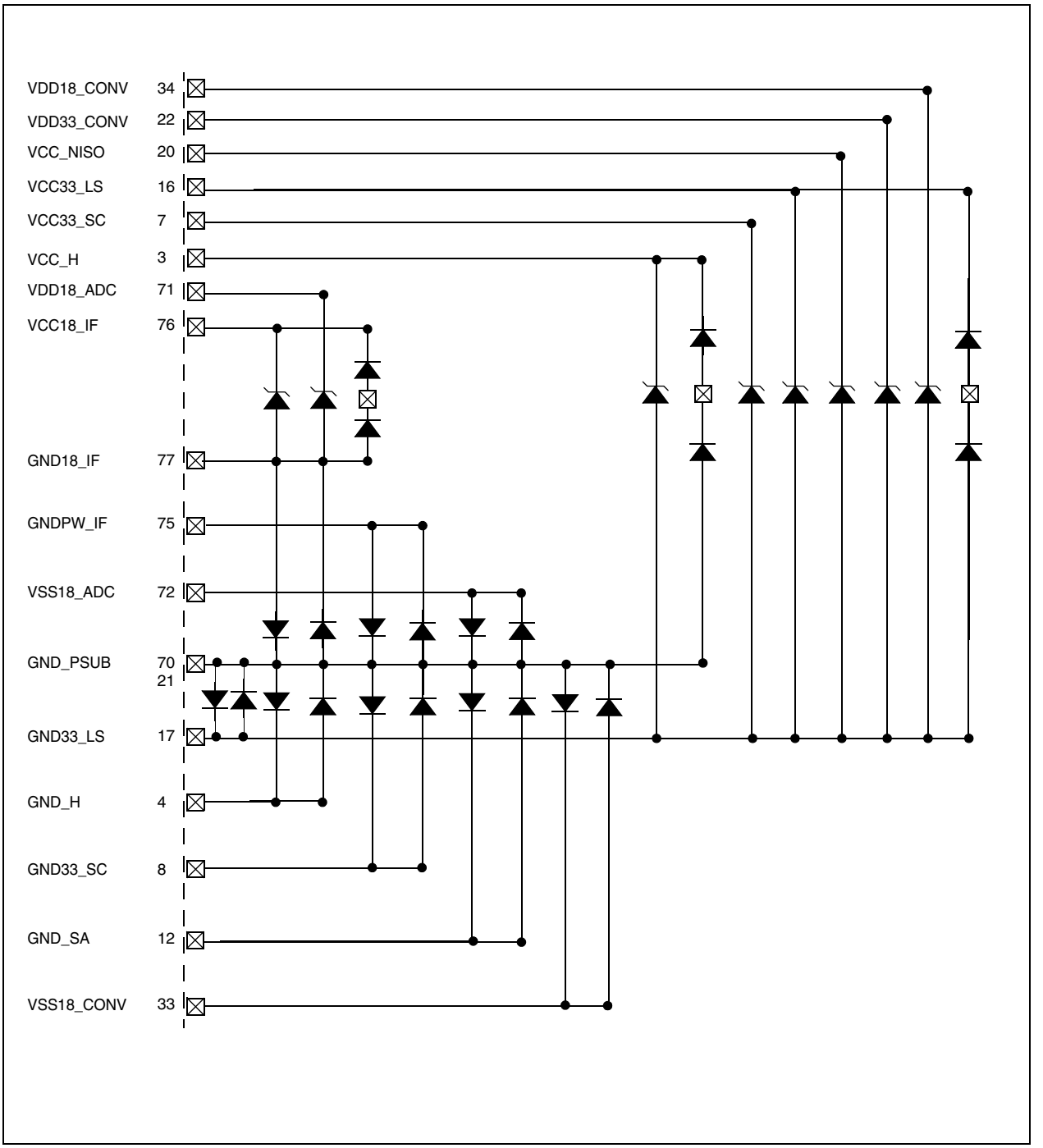

VDD33_I01
S/PDIF_IN 44
VSS


VDD33_I02
I2S_PCM_CLK 60
I2S_LR_CLK 61
I2S_DATA0 62
I2S_DATA1 63
I2S_DATA2 64
VSS


VCC18_CLK1
XTALIN_CLKXTP 52
GND18_CLK1
VCC18_CLK1
500K
XTALOUT_CLKXTM 53
GND18_CLK1


VDD18
CLK_SEL 51
VSS


SCL 35
SDA 40
VSS


VDD18_CONV 34
VDD33_CONV 22
VCC_NISO 20
VCC33_LS 16
VCC33_SC 7
VCC_H 3
VDD18_ADC 71
VCC18_IF 76
GND18_IF 77
GNDPW_IF 75
VSS18_ADC 72
GND_PSUB 70
21
GND33_LS 17
GND_H 4
GND33_SC 8
GND_SA 12
VSS18_CONV 33

16 Electrical Characteristics

Test Conditions: T_{OPER} = 25° C, V_{CC_H} = 8 V, V_{XX_18} = 1.8V, V_{XX_33} = 3.3V, crystal oscillator at 27 MHz, default register values for synthesizer, unless otherwise specified.

16.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{XX_18}	Analog and Digital 1.8 V Supply Voltage (V_{CC18_CLK1}, V_{CC18_CLK2}, V_{CC18_IF}, V_{DD18}, V_{DD18_CONV}, V_{DD18_ADC})	2.5	V
V_{XX_33}	Analog and Digital 3.3 V Supply Voltage (V_{CC33_SC}, V_{CC33_LS}, V_{DD33_IO1}, V_{DD33_IO2}, V_{DD33_CONV}, V_{CC_NISO})	4.0	V
HV_{CC}	Analog Supply High Voltage (V_{CC_H})	8.8	V
V_{ESD}	Capacitor 100 pF discharged via 1.5 kΩ serial resistor (Human Body Model)	4	kV
T_{OPER}	Operating Ambient Temperature	0, +70	°C
T_{STG}	Storage Temperature	-55 to +150	°C

16.2 Thermal Data

Symbol	Parameter		Value	Units
R_{thJA}	Junction-to-Ambient Thermal Resistance		42	°C/W

16.3 Power Supply Data

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{XX_18}	Analog and Digital 1.8 V Supply Voltage (V_{CC18_CLK1}, V_{CC18_CLK2}, V_{CC18_IF}, V_{DD18}, V_{DD18_CONV}, V_{DD18_ADC})	1.70	1.80	1.90	V
V_{XX_33}	Analog and Digital 3.3 V Supply Voltage (V_{CC33_SC}, V_{CC33_LS}, V_{DD33_IO1}, V_{DD33_IO2}, V_{DD33_CONV}, V_{CC_NISO})	3.13	3.30	3.47	V
HV_{CC}	Analog Supply High Voltage (V_{CC_H})	7.6	8.0	8.4	V
I_{VDD18}	Current Consumption for Digital 1.8 V Supply (V_{CC18_CLK2}, V_{DD18}, V_{DD18_CONV}, V_{DD18_ADC})		TBD		mA
I_{VDD33}	Current Consumption for Digital 3.3 V Supply (V_{DD33_IO1}, V_{DD33_IO2})		TBD		mA
I_{VCC18}	Current Consumption for Analog 1.8 V Supply (V_{CC18_CLK1}, V_{CC18_IF})		TBD		mA
I_{VCC33}	Current Consumption for Analog 3.3 V Supply (V_{CC33_SC}, V_{CC33_LS}, V_{DD33_CONV}, V_{CC_NISO})		TBD		mA
I_{VCC_H}	Current Consumption for Analog Supply High Voltage (8 V)		TBD		mA
P_{DTOT}	Total Power Dissipation		TBD		mW

16.4 Crystal Oscillator

Symbol	Parameter	Min.	Typ.	Max.	Units
f_P	Crystal Series Resonance Frequency (at C21 = C22 = 27 pF load capacitor)		27		MHz
DF/F_P	Frequency Tolerance at 25 °C	-30		+30	ppm
DF/F_T	Frequency Stability versus Temperature within a range from 0 to 70 °C	-30		+30	ppm
C1	Motional Capacitor			15	fF
R_S	Serial Resistance			30	Ω
C_S	Shunt Capacitance			7	pF

16.5 Analog Sound IF Signal

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
$BAND_{SIF}$	SIF Frequency Flatness		AGC_ERR at 0, frequency range from 4 to 7MHz				dB
R_{INSIF}	SIF Input Resistance			60	72	85	kΩ
DC_{INSIF}	SIF Input DC Level				0.9		V
C_{INSIF}	SIF Input Capacitance				3		pF
FM Carrier							
$VSIF_{FM}$	SIF Input Sensitivity		SNR 40 dB RMS unweighted 20 Hz to 15 kHz Standard M/N 27 kHz FM Deviation 1 kHz	TBD			μV_{PP}
$DFSIF_{FM}$	SIF Carrier Accuracy for FM	Standard (FM50k)			±1	±5	kHz
		Shifted Standard (FM50k with DCO compensation)				±120	kHz
AGC							
AGC_{step}	IF AGC Step			1.4	1.5	1.6	dB
AGC_{dyn}	Relative Maximum Gain to Step 0		Valid from Step 21 to Step 31	29	30	31	dB

16.6 SIF to I²S Output Path Characteristics

Test Conditions: SIF amplitude = 100 mVpp, unless otherwise specified, I²S output.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
FM Demodulation						
$BAND_{FM}$	Frequency Response	20 Hz to 15 kHz			TBD	dB

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SNR_{FM}	Signal to Noise	RMS unweighted, 20 Hz to 15 kHz, Standard M/N 27 kHz FM Deviation,1 kHz	TBD			dB
THD_{FM}	Total Harmonic Distortion				TBD	%
SEP_{FM}	Stereo Channel Separation	Standard M/N BTSC stereo, FM deviation, 1 kHz	TBD			dB

16.7 SCART to SCART Analog Path Characteristics

Test Conditions: $Rload_{MAX}$ = 10 kΩ, $Cload_{MAX}$ = 330 pF, MONO_IN voltage = 0.5 V_{RMS}

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
Analog-to-Analog STEREO and MONO							
$R_{INSCART}$	SCART Input Resistance				34		kΩ
$R_{OUTSCART}$	Output Resistance for SCARTs				40		Ω
$VDC_{INSCART}$	SCART Input DC Level				1.57		V
$VDC_{OUTSCART}$	SCART Output DC Level				3.64		V
$CLIP_{SCART}$	Clipping SCART	Clipping input level from SCART input	At 1 kHz 1% THD				V_{RMS}
		Clipping input level from MONO_IN input					V_{RMS}
THD_{SCART}	THD SCART	THD from SCART input	1 V_{RMS}, at 1 KHz		0.02		%
		THD from MONO_IN input	0.25 V_{RMS}, at 1 KHz		0.02		%
SNR_{SCART}	Signal to Noise Ratio	SCART input	1 $V_{RMS,}$ 20 Hz to 20 kHz Bandwidth, RMS unweighted		82		dB
		MONO_IN input	0.25 $V_{RMS,}$ 20 Hz to 20 kHz Bandwidth, RMS unweighted		76		dB
$BAND_{SCART}$	Frequency Flatness	SCART input	20 Hz to 20 kHz				dB
		MONO_IN input	20 Hz to 20 kHz		12		dB
$XTALK_{L/R}$	Left/Right Crosstalk		1 V_{RMS} @ 1 kHz on ref signal, the other one grounded		90		dB
$XTALK_{IN}$	Audio Crosstalk from Input Channel *n* to Input Channel *m*		1 V_{RMS} @ 1 kHz on ref signal, all other inputs grounded		90		dB
$XTALK_{OUT}$	Audio Crosstalk from Output Channel *n* to Output Channel *m*		1 V_{RMS} @ 1 kHz on reference output, signal on a single input, all other inputs grounded		90		dB

16.8 SCART and MONO IN to I²S Path Characteristics

Test Conditions: Sampling Frequency = 32 kHz, Maximum MONO_IN voltage = 0.5 V_{RMS}.

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
THD_{ADC}	THD ADC	THD from SCART input	V_{IN} = 2 V_{RMS} at 1 KHz		0.006		%
		THD from MONO_IN input	V_{IN} = 0.5 V_{RMS} at 1 KHz		0.006		%
SNR_{ADC}	Signal to Noise Ratio		20 to 15 kHz Bandwidth, RMS unweighted V_{IN} = 200 mV_{RMS} SCART input				dB
$BAND_{ADC}$	Frequency Flatness		20 Hz to 15 kHz				dB
$XTALK_{ADC}$	Left Right Crosstalk		at 1 KHz, V_{IN} = 1 V_{RMS}				dB

16.9 I2S to LS/HP/SUB/C Path Characteristics

Test Conditions: Sampling Frequency = 32KHz, L_{LOAD} = 100 µH, C_{LOAD} = 33nF, R_{LOAD} = 30KΩ

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
R_{OUTDAC}	Output Resistance for Main Outputs	LS_L, LS_R, LS_SUB, LS_C, HP_LSS_R and HP_LSS_L pins		90		Ω
VDC_{OUTDAC}	MAIN Output DC Level			1.54		V
THD_{DAC}	Total Harmonic Distortion	90% Full-scale Range at 1 kHz				%
SNR_{DAC}	Signal to Noise Ratio	20 to 15 kHz Bandwidth, RMS unweighted, at -20dB full range				dB
$V_{OUTAMPDAC}$	MAIN Output Amplitude	100% Full-scale Range at 1 kHz		900		mV_{RMS}
$XTALK_{DAC}$	Left Right Crosstalk	at 1 KHz, -20dBFS				dB

16.10 I²S to SCART Path Characteristics

Test Conditions: Sampling Frequency = 32 kHz, C_{LOAD} = 33 nF on DAC SCART pins, DAC SCART prescale at -5.5 dB.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$THD_{DACSCART}$	Total Harmonic Distortion	90% Full-scale Range at 1 kHz		0.08		%
$SNR_{DACSCART}$	Signal to Noise Ratio	20 Hz to 15 kHz Bandwidth unweighted, -20dB Full Range				dB
$V_{ODACSCART}$	MAIN Output Amplitude	100% Full-scale Range at 1 kHz		2		V_{RMS}
$XTALK_{DACSCART}$	Left Right Crosstalk	at 1 KHz, -20 dBFS				dB

16.11 MUTE Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$MUTE_{DAC}$	DAC Mute analog	I2S to DAC at 1 kHz				dB
$MUTE_{SCART}$	SCART Mute	2 V_{RMS} @ 1 kHz on ref signal, all other inputs grounded				dB

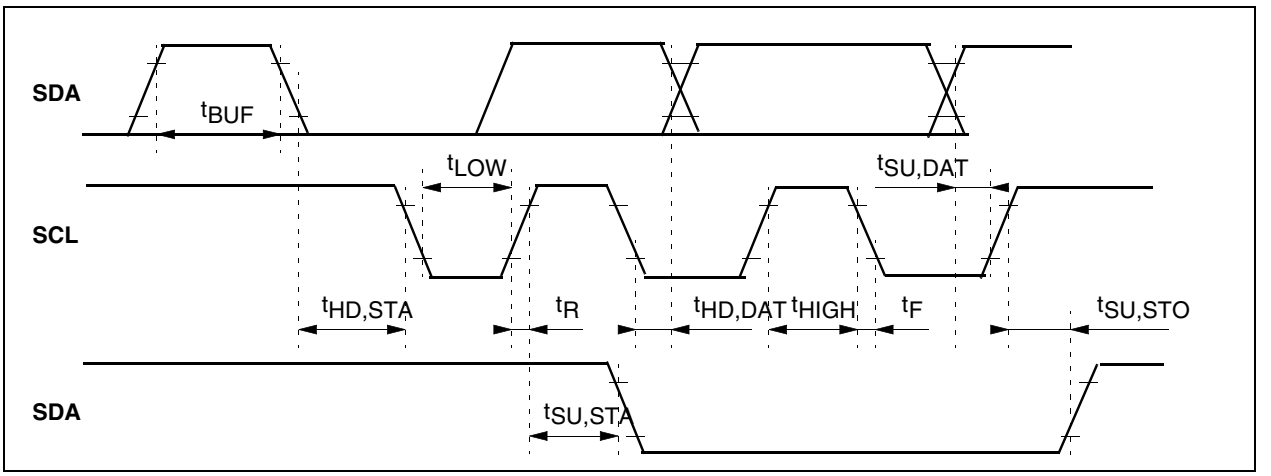
16.12 Digital I/Os Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Low Level Input Voltage	except SDA, SCL and CLK_SEL, 3.3V power supply			0.5	V
V_{IH}	High Level Input Voltage	except SDA, SCL and CLK_SEL, 3.3V power supply	2.0			V
I_{IN}	Input Current				1	µA
VIL_{CLK_SEL}	CLK_SEL Low Level Input Voltage	1.8V power supply			0.3	V
VIH_{CLK_SEL}	CLK_SEL High Level Input Voltage	1.8V power supply	1.2			V
V_{OL}	Low Level Output Voltage	S/PDIF_OUT, IRQ, BUS_EXP			0.3	V
V_{OH}	High Level Output Voltage	S/PDIF_OUT, IRQ, BUS_EXP	3.0			V

16.13 I²C Bus Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
SCL						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		2.3		5.5	V
I_{IL}	Input Leakage Current	V_{IN} = 0 to 5.0 V	-10		10	µA
f_{SCL}	Clock Frequency				400	kHz
t_R	Input Rise Time	1 V to 2 V			300	ns
t_F	Input Fall Time	2 V to 1 V			300	ns
C_I	Input Capacitance				10	pF
SDA						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		2.3		5.5	V
I_{IL}	Input Leakage Current	V_{IN} = 0 to 5.0 V	-10		10	µA
t_R	Input Rise Time	1 V to 2 V			300	ns
t_F	Input Fall Time	2 V to 1 V			300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3 mA			0.4	V
t_F	Output Fall Time	2 V to 1 V			250	ns
C_L	Load Capacitance				400	pF
C_I	Input Capacitance				10	pF
I²C Timing						
t_{LOW}	Clock Low period		1.3			µs
t_{HIGH}	Clock High period		0.6			µs
$t_{SU,DAT}$	Data Set-up Time		100			ns
$t_{HD,DAT}$	Data Hold Time		0		900	ns
$t_{SU,STO}$	Set-up Time from Clock High to Stop		0.6			µs
t_{BUF}	Start Set-up Time following a Stop		1.3			µs
$t_{HD,STA}$	Start Hold Time		0.6			µs
$t_{SU,STA}$	Start Set-up Time following Clock Low to High Transition		0.6			µs

Figure 34: I²C Bus Timing



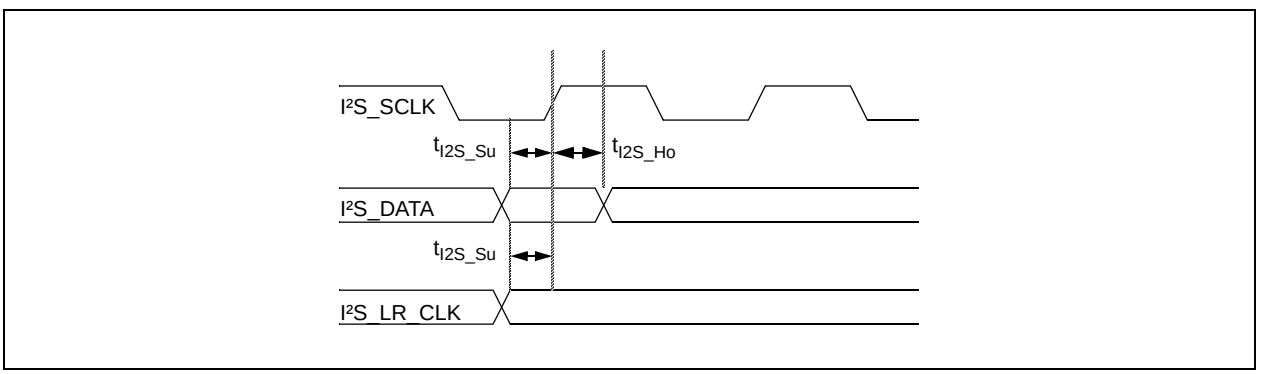
16.14 I²S Bus Interface

I²S Bus Interface timing values shown in Figure 35.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I²S Input						
V_{I2S_IL}	Input I²S Low Level Voltage				0.8	V
V_{I2S_IH}	Input I²S High Level Voltage		2			V
Z_{I2S}	Input I²S Impedance				5	pF
I_{I2S_Leak}	I²S Leakage Current		-1		1	µA
t_{I2S_Su}	I²S Input Setup Time before Rising Edge of Clock	See Figure 35	30			ns
t_{I2S_Ho}	I²S Input Hold Time after Rising Edge of Clock	See Figure 35	100			ns
f_{I2S_LR0}	I²S Left Right Strobe Input Frequency (I²S_DATA0 and I²SA_DATA with SRC)		30		49	kHz
f_{I2S_SCL0}	I²S Serial Clock Input Frequency (I²S_DATA0 and I²SA_DATA with SRC)		1.092		3.136	MHz
f_{I2S_LR}	I²S Left Right Strobe Input Frequency (I²S_DATA0 and I²SA_DATA with PLL, I²S_DATA1,2)	Deviation = ±250 ppm	32	48		kHz
f_{I2S_SCL}	I²S Serial Clock Input Frequency (I²S_DATA0 and I²SA_DATA with PLL, I²S_DATA1,2)			3.072		MHz
R_{I2S_SCL}	I²S Serial Clock Input Ratio		0.9		1.1	
I²S Output (I²S_DATA0 only)						
V_{I2SOL}	Output I²S Low Level Voltage	I_{OL} = 2 mA			0.4	V
V_{I2SOH}	Output I²S High Level voltage	I_{OH} = 2 mA	2.4			V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{I2S_OLR}	I²S Left Right Strobe Output Frequency (I²S_DATA0 and I²SO_DATA0,1)			48		kHz
f_{I2S_OSCL}	I²S Serial Clock Output Frequency (I²S_DATA0 and I²SO_DATA0,1)			3.072		MHz
R_{I2S_SCL}	I²S Serial Clock Output Ratio		0.9		1.1	
t_{I2S_DEL}	I²S Output Delay After Falling Edge of Clock	See Figure 35, Cl = 30 pF			30	ns

Figure 35: I²S Input Bus Timings



17 Package Mechanical Data

17.1 TQFP80 Package

Figure 36: 80-Pin Thin Plastic Quad Flat Package

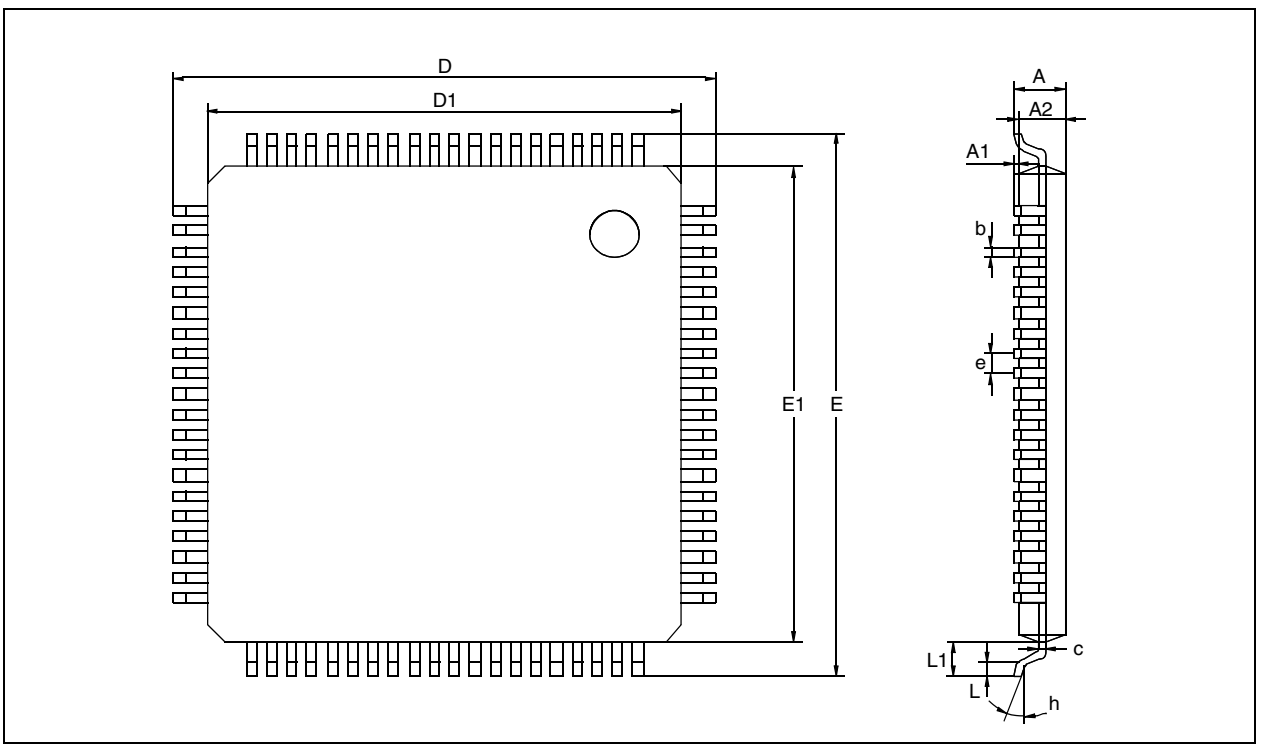


Table 23: Package Mechanical Dimensions

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.65			0.026	
K	0°	3.5°	0.75°	0°	3.5°	0.75°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	

17.2 TQFP100 Package

Figure 37: 100-Pin Thin Plastic Quad Flat Package

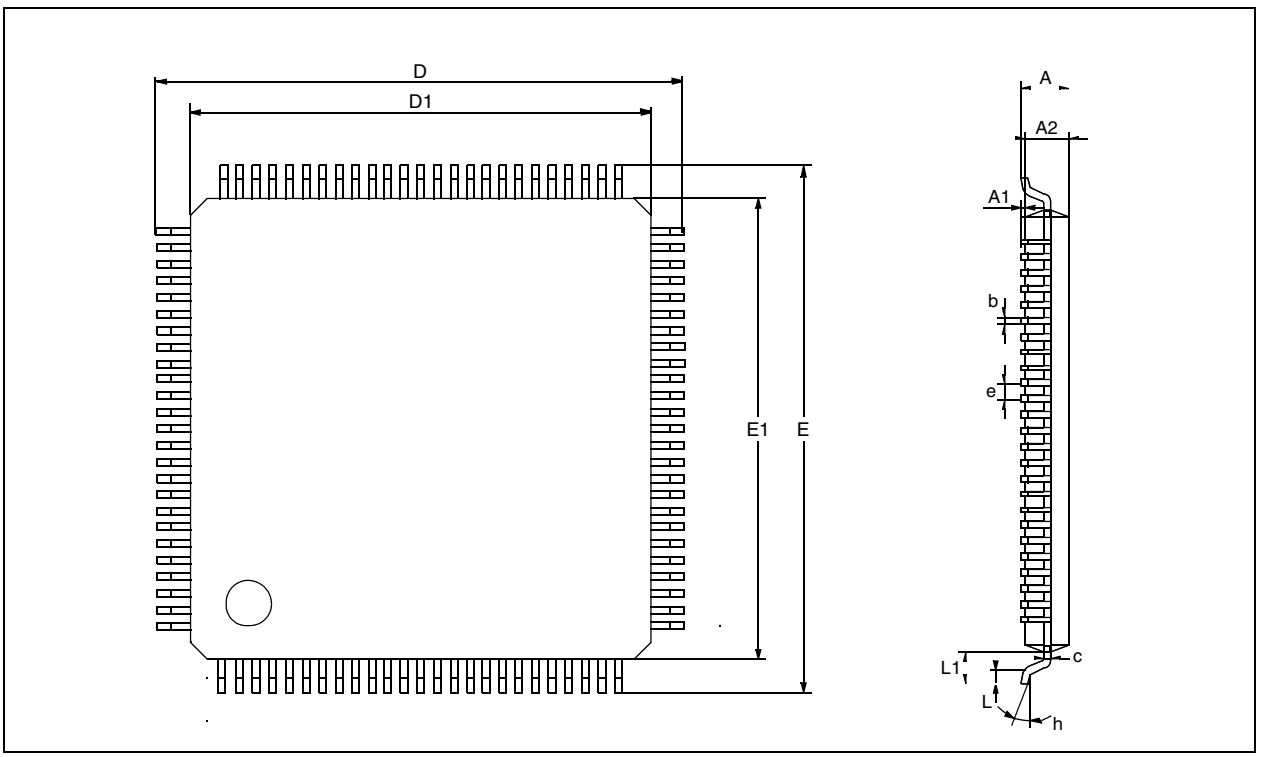


Table 24: Package Mechanical Dimensions

Dim.	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	100					

18 Revision History

Revision	Date	Modification
0.1	15 Nov. 2004	Preliminary Datasheet - First Issue.
0.2	19 Nov. 2004	Major updates to Key Features on page 1, Typical Applications on page 1 and Chapter 1: General Description on page 8.
0.3	7 Jan. 2005	Addition of TQFP100 information.
1.0	23 Feb. 2005	Updated Figure 1: STV82x8 Block Diagram (TQFP80) on page 2, Figure 2: STV82x8 Block Diagram (TQFP100) on page 3, Section 16.5: Analog Sound IF Signal on page 146 and Section 16.6: SIF to I²S Output Path Characteristics on page 146.

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