



STL80NF3LL

N-CHANNEL 30V - 0.0045Ω - 80A PowerFLAT™ (6X5)

STripFET™ II MOSFET

PRODUCT PREVIEW

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STL80NF3LL	30 V	< 0.0055 Ω	20 A (2)

- TYPICAL R_{DS(on)} = 0.0045 Ω @ 10V
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

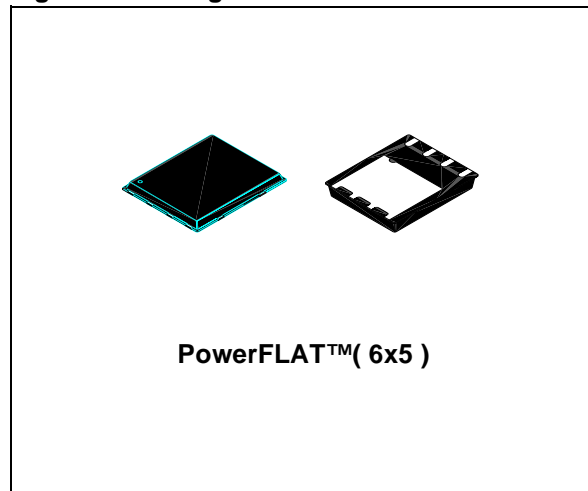
DESCRIPTION

The STL80NF3LL utilizes the second generation of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. Such features make it the best choice in high efficiency DC-DC converters for Telecom and Computer industries. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

APPLICATIONS

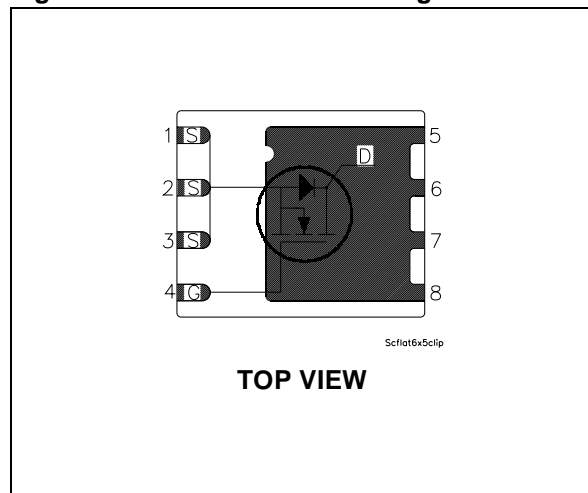
- HIGH-EFFICIENCY DC-DC CONVERTERS
- SYNCHRONOUS RECTIFICATION

Figure 1: Package



PowerFLAT™ (6x5)

Figure 2: Internal Schematic Diagram



TOP VIEW

Table 2: Order Codes

Part Number	Marking	Package	Packaging
STL80NF3LL	L80NF3LL	PowerFLAT™ (6x5)	TAPE & REEL

Rev. 3

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{GS}	Gate- source Voltage	± 16	V
I _D (1)	Drain Current (continuous) at T _C = 25°C	80	A
I _D (1)	Drain Current (continuous) at T _C = 100°C	50	A
I _{DM} (3)	Drain Current (pulsed)	320	A
I _D (2)	Drain Current (continuous) at T _C = 25°C	20	A
P _{TOT} (2)	Total Dissipation at T _C = 25°C	4	W
P _{TOT} (1)	Total Dissipation at T _C = 25°C	80	W
	Derating Factor(2)	0.03	W/°C
T _{stg}	Storage Temperature	- 55 to 150	°C
T _j	Max. Operating Junction Temperature		

Table 4: Thermal Data

R _{thj-c}	Thermal Resistance Junction-Case (Drain)	1.56	°C/W
R _{thj-pcb} (2)	Thermal Operating Junction-pcb	31.3	°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)**Table 5: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			± 10	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1			V
R _{DSON}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 10 A V _{GS} = 4.5 V, I _D = 10 A		0.0045 0.0055	0.0055 0.007	Ω Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (4)	Forward Transconductance	V _{DS} = 10V, I _D = 10 A		37		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f= 1 MHz, V _{GS} = 0		2160		pF
C _{oss}	Output Capacitance			614		pF
C _{rss}	Reverse Transfer Capacitance			98		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		4.1		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}= 15\text{ V}$, $I_D= 10\text{ A}$		23.5		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$		39		ns
$t_{d(off)}$	Turn-off-Delay Time	(see Figure 15)		47.5		ns
t_f	Fall Time			37		ns
Q_g	Total Gate Charge	$V_{DD}= 15\text{V}$, $I_D= 10\text{ A}$, $V_{GS}= 4.5\text{ V}$		26	35	nC
Q_{gs}	Gate-Source Charge	(see Figure 17)		7		nC
Q_{gd}	Gate-Drain Charge			12		nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
I_{SDM} (3)	Source-drain Current (pulsed)				80	A
V_{SD} (4)	Forward On Voltage	$I_{SD}= 20\text{ A}$, $V_{GS}= 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD}= 20\text{ A}$, $di/dt= 100\text{ A}/\mu\text{s}$,		39		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}= 15\text{ V}$, $T_j = 150^\circ\text{C}$		45		nC
I_{RRM}	Reverse Recovery Current	(see Figure 16)		2.3		A

(1) The value is rated according R_{thj-c} .

(2) When mounted on FR-4 board of 1in^2 , 2oz Cu., $t < 10\text{sec}$

(3) Pulse width limited by safe operating area.

(4) Pulsed: Pulse duration = $300\ \mu\text{s}$, duty cycle 1.5 %

Figure 3: Safe Operating Area

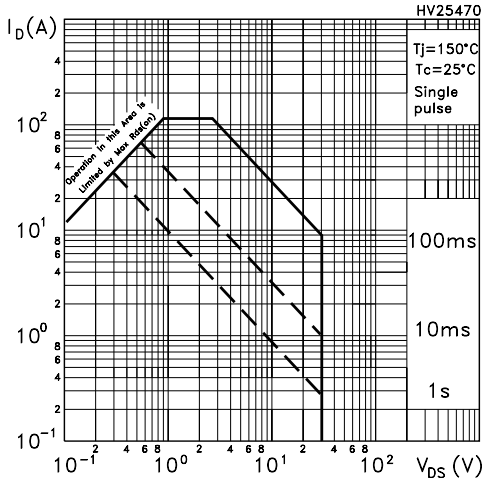


Figure 4: Output Characteristics

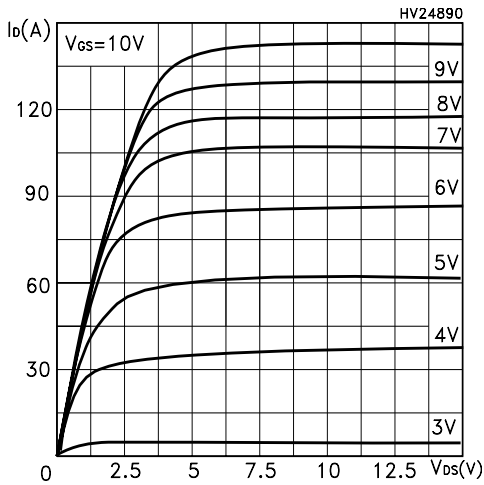


Figure 5: Transconductance

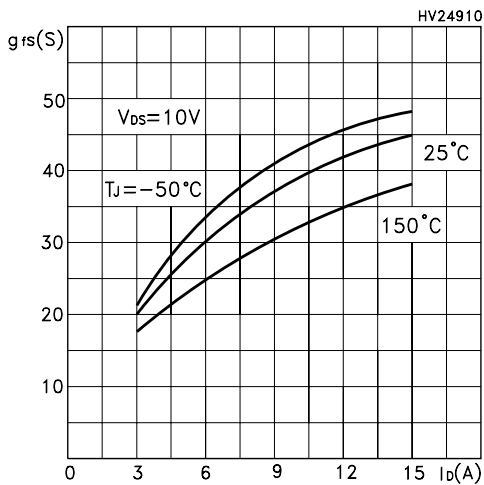


Figure 6: Thermal Impedance

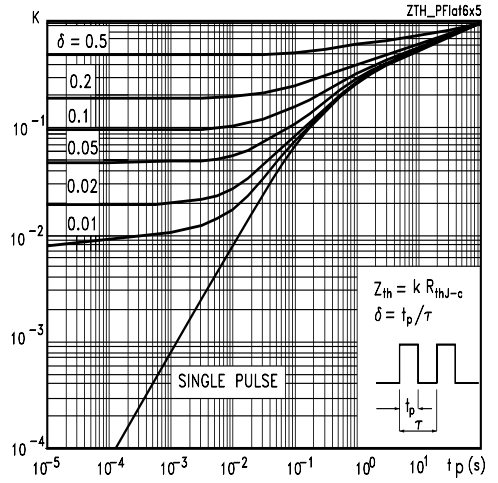


Figure 7: Transfer Characteristics

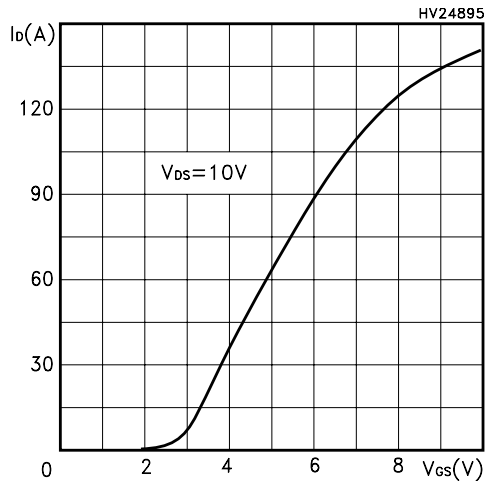


Figure 8: Static Drain-source On Resistance

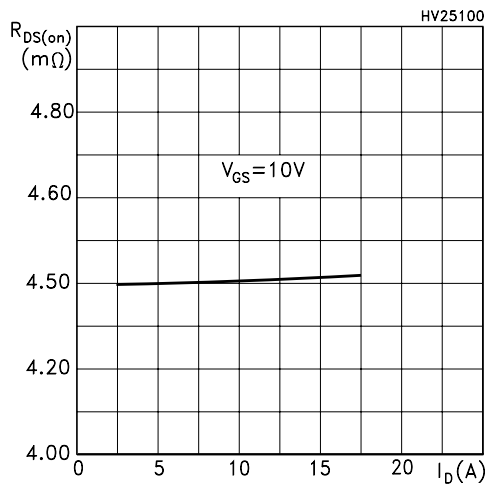


Figure 9: Gate Charge vs Gate-source Voltage

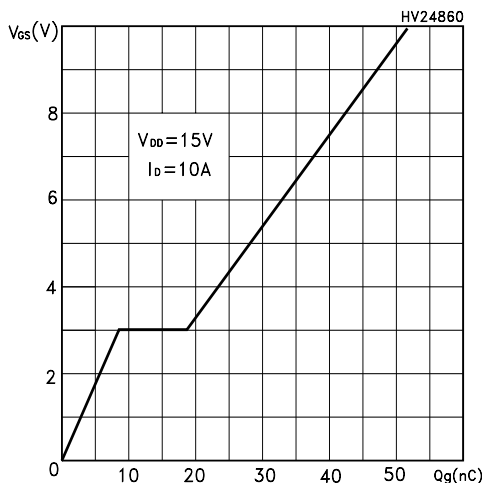


Figure 10: Normalized Gate Threshold Voltage vs Temperature

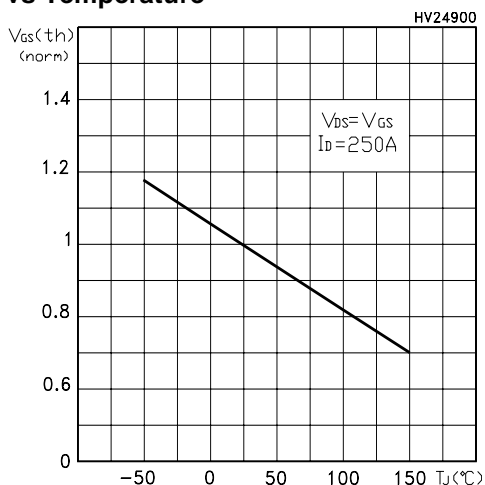


Figure 11: Normalized On Resistance vs Temperature

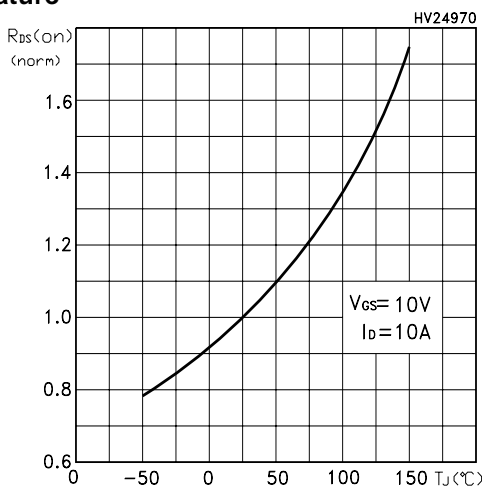


Figure 12: Capacitance Variations

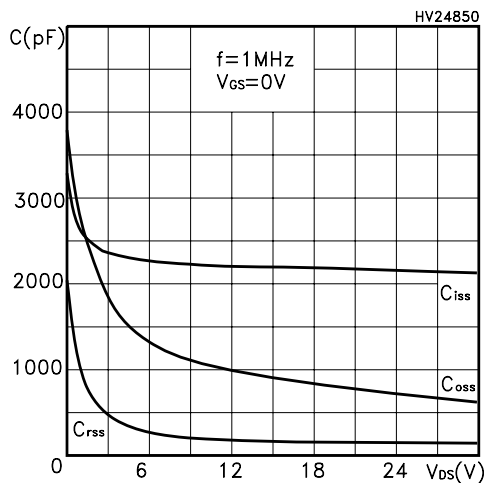


Figure 13: Normalized BVDSS vs Temperature

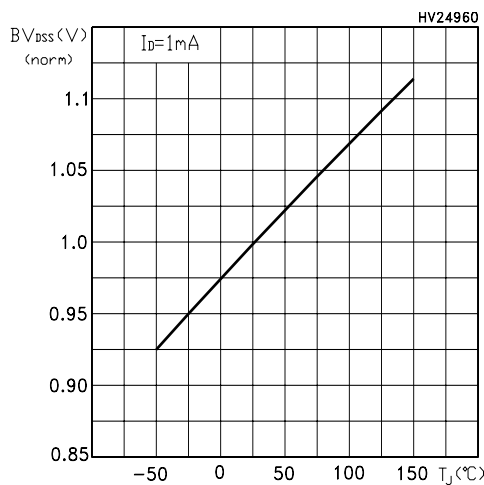


Figure 14: Source-Drain Diode Forward Characteristics

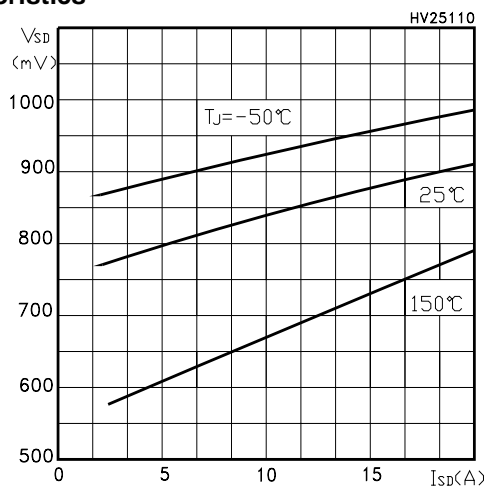


Figure 15: Switching Times Test Circuit For Resistive Load

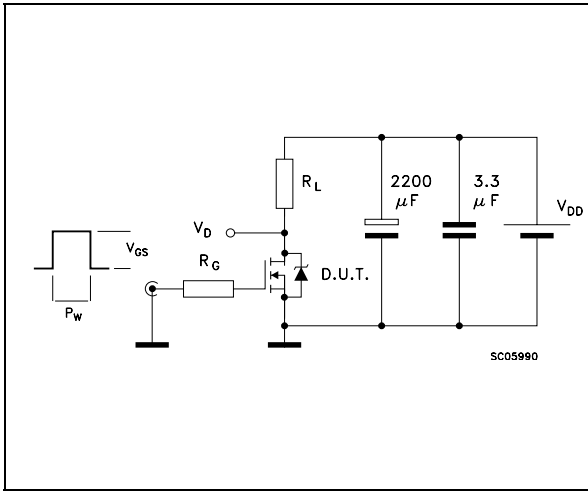


Figure 16: Test Circuit For Diode Recovery Times

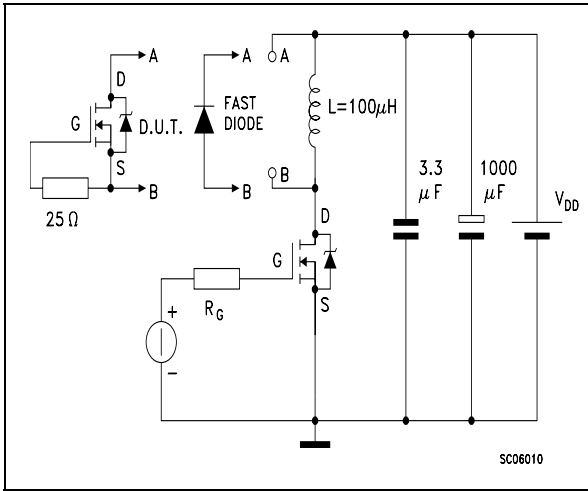
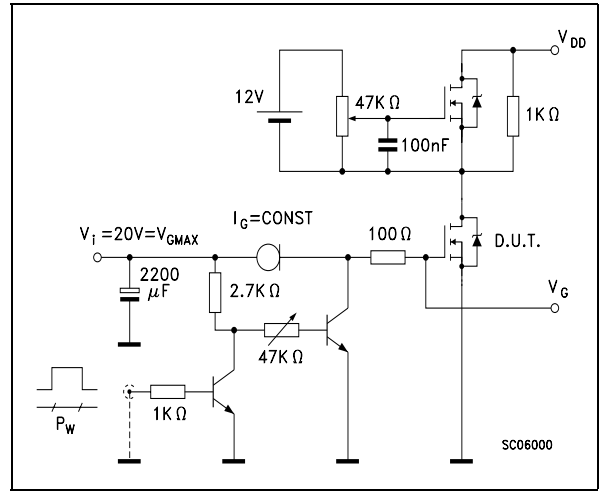


Figure 17: Gate Charge Test Circuit



PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68	0.103	0.105	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035

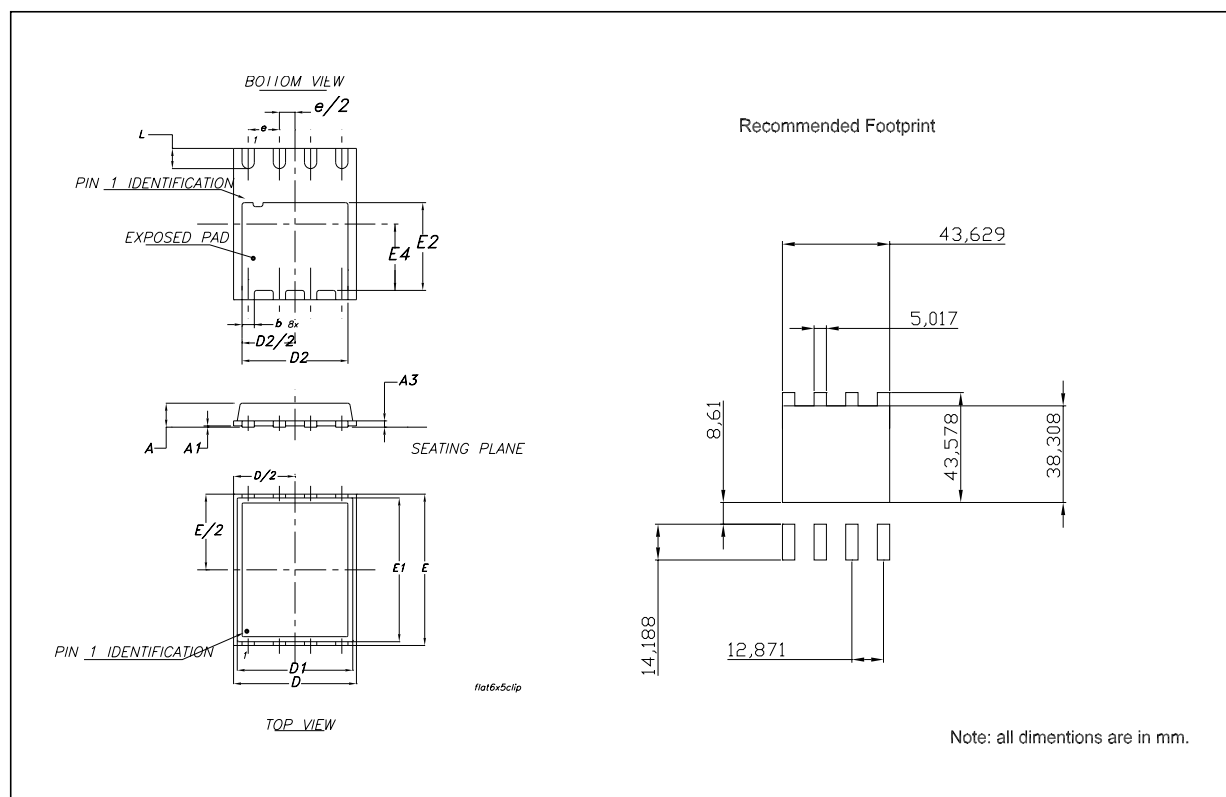


Table 9: Revision History

Date	Revision	Description of Changes
18-Apr-2005	1	First Release.
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New R_G value on table 6

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