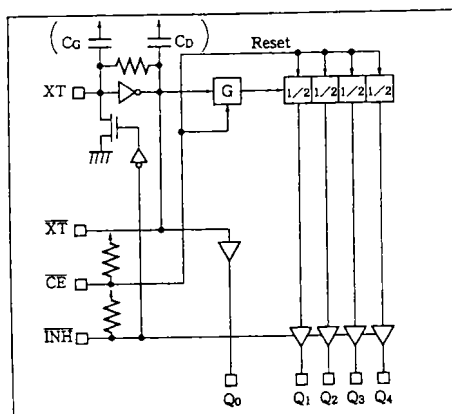


The SM5605F series are C-MOS LSIs for quartz oscillating module. Each LSI has a high frequency oscillating circuit and dividers with low current consumption. One of the output signals is a fundamental frequency and the others are divided frequencies. This series have two types of oscillating circuits. One is built-in capacitor for oscillating, and the other is the type of external capacitor.

- Operating voltage (3 to 6V)
- Built-in feed back resistance of inverter amplifier
- Fundamental frequency and divided frequencies output
- Built-in capacitor for oscillating (FC type) CD-20pF (TYP), CG-20pF (TYP)
- Maximum frequency ... 30MHz
- Low current consumption
- Fan out 2TTL
- Standby function
- Chip form

Pin diagram of the A5605F IC. The chip is a square package with pins numbered 1 to 16. The top pins (1-5) are XT, INH, XT, VDD, and CE. The right pins (6-9) are Q0, Q1, Q2, and Q3. The bottom pins (10-13) are Q0, Q1, Q2, and Q3. The left pins (14-16) are NC, VDD, and NC. The chip is labeled A5605F.



NAME	X	Y
V _{SS}	285	155
XT	485	155
Q ₀	710	155
Q ₁	1060	155
Q ₂	1350	395
Q ₃	1350	675
Q ₄	1350	930
CE	1350	1245
V _{DD}	1045	1245
XT	845	1245
INH	465	1245
XT	155	1245
NC	155	955
V _{DD}	155	755
XT	155	555
NC	155	355

NAME	FUNCTION
XT	Input terminal for oscillating
$\overline{\text{XT}}$	Output terminal for oscillating
INH	"L" Standby mode On chip pull-up resistance
$\overline{\text{CE}}$	Output control for divided frequency Pull-up resistance
V _{DD}	Power-supply
V _{SS}	Ground
Q ₀	Output terminal for fundamental frequency
Q ₁₋₄	Output terminal for divided frequency

■ ABSOLUTE MAXIMUM RATING ($V_{SS}=0V$)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V_{DD}	$V_{SS}-0.5$ to $V_{SS}+7.0$	V
Input voltage	V_{IN}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Output voltage	V_{OUT}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Storage temperature	T_{STG}	-65 to +150	°C

■ RECOMMENDED OPERATIONAL CONDITIONS ($V_{SS}=0V$)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Operating voltage	V_{DD}	3		6	V
Input voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	T_{OPR}	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

 $V_{DD}=5V$, $T_a=-40^{\circ}C \sim +85^{\circ}C$

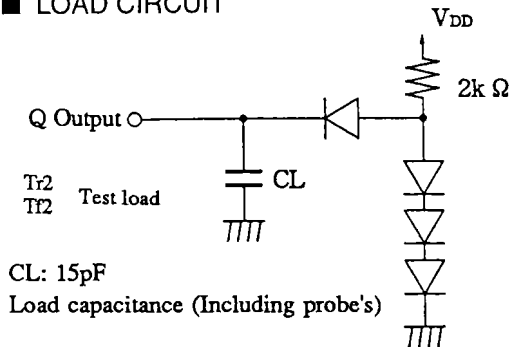
ITEM	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Output current 1 ("H" level)	I _{OH1}	Exclude $\overline{XT}$ terminal	V _{DH} = 0.9V _{DD}	1.0			mA
Output current 1 ("L" level)	I _{OL1}	Fig. 1, V _{DD} = -5V ±0.5V	V _{OL} =0.1V _{DD}	3.2			
Output current 2 ("H" level)	I _{OH2}	Exclude XT terminal	V _{OH} =2.4V	1.0			mA
Output current 2 ("L" level)	I _{OL2}	Fig. 1, V _{DD} =5V ±0.5V	V _{OL} =0.4V	3.2			
Output current 3 ("H" level)	I _{OH3}	V _{OH} =4.5V	Ta=25°C, V _{DD} = 5V	3.5	5	6.5	mA
Output current 3 ("L" level)	I _{OL3}	V _{OL} =0.5V	XT terminal, Fig. 6	3.5	5	6.5	
Input voltage ("H" level)	V _{IH}	INH, CE terminal		0.8V _{DD}			V
Input voltage ("L" level)	V _{IL}	V _{DD} = -5V ±0.5V				0.2V _{DD}	
Input bias voltage	V _{XBS}	XT terminal Ta=25°C	Fig. 2	2.2	2.5	2.8	mA
Current consumption 1	I _{DD1}	CE, INH=OPEN	Fig. 3		4.5	6.5	
Current consumption 2	I _{DD2}	CE="L", INH=OPEN	Fig. 3		3.5	5.5	
Current consumption 3	I _{DD3}	INH="L", CE=OPEN			0.1	0.4	
Pull-up resistance	R _{UP}	Ta=25°C	Fig. 4	20	40	80	kΩ
Feed back resistance	R _F	Ta=25°C	Fig. 5	1		5	MΩ
Internal capacitor	CG	f=1MHz		10	20	35	pF
	CD	f=1MHz		10	20	35	

■ SWITCHING CHARACTERISTICS $f=16MHz$ (Except $\overline{XT}$ terminal), $V_{DD}=-5V \pm 0.5V$, $T_a=25^{\circ}C$

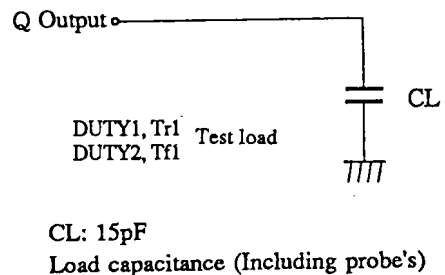
ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output rise time 1	T_{r1}	Fig. 3, Circuit-2, $0.1V_{DD} \rightarrow 0.9V_{DD}$		5	10	nS
Output rise time 2	T_{r2}	Fig. 3, Circuit-1, $0.4V_{DD} \rightarrow 2.4V_{DD}$		5	10	
Output fall time 1	T_{f1}	Fig. 3, Circuit-2, $0.9V_{DD} \rightarrow 0.1V_{DD}$		5	10	nS
Output fall time 2	T_{f2}	Fig. 3, Circuit-1, $2.4V_{DD} \rightarrow 0.4V_{DD}$		5	10	
Duty of fundamental output	$DUTY_1$	Fig-3, Circuit-2, $V_{DD}=5V$	Q_0	40	60	%
Duty of divided output	$DUTY_2$		Q_1 to Q_4	45	55	
Output delay time 1	T_{PLH1}	Q_1 output monitor		30	60	nS
Output delay time 1	T_{PHL1}	$V_{DD}=5V$ at INH		35	70	
Output delay time 2	T_{PLH2}	Q_1 output monitor		70	140	nS
Output delay time 2	T_{PHL2}	$V_{DD}=5V$ at CE		70	140	

 f_0 : Input frequency to XT terminal

■ LOAD CIRCUIT



Circuit-1



Circuit-2

■ TEST CIRCUIT

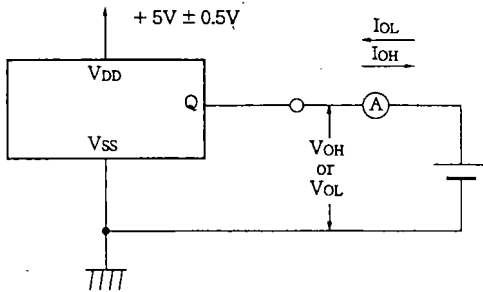


Fig. 1

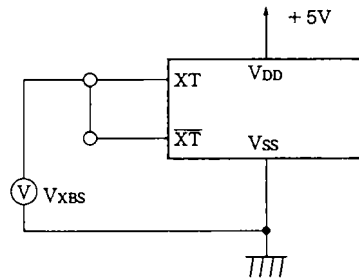


Fig. 2

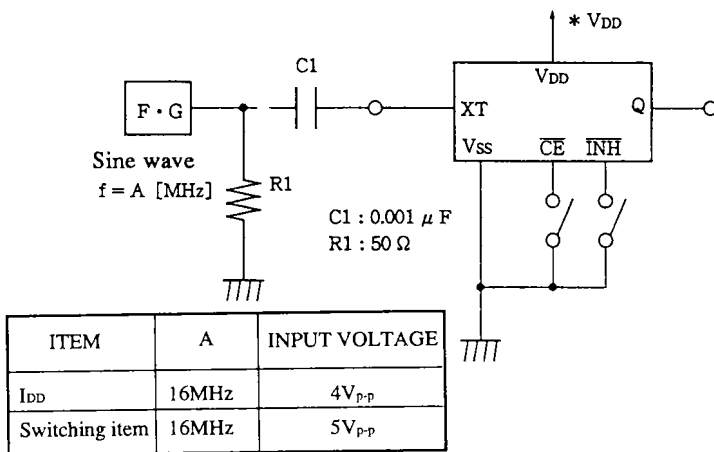
* Test of I_{DD} $V_{DD}=5V$ * Test of switching characteristics $V_{DD}=5V \pm 0.5V$ 

Fig. 3

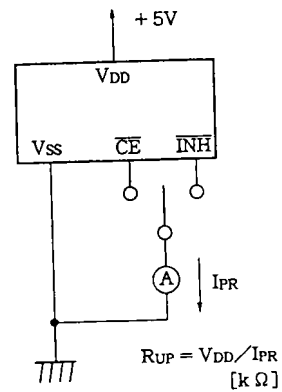


Fig. 4

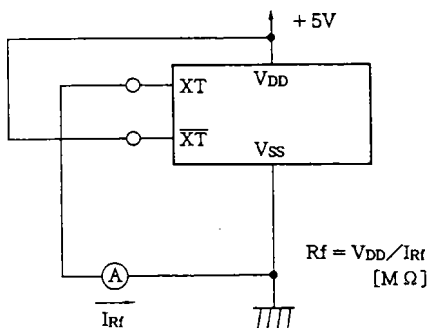


Fig. 5

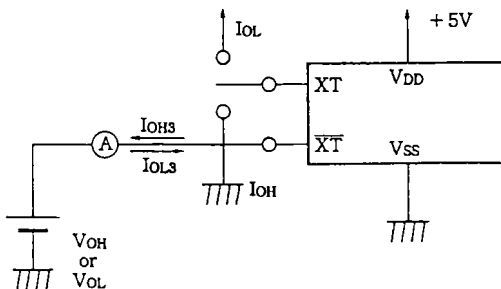
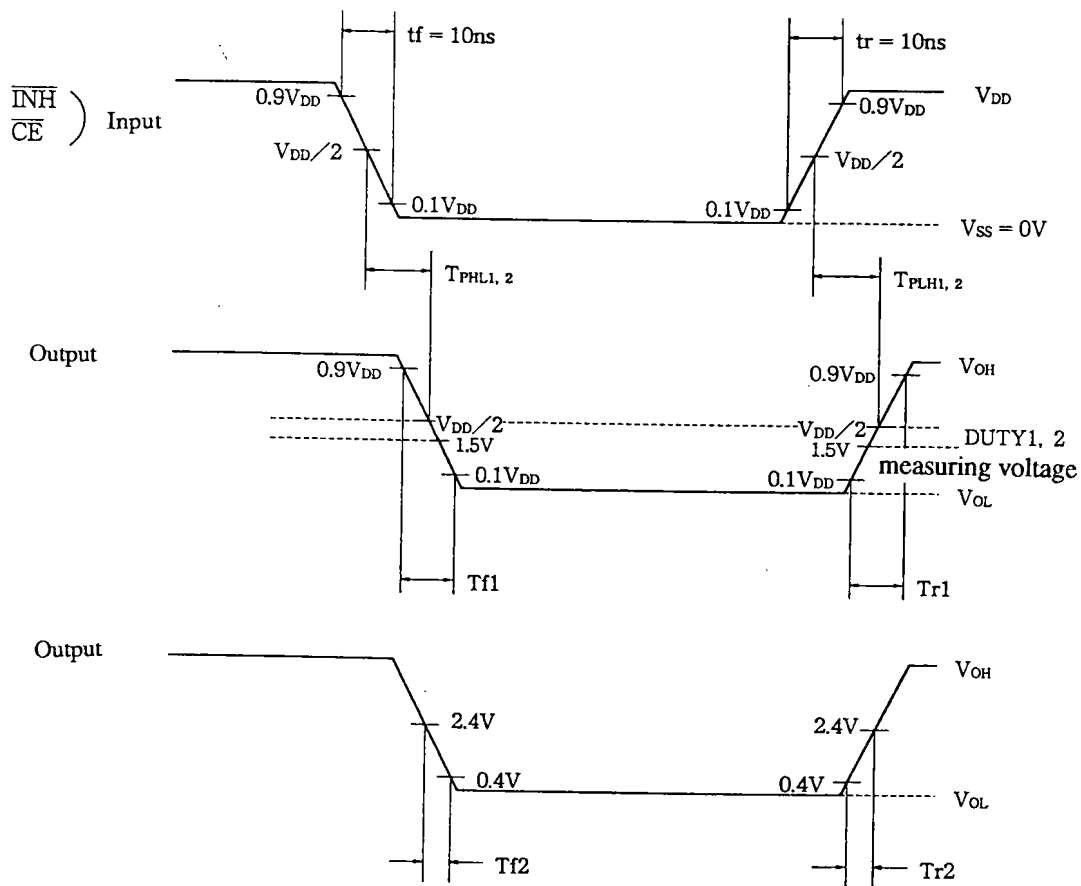


Fig. 6

■ WAVEFORMS FOR SWITCHING TIME



■ SERIES TABLE

SERIES	Built-in capacity type
SM5605FA	No capacity
SM5605FC	CD, CG=20pF (TYP.)

■ FUNCTIONAL TABLE

$\overline{\text{INH}}$	$\overline{\text{CE}}$	Q_0	Q_1	Q_2	Q_3	Q_4
H or OPEN	H or OPEN	f_0	$f_0/2$	$f_0/4$	$f_0/8$	$f_0/16$
H or OPEN	L	f_0	L	←	←	←
L	H or OPEN	L	←	←	←	←
L	L	L	←	←	←	←