SL6140

400MHz Wideband AGC Amplifier

DS2159 ISSUE 5.0 July 1999

Features

- 400MHz Bandwidth (R_L=50Ω)
- High voltage Gain 45dB (R_L=1kΩ)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Surface Mount Plastic Package
- Low Cost

Applications

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

Description

The SL6140 is an integrated broadband AGC amplifier, designed on an advanced bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz. Gain control is also provided with over 70dB of dynamic range. The SL6140 offers over 45dB of voltage gain with an R_L of 1kΩ.

Ordering Information
SL6140/NA/MP
Industrial temperature range miniature plastic package
SL6140/NA/MPTC
Tape and Reel

The SL6140 (Figure 3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor (R_{AGC}), the value of which adjusts the curve of gain reduction versus control voltage (see Figure 4). As the output stage of the amplifier is an open collector the maximum voltage gain is determined by R_L. With load resistance of 1kΩ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB ($20\log_{10} V_{OUT}/V_{IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for R_L = 1kΩ, as compared with 400MHz for R_L = 50Ω. R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Figure 7 through to 10 show the typical S parameters for the device. Figures 11 and 12 show the typical variation in 3rd order intercept performance with AGC.

In any application, the substrate should be connected to the most negative point in the circuit, usually to the same point as pin 3.

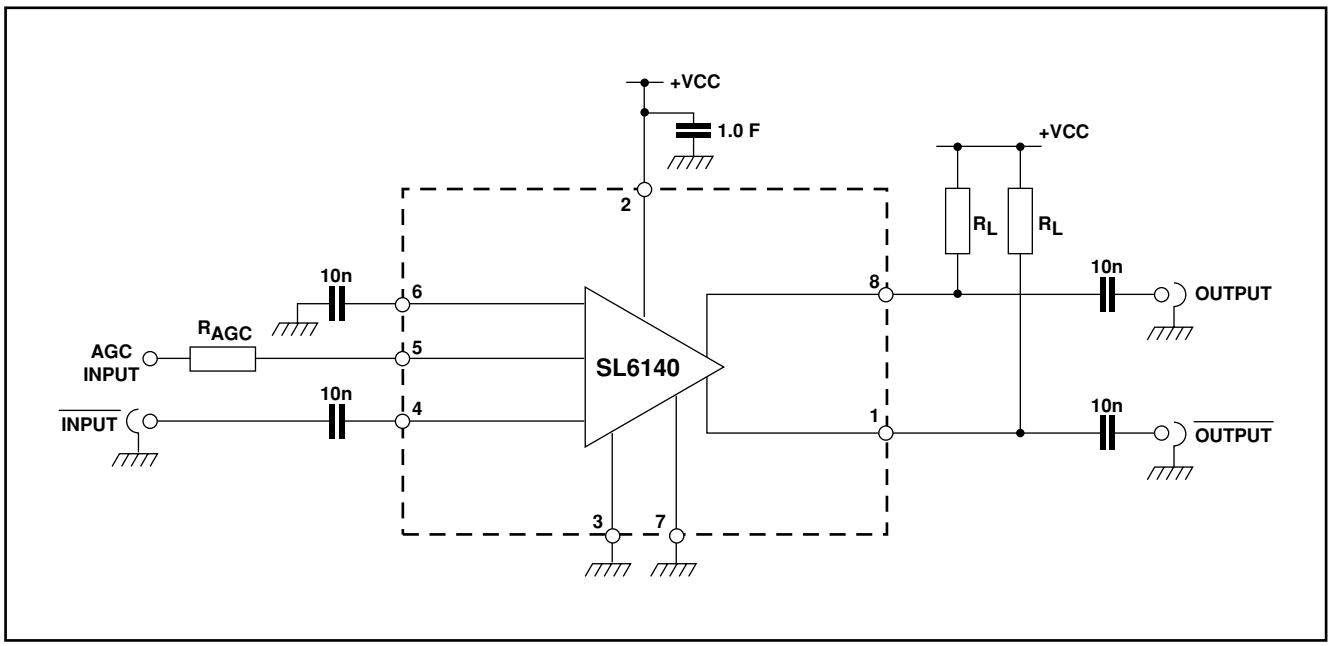


Figure 1 - Typical Application

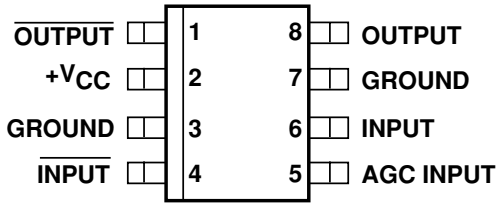


Figure 2 - Pin Connections Diagram (top view)

Electrical Characteristics

T_{amb} = 25°C, V_{CC} = 12V +5%, V_{IN} = 1mV_{RMS}, Frequency = 6MHz, Load (R_L) = 10KOHms, R_{AGC} = 22KOHm
These characteristics are guaranteed over the following conditions (unless otherwise stated)

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	5,6,7		19	23	mA	No input signal
Output stage current	5,6 (sum)	5	7	9	mA	No input signal
Output current matching (magnitude of difference of output currents)	5,6		1.0		mA	
AGC range	2	60	75		dB	See Figure 4 & Note 1 (VAGC = 0V to 10V)
Voltage gain (single ended)	5,6 5,6	40	45 55 15		dB dB dB	R_L = 1kΩ See Figure 5 & Note 1 Tuned input and output R_L = 50Ω
Bandwidth (-3dB)	5,6		25 400		MHz	RL = 1kΩ See Figure 5 RL = 50Ω
Maximum output level (single ended) 0dB AGC -30dB AGC	 5,6 5,6		 3.5 3.5		 V p-p V p-p	 Note 1 R_L = 1kΩ. Note 1
Noise figure	5,6		5		dB	Test CCT Figure 13

Note. 1 Guaranteed but not tested.

Absolute Maximum Ratings

Supply voltage, V_{CC}		+18V
Input voltage (differential)		+5V
AGC supply		V_{CC}
Storage temperature		-55°C to +150°C
Operating temperature range		
SL6140	MP	-40°C to +85°C at 200mW
Chip operating temperature		
SL6140	MP	+150°C

Thermal Resistance

Chip-to-ambient		
SL6140	MP	163°C/W
Chip-to-case		
SL6140	MP	57°C/W

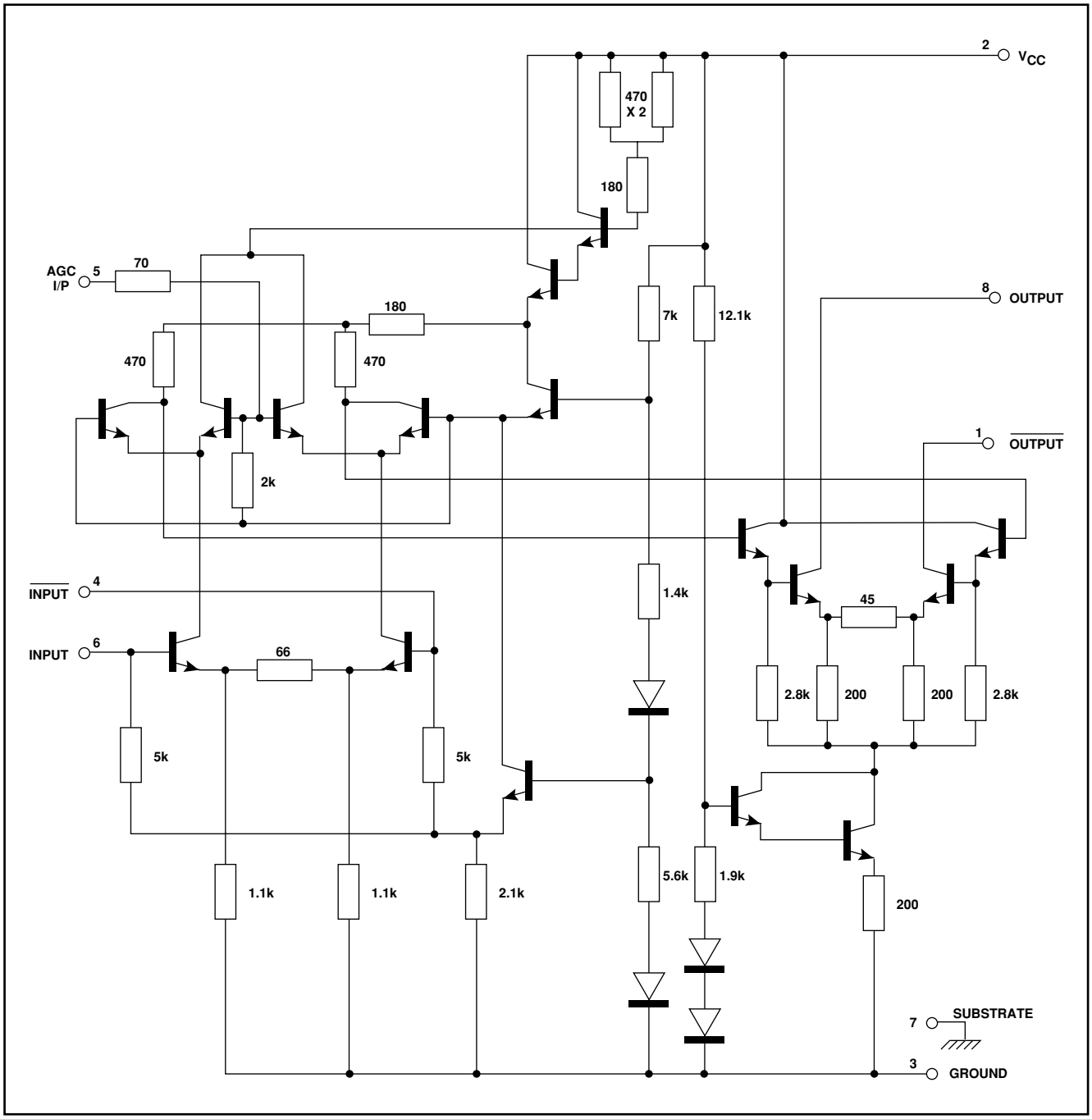


Figure 3 - Full Circuit Diagram of SL6140

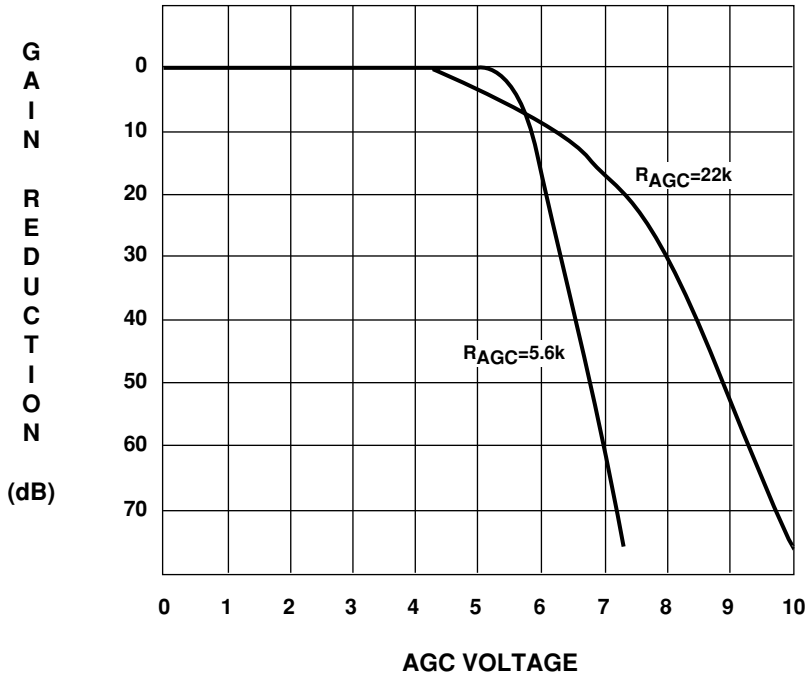


Figure 4 - Gain Reduction v. AGC Voltage

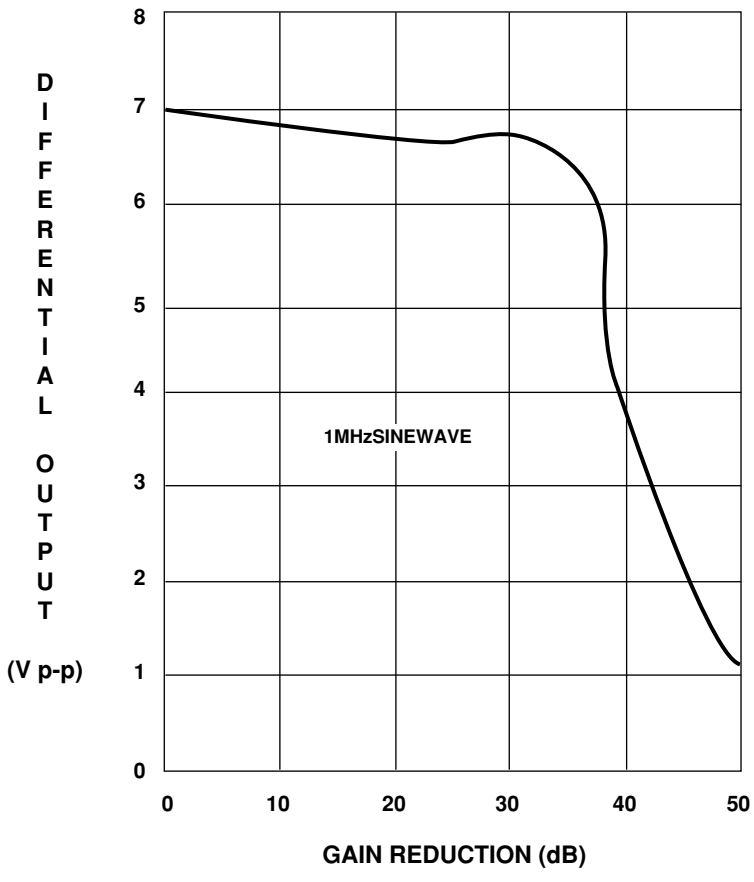


Figure 5 - Max Differential O/P Voltage v. Gain Reduction

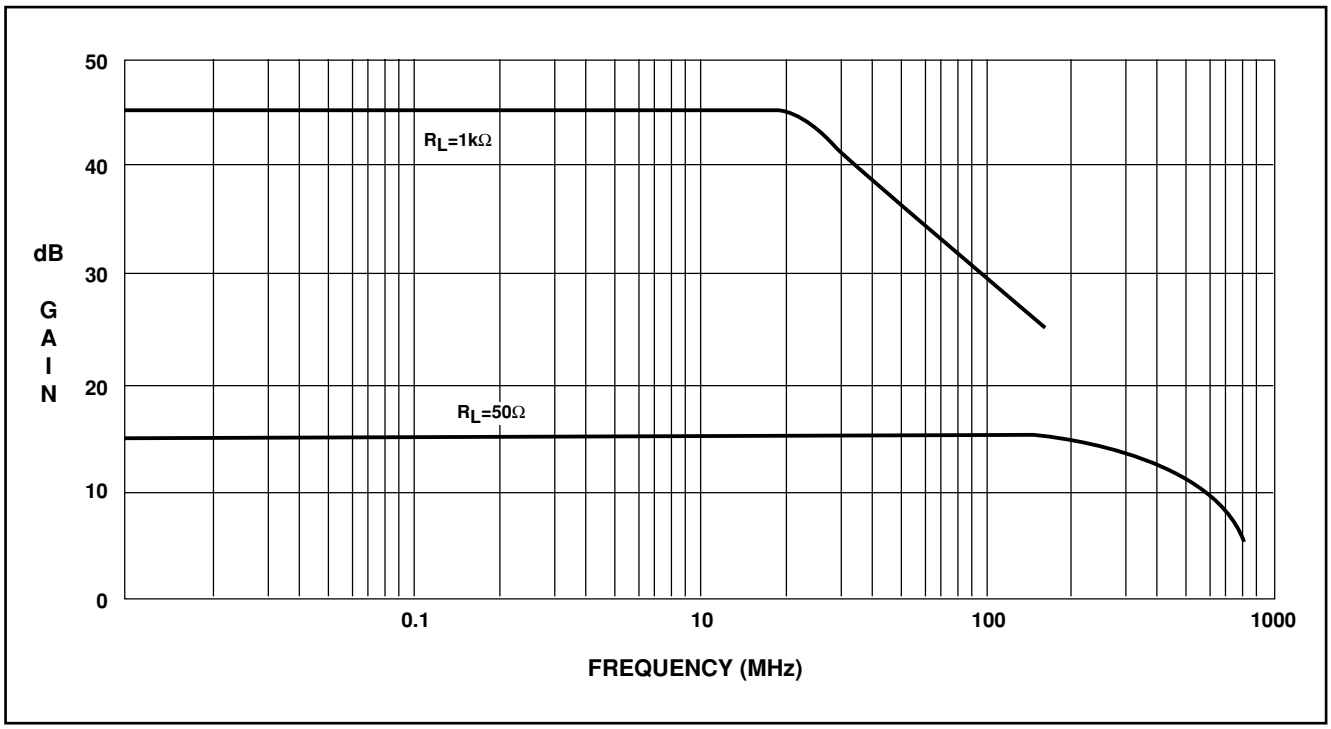


Figure 6 - Voltage Gain v. Frequency

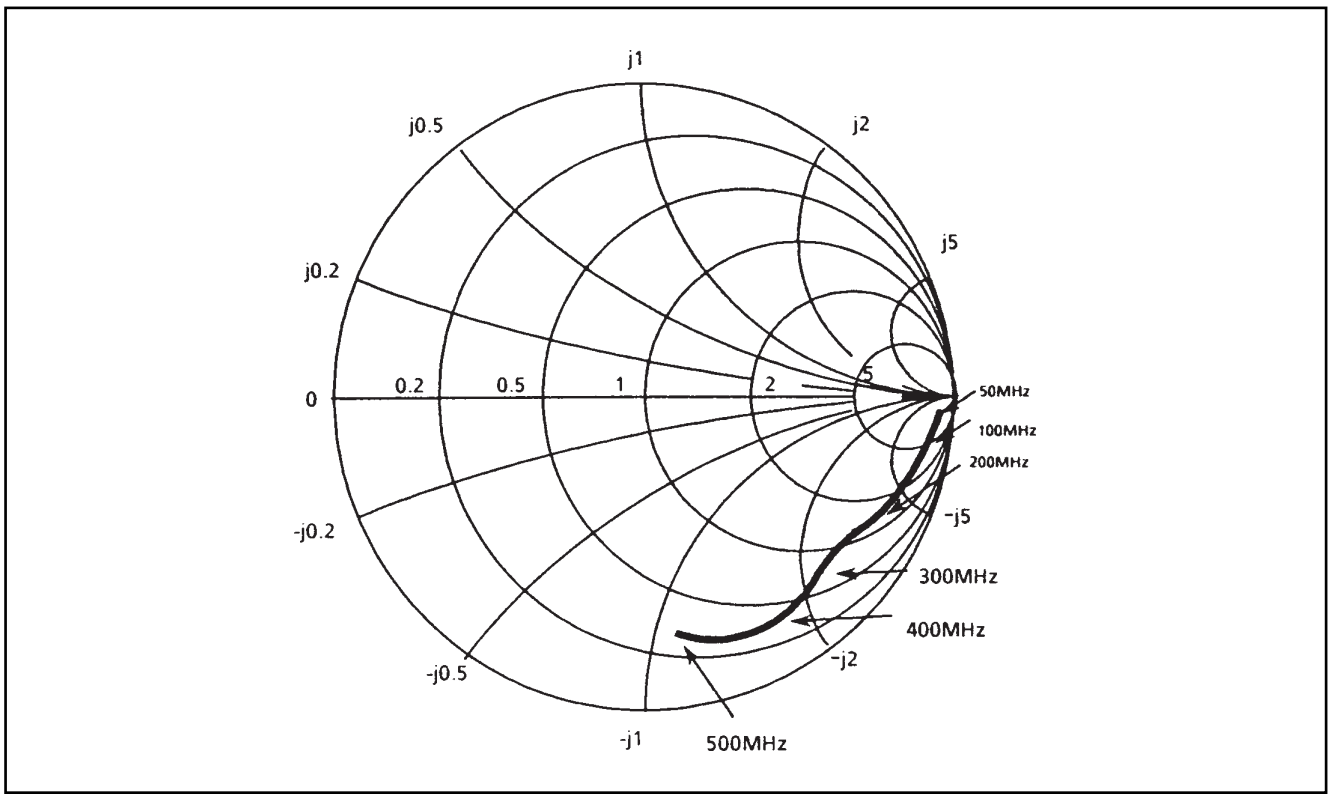


Figure 7 - Input Impedance 50Ω System

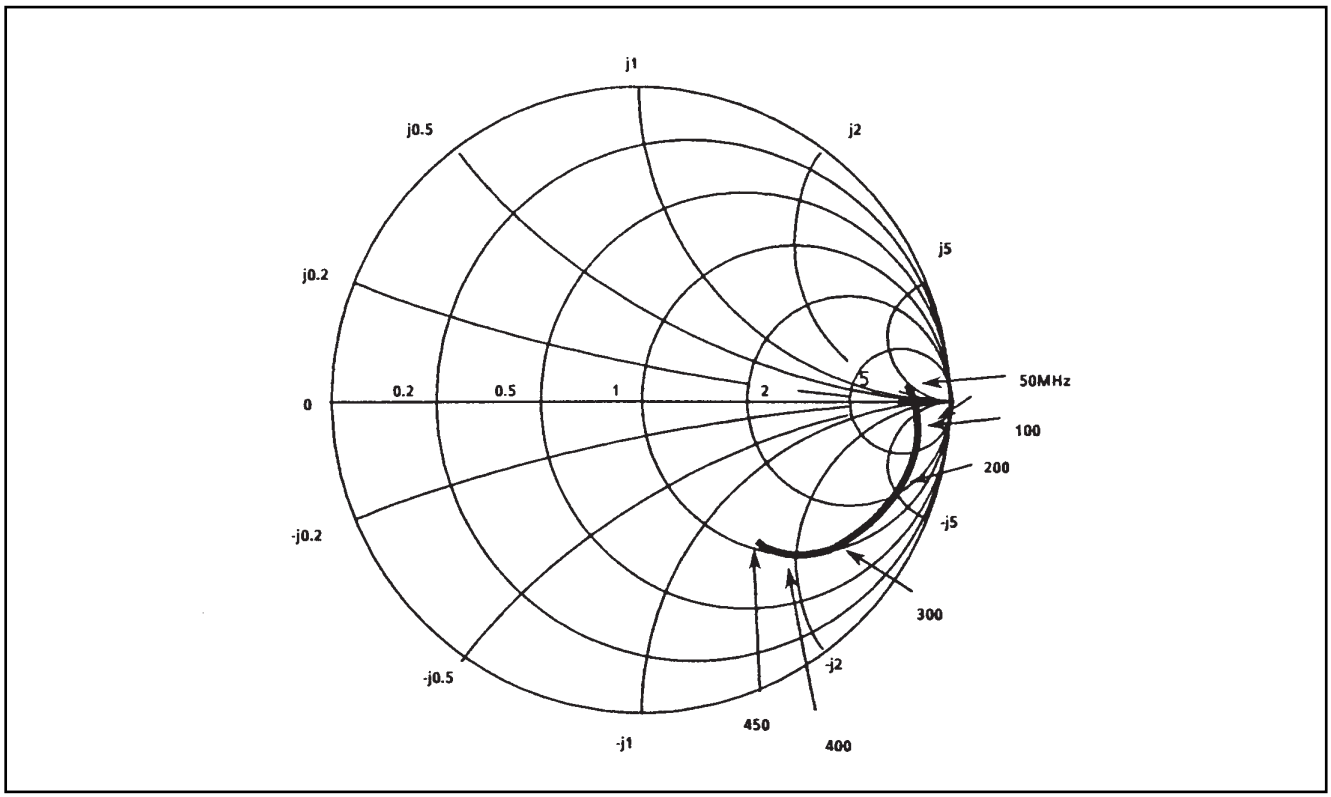


Figure 8 - Output Impedance 50Ω System

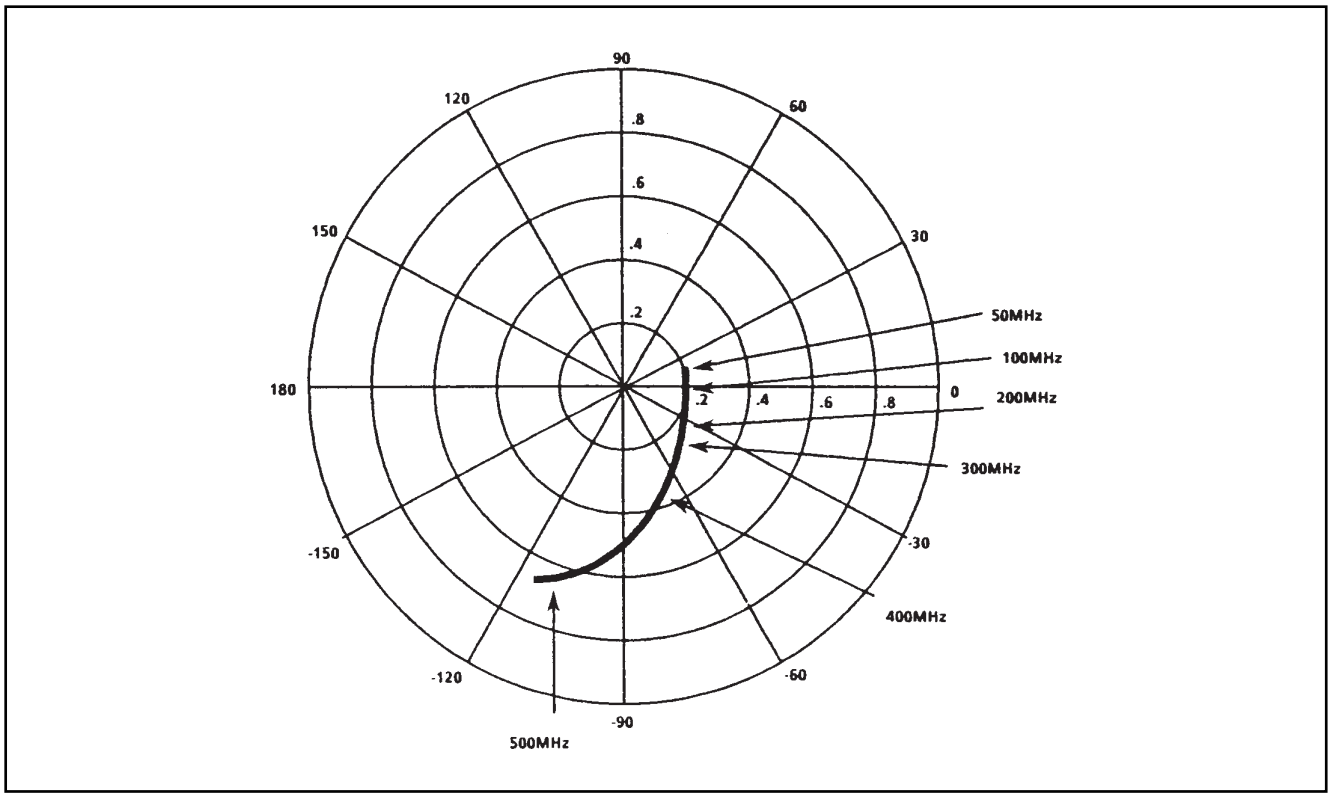


Figure 9 - Reverse Transmission Coefficient S_{12} SL6140

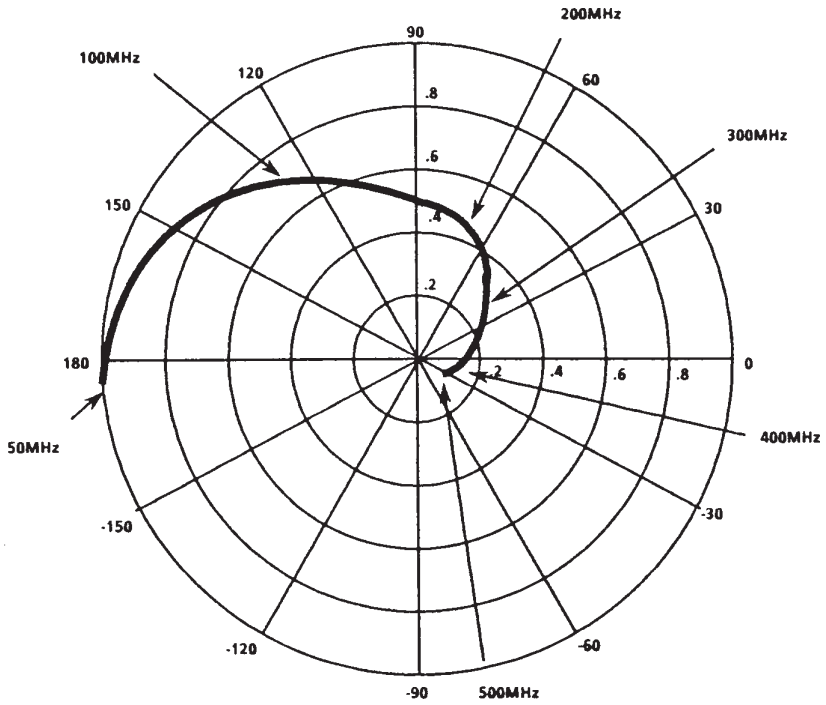


Figure 10 - Forward Transmission Coefficient S_{12} SL6140

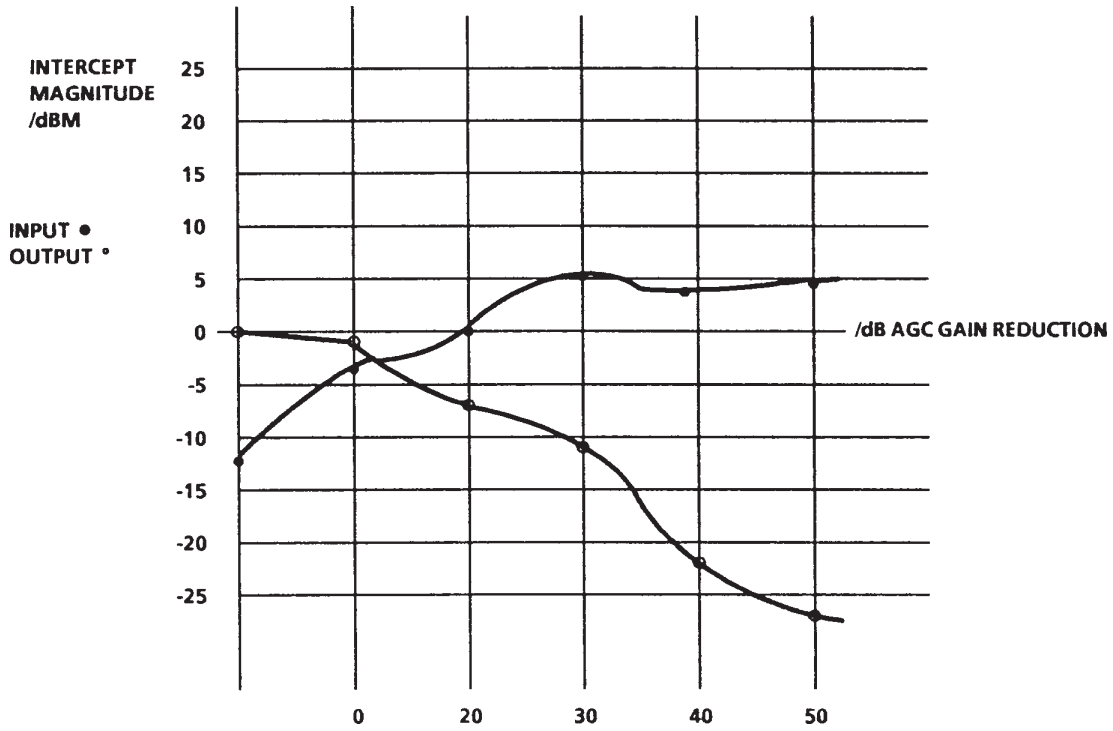


Figure 11 3rd Order Intercept Point Against Gain Reduction At 250.0MHz and 254.0MHz

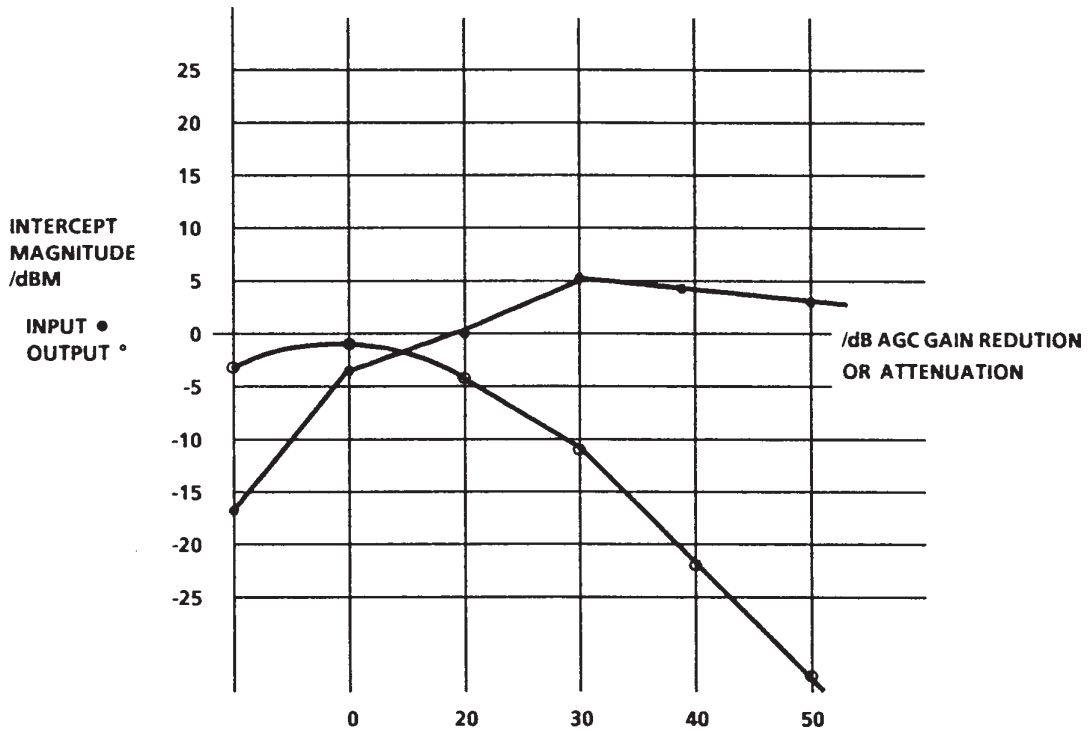
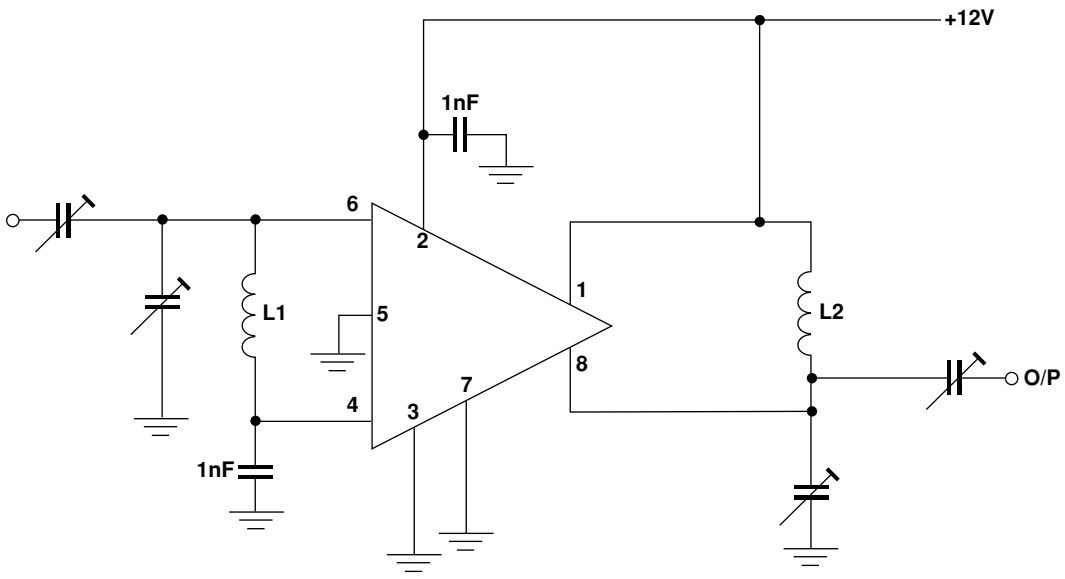
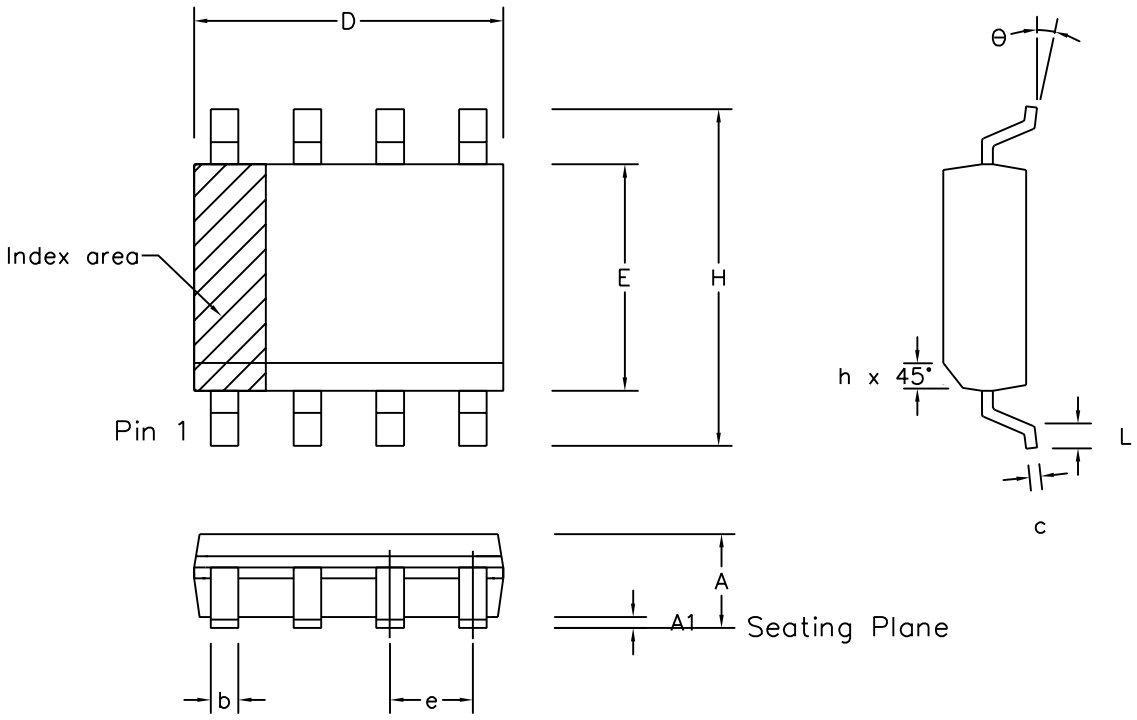


Figure 12 - 3rd Order Intercept Point Against Gain Reduction At 100.0MHz and 104.0MHz



VARIABLE CAPS 3-25pF
L1 7 TURNS # 18 SWG 8mm DIA 16mm LONG
L2 6 TURNS # 16 SWG 14mm DIA 19mm LONG

Figure 13 - 50MHz Noise Figure Test Circuit



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

GPD00010

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE