N-Channel Reduced Q$_g$, Fast Switching MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C$_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC
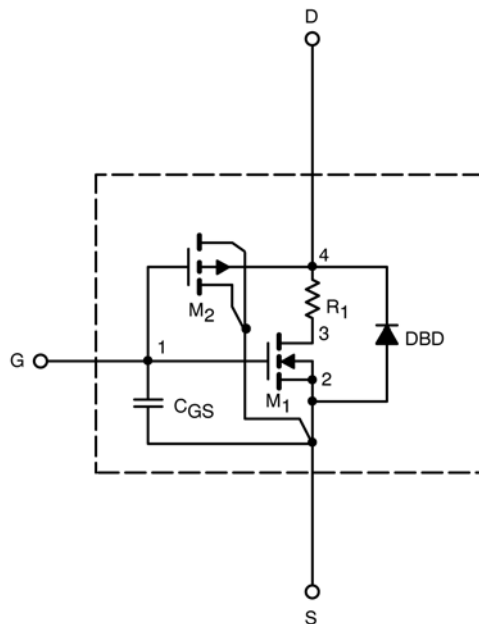
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T$_J$ = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$ = V$_{GS}$, I$_D$ = 250 µA	1.1		V
On-State Drain Current[a]	I$_{D(on)}$	V$_{DS}$ ≥ 5 V, V$_{GS}$ = 10 V	838		A
Drain-Source On-State Resistance[a]	r$_{DS(on)}$	V$_{GS}$ = 10 V, I$_D$ = 16 A	0.0054	0.0058	Ω
		V$_{GS}$ = 4.5 V, I$_D$ = 13 A	0.0080	0.0080	
Forward Transconductance[a]	g$_{fs}$	V$_{DS}$ = 15 V, I$_D$ = 16 A	49	38	S
Diode Forward Voltage[a]	V$_{SD}$	I$_S$ = 3 A, V$_{GS}$ = 0 V	0.74	0.74	V
Dynamic[b]					
Total Gate Charge	Q$_g$	V$_{DS}$ = 15 V, V$_{GS}$ = 5 V, I$_D$ = 16 A	16	16.3	nC
Gate-Source Charge	Q$_{gs}$		4	4	
Gate-Drain Charge	Q$_{gd}$		5.9	5.9	
Turn-On Delay Time	t$_{d(on)}$	V$_{DD}$ = 15 V, R$_L$ = 15 Ω I$_D$ ≅ 1 A, V$_{GEN}$ = 10 V, R$_G$ = 6 Ω	12	14	ns
Rise Time	t$_r$		10	10	
Turn-Off Delay Time	t$_{d(off)}$		28	44	
Fall Time	t$_f$		26	20	
Source-Drain Reverse Recovery Time	t$_{rr}$	I$_F$ = 3 A, di/dt = 100 A/µs	32	40	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA (T$_J$=25°C UNLESS OTHERWISE NOTED)
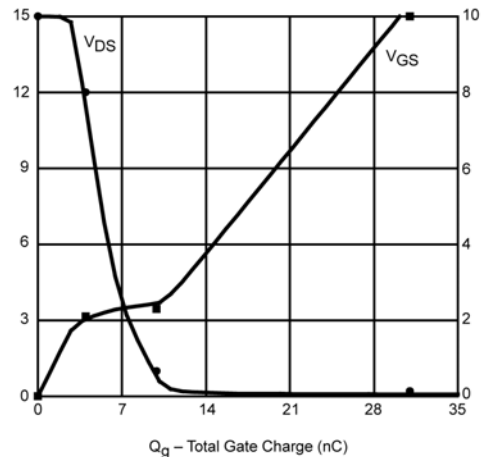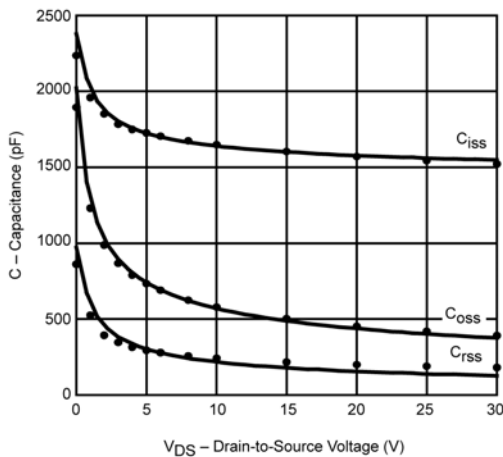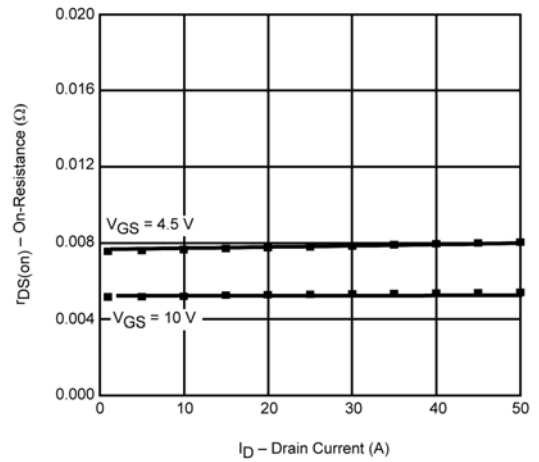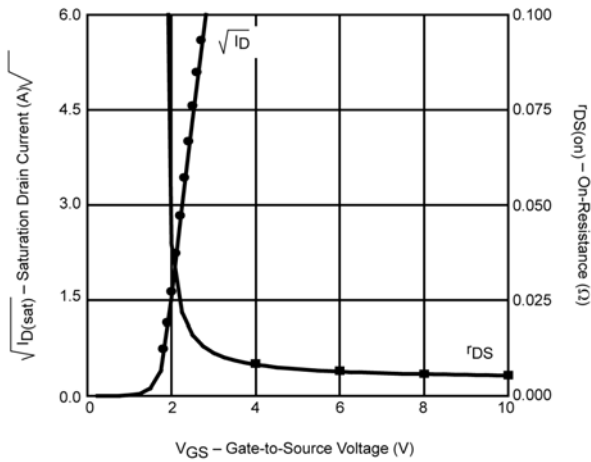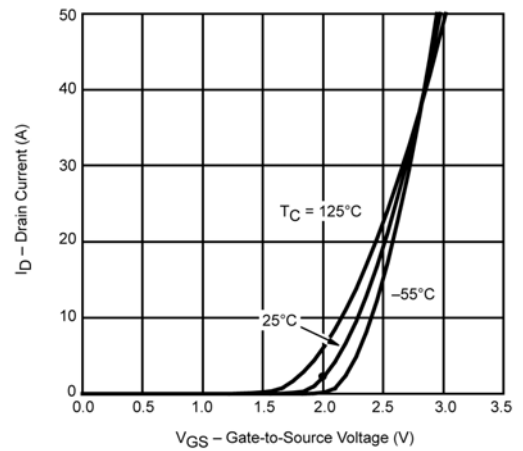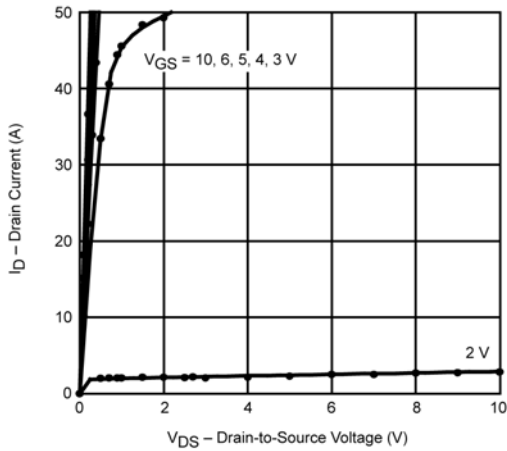
Note: Dots and squares represent measured data.