XC9500XV Family High-Performance CPLD

DS049 (v2.0) January 15, 2001

Advance Product Specification

Features

- Optimized for high-performance 2.5V systems
  - 3.5 ns pin-to-pin logic delays
  - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
  - Lower power operation
  - Multi-voltage operation
  - FastFLASH technology
- Advanced system features
  - In-system programmable
  - Output banking (XC95144XV, XC95288XV)
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 10,000 program/erase cycles endurance rating
  - 20 year data retention
- Pin-compatible with 3.3V core XC9500XL family in common package footprints
- Hot Plugging capability

Family Overview

The XC9500XV family is a 2.5V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where high device reliability and low power dissipation is important. Each XC9500XV device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XV family is designed to work closely with the Xilinx Spartan-XL and Virtex FPGA families, allowing system designers to partition logic optimally between fast interface circuitry and high-density general purpose logic. As shown in Table 1, logic density of the XC9500XV devices ranges from 800 to 6400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500XV family members are fully pin-compatible, allowing easy design migration across multiple density options in a given package footprint.

The XC9500XV architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. In-system programming throughout the full commercial operating range and a high programming endurance rating provide worry-free reconfigurations of system field upgrades. Extended data retention supports longer and more reliable system operating life.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. Each user pin is compatible with 3.3V, 2.5V, and 1.8V inputs, and the outputs may be configured for 3.3V, 2.5V, or 1.8V operation. The XC9500XV device exhibits symmetric full 2.5V output voltage swing to allow balanced rise and fall times.

Architecture Description

Each XC9500XV device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT II switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with extra wide 54 inputs and 18 outputs. The FastCONNECT II switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, up to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.

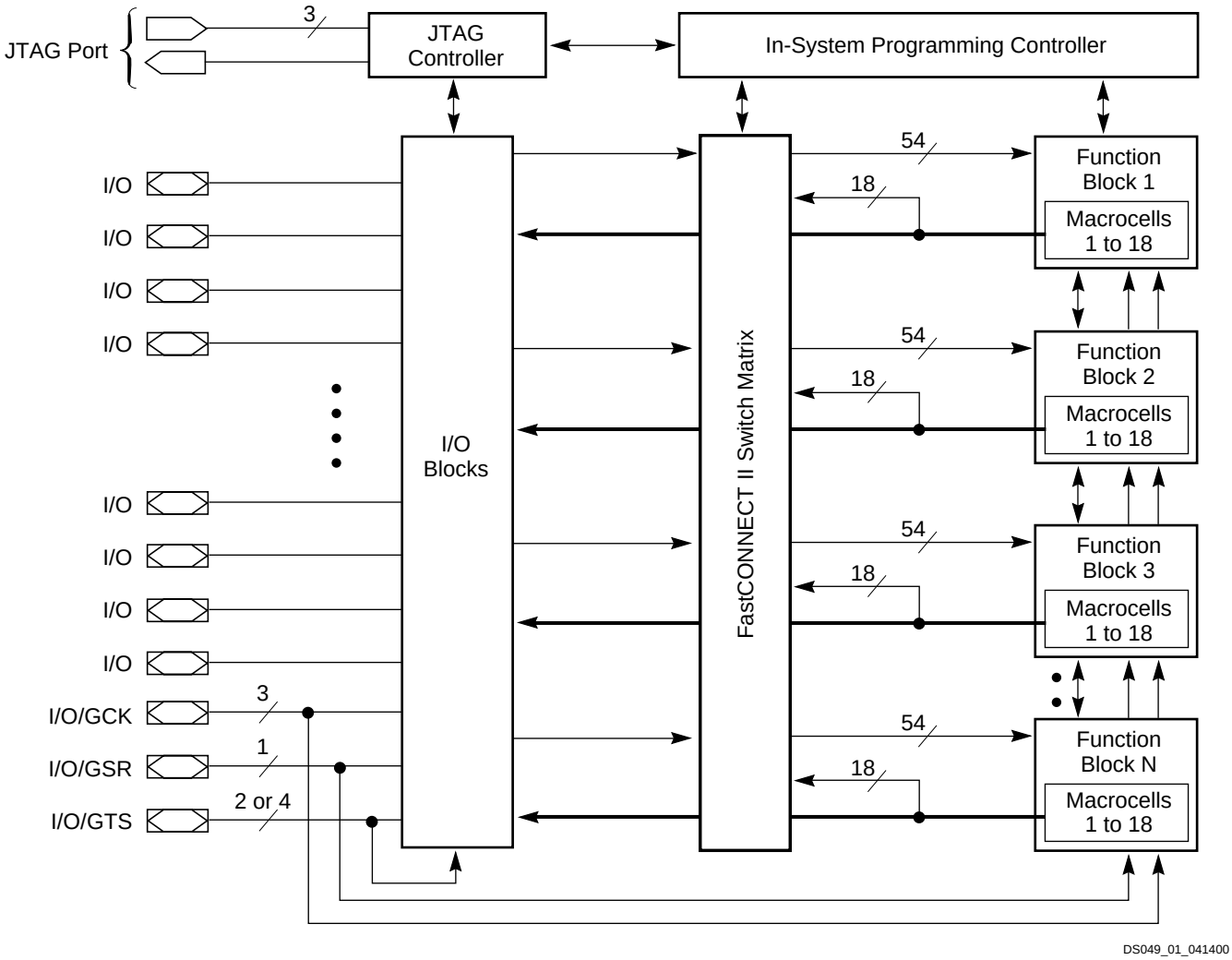

Figure 1: **XC9500XV Architecture**
Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

Table 1: **XC9500XV Device Family**

	XC9536XV	XC9572XV	XC95144XV	XC95288XV
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
T_{PD} (ns)	3.5	4	4	5
T_{SU} (ns)	2.8	3.1	3.1	3.7
T_{CO} (ns)	1.8	2.0	2.0	2.5
f_{SYSTEM} (MHz)	278	250	250	222
Output Banks	1	1	2	4

Table 2: **XC9500XV Packages and User I/O Pins (not including four dedicated JTAG pins)**

	XC9536XV	XC9572XV	XC95144XV	XC95288XV
44-pin PLCC	34	34	-	-
44-pin VQFP	34	34	-	-
100-pin TQFP	-	72	81	-
144-pin TQFP	-	-	117	117
208-pin PQFP	-	-	-	168
48-pin CSP	36	38	-	-
144-pin CSP	-	-	117	-
280-pin CSP	-	-	-	192
256-pin FBGA	-	-	-	192

Function Block

Each Function Block, as shown in Figure 2 is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT II switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Fifty-four inputs provide 108 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

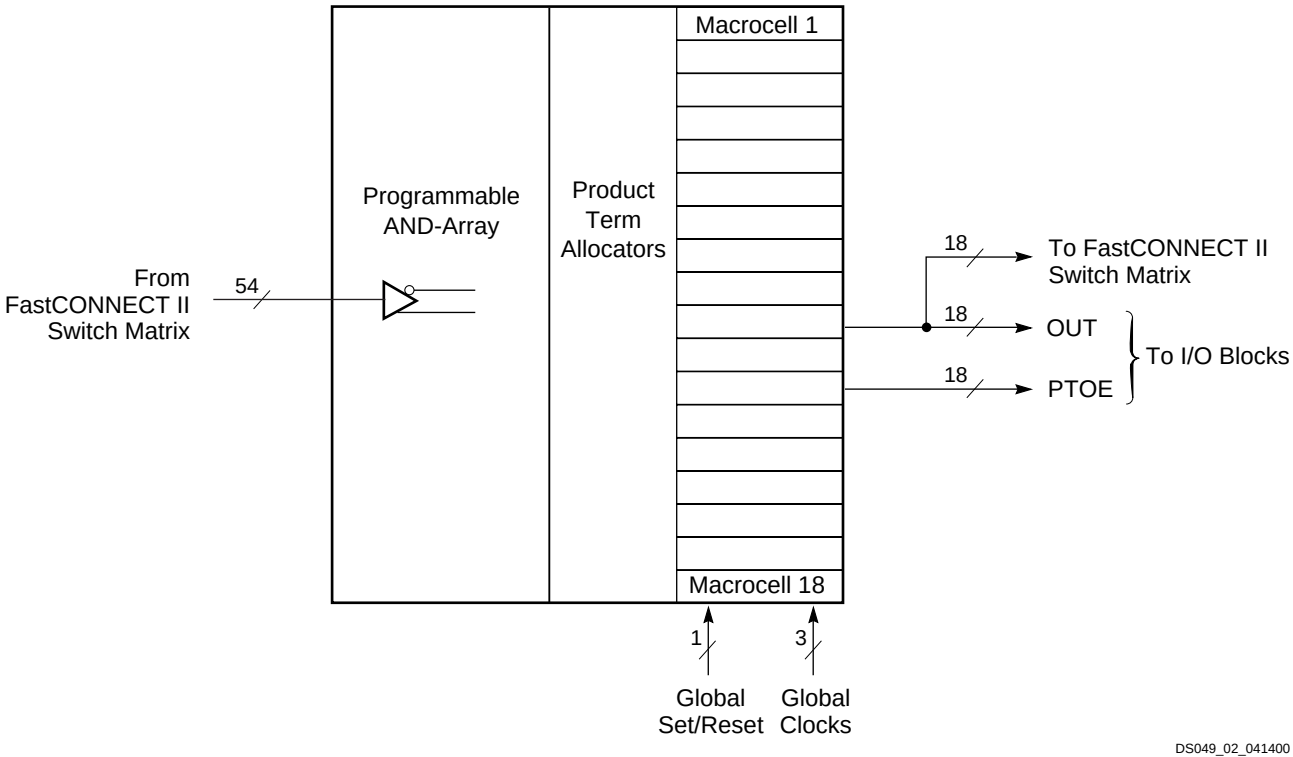

Figure 2: **XC9500XV Function Block**

Macrocell

Each XC9500XV macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, clock enable, set/reset, and output enable.

The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

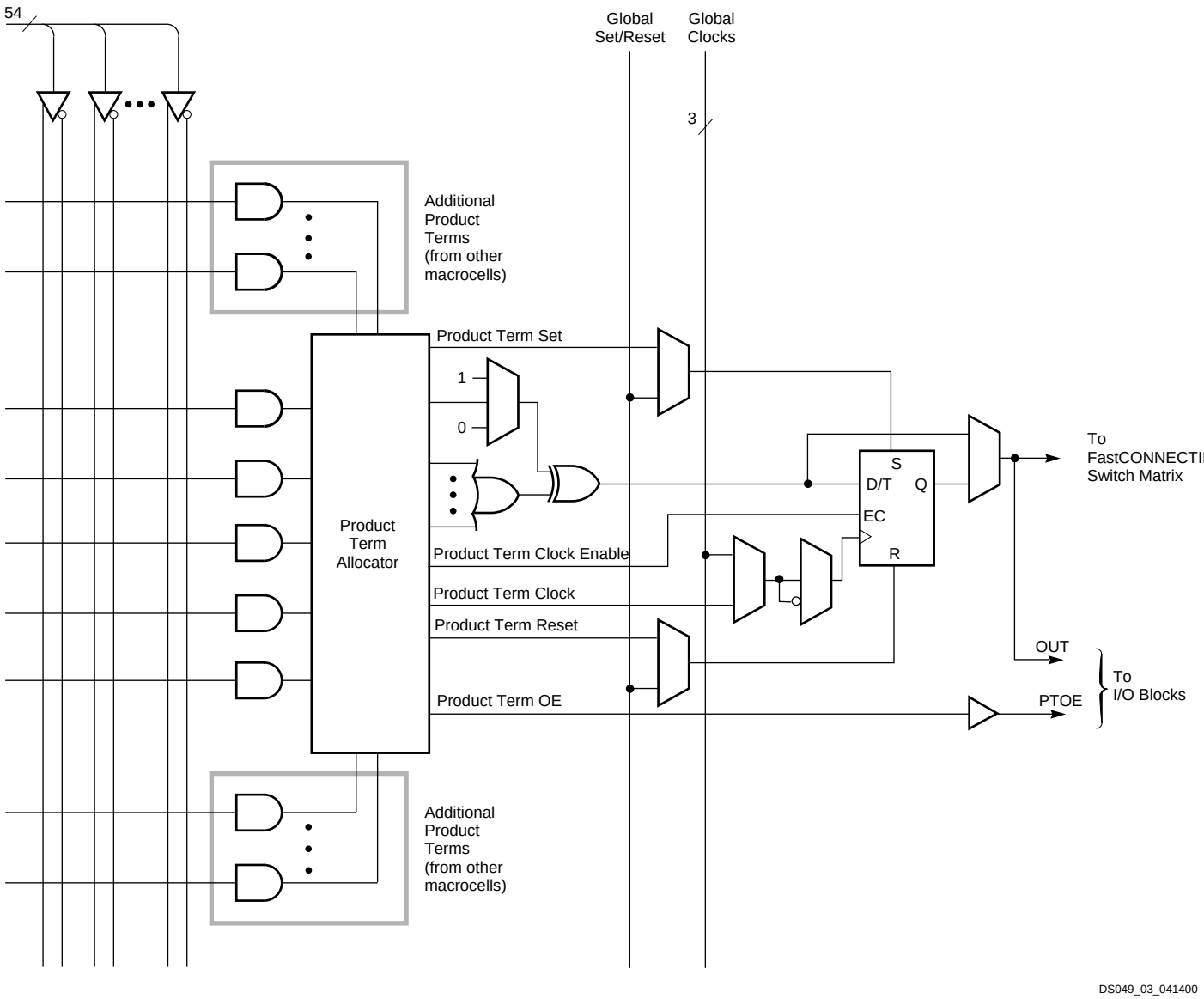

Figure 3: **XC9500XV Macrocell Within Function Block**
Note: See Figure 8 for additional clock enable details

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product term clock. Both true and complement polarities of the selected clock source can be used within each macrocell. A GSR input is also provided to allow user registers to be set to a user-defined state.

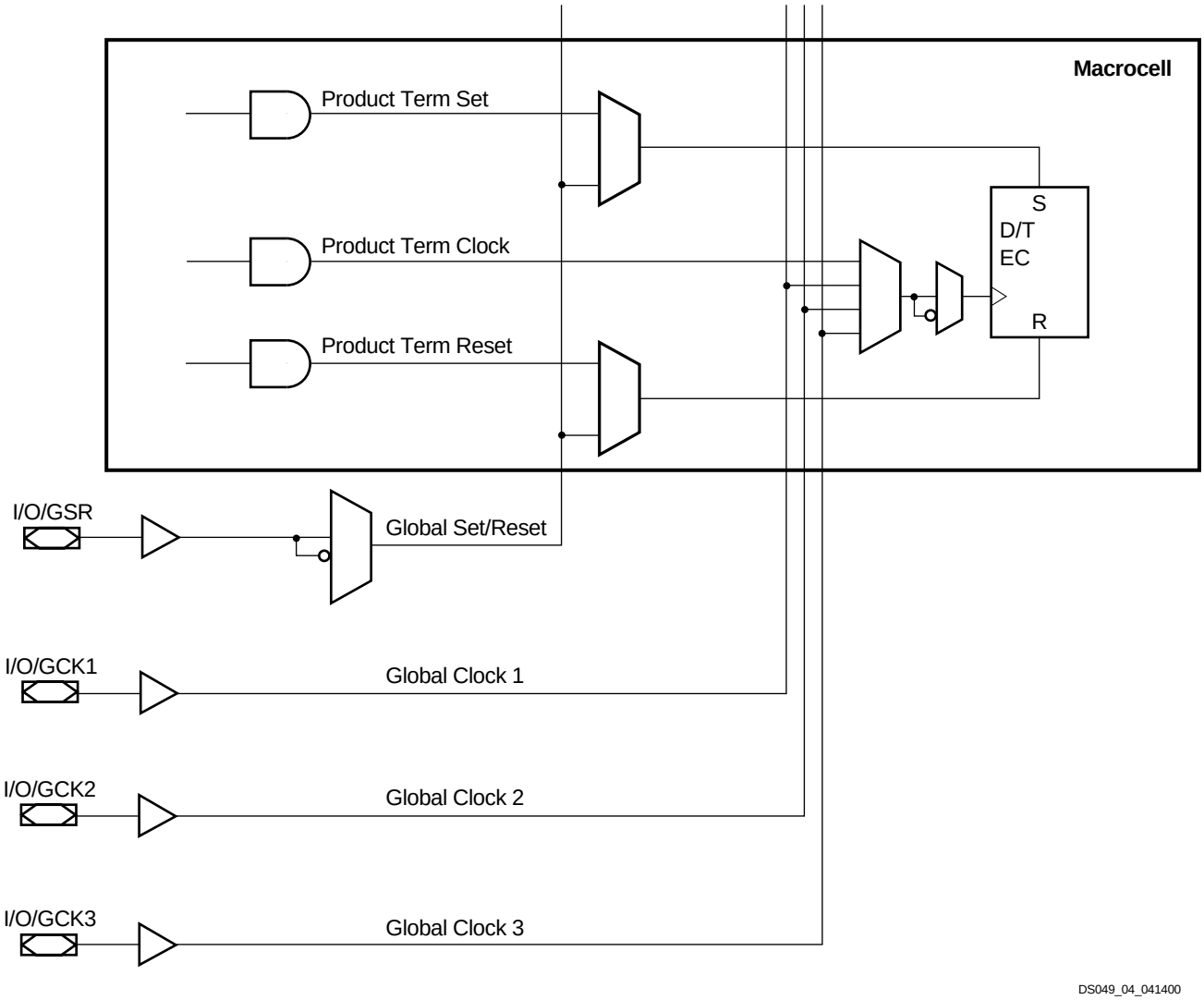

Figure 4: **Macrocell Clock and Set/Reset Capability**

Product Term Allocator

The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.

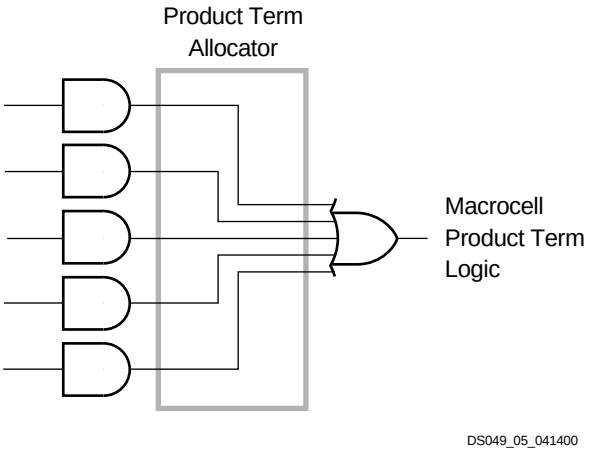

Figure 5: **Macrocell Logic Using Direct Product Term**

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of $T_{PTA,}$ as shown in Figure 6.

Note that the incremental delay affects only the product terms in other macrocells. The timing of the direct product terms is not changed..

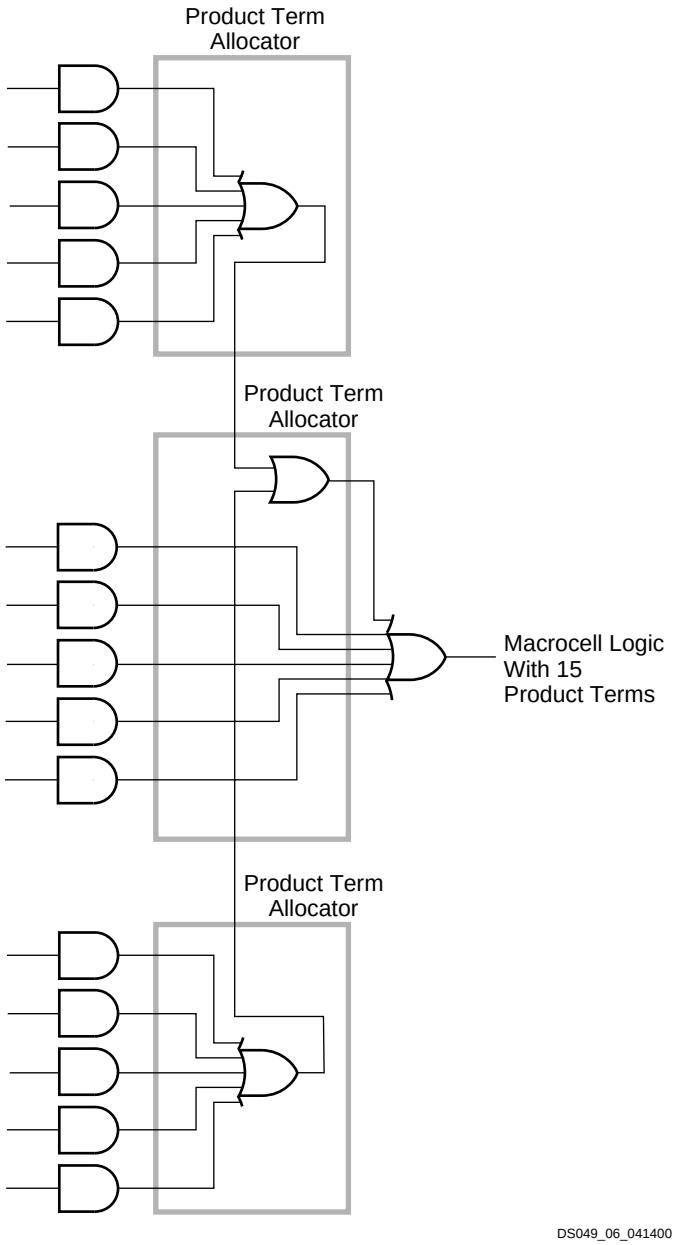

Figure 6: **Product Term Allocation With 15 Product Terms**

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7. In this example, the incremental delay is only $2*T_{PTA}$. All 90 product terms are available to any macrocell, with a maximum incremental delay of $8*T_{PTA}$.

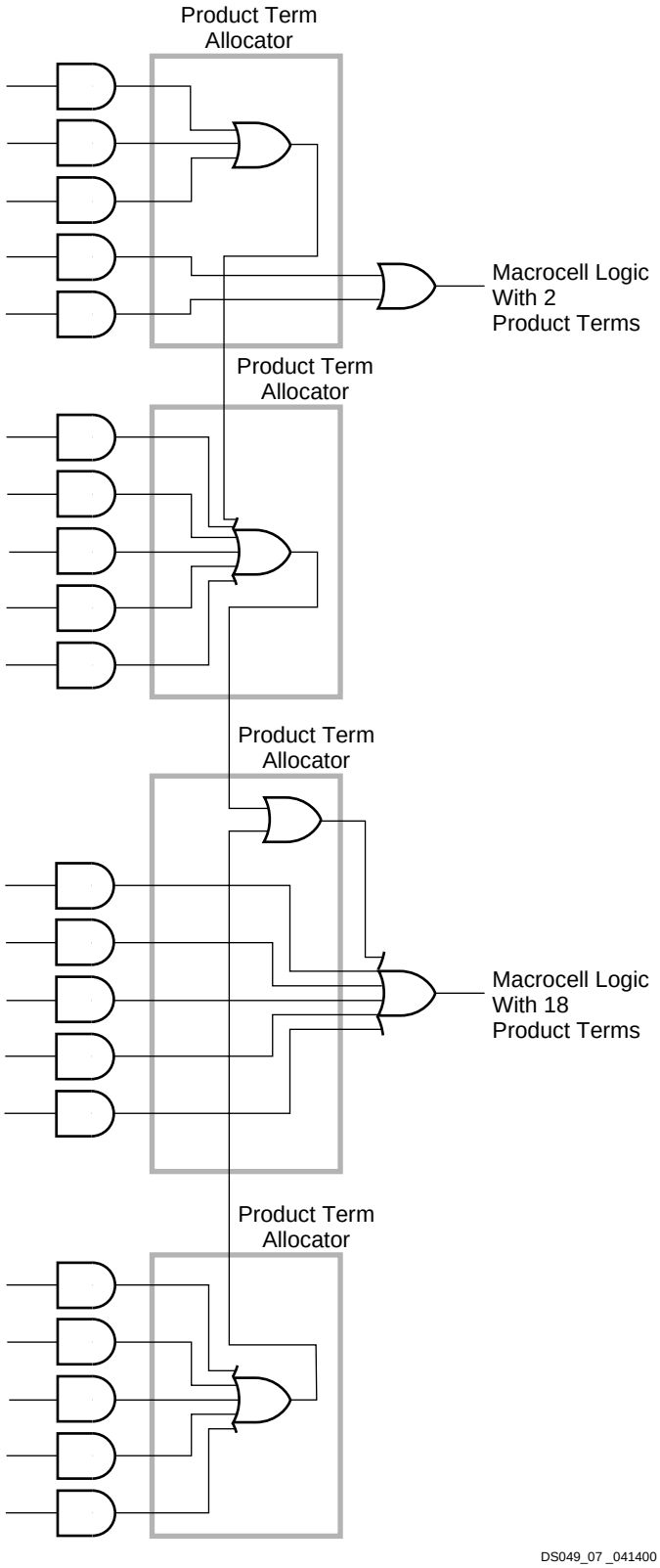

Figure 7: **Product Term Allocation Over Several Macrocells**

The internal logic of the product term allocator is shown in Figure 8.

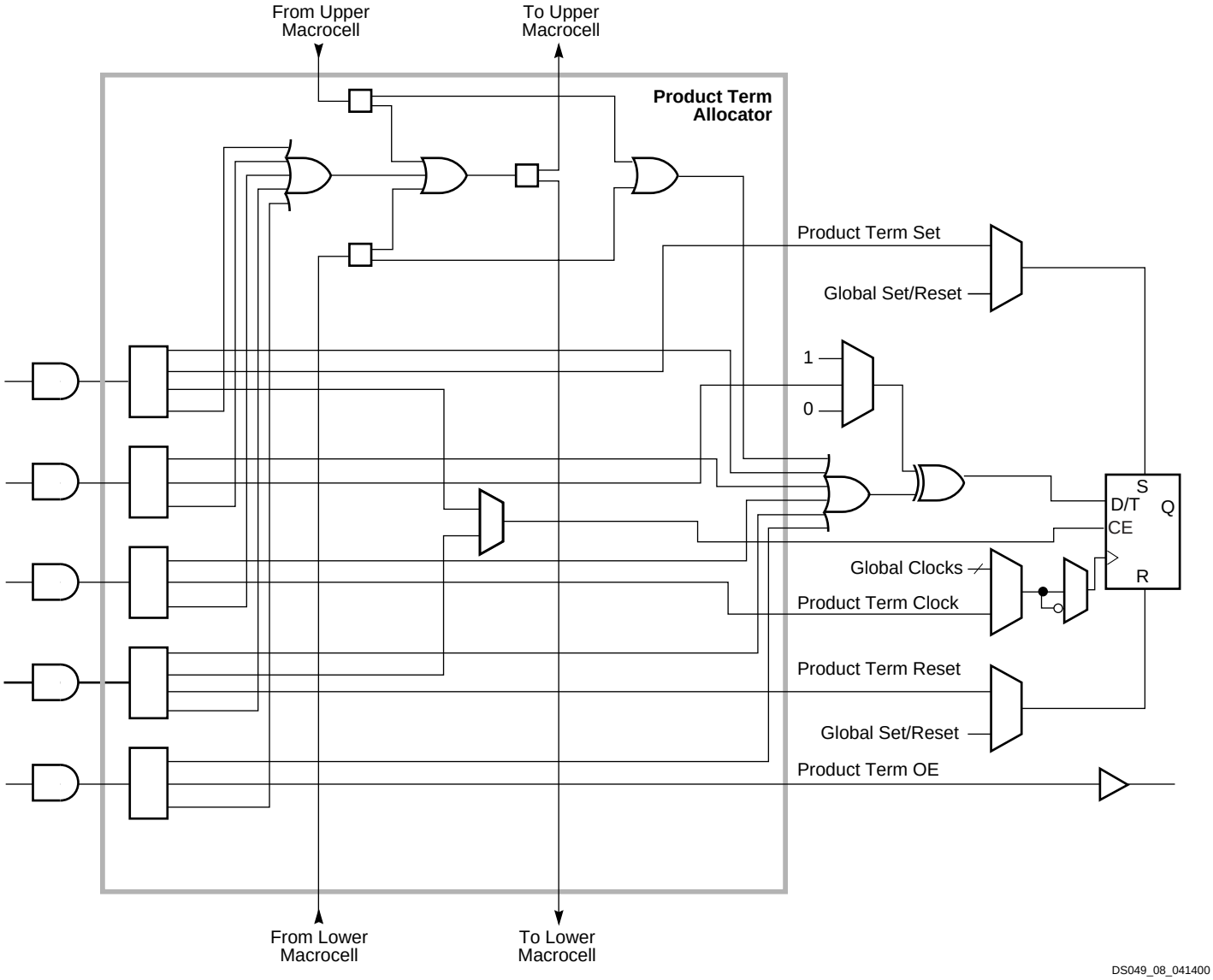

Figure 8: **Product Term Allocator Logic**

FastCONNECT II Switch Matrix

The FastCONNECT II Switch Matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT II matrix. Any of these (up to a fan-in limit of 54) may be selected to drive each FB with a uniform delay.

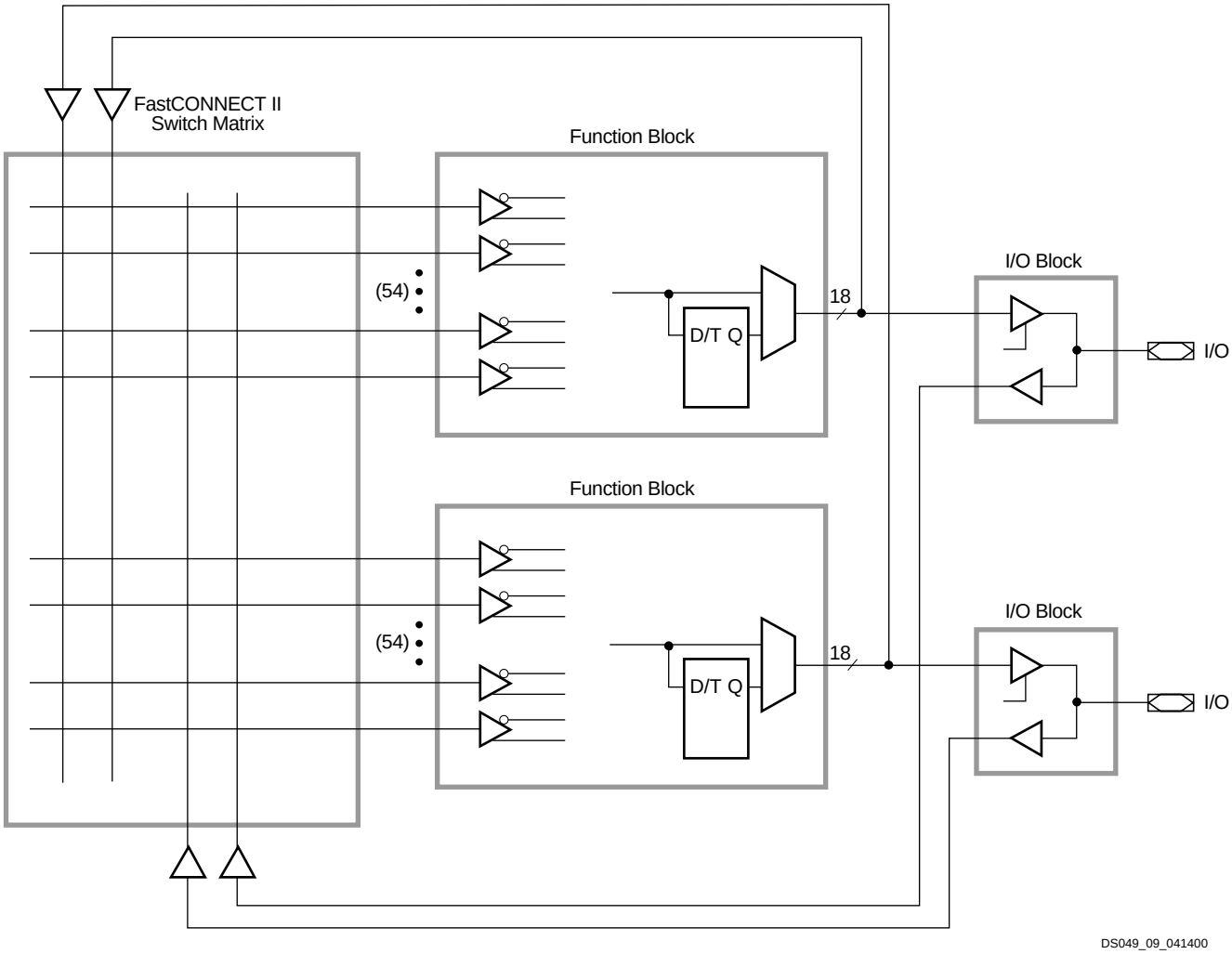

Figure 9: **FastCONNECT II Switch Matrix**

I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

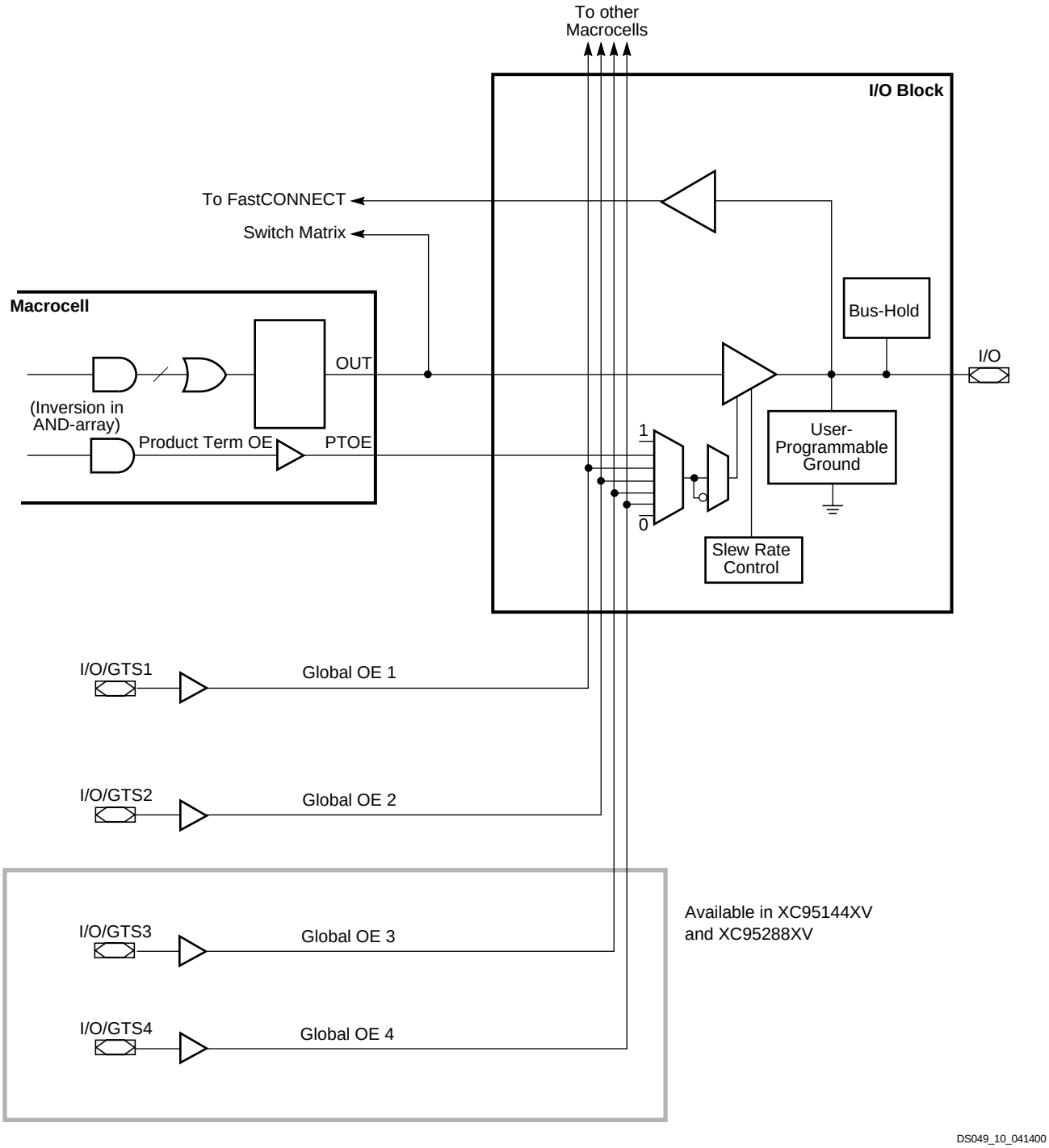

Figure 10: **I/O Block and Output Enable Capability**

The input buffer is compatible with 3.3V CMOS, 2.5V CMOS, and 1.8V CMOS signals. The input buffer uses the internal 2.5V voltage supply (V_{CCINT}) to ensure that the input thresholds are constant and do not vary with the V_{CCIO} voltage. Each input buffer provides input hysteresis (50 mV typical) to help reduce system noise for input signals with slow rise or fall edges.

Each output driver is designed to provide fast switching with minimal power noise. All output drivers in the device may be configured for driving either 3.3V, 2.5V, or 1.8V CMOS levels by connecting the device output voltage supply (V_{CCIO}) to a 3.3V, 2.5V, or 1.8V voltage supply. Figure 11(a) shows how the XC9500XV device can be used in a 2.5V only system.

Each output driver can also be configured for slew-rate limited operation. Output edge rates may be slowed down to reduce system noise (with an additional time delay of T_{SLEW}) under user control. See Figure 12.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global output enable signals (GTS), always “1”, or always “0”. There are two global output enables for devices with 72 or fewer macrocells, and four global output enables for devices with 144 or more macrocells. Any selected output enable signal may be inverted locally at each pin output to provide maximum design flexibility.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins in order to force otherwise unused pins to a low voltage state, as well as provide for additional device grounding capability. This grounding of the pin is achieved by internal logic that forces a logic Low output regardless of the internal macrocell signal, so the internal macrocell logic is unaffected by the programmable ground pin capability.

Each IOB also provides for bus-hold circuitry that is active during valid user operation. The bus-hold feature eliminates the need to tie unused pins either High or Low by holding the last known state of the input until the next input signal is present. The bus-hold circuit drives back the same state via a nominal resistance (R_{BH}) of 50K ohms. See Figure 13.

Note: The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals when interfacing to 2.5V components.

When the device is not in valid user operation, the bus-hold circuit defaults to an equivalent 50K ohm pull-up resistor in order to provide a known repeatable device state. This occurs when the device is in the erased state, in programming mode, in JTAG INTEST mode, or during initial power-up. A pull-down resistor (1K ohm) may be externally added to any pin to override the default R_{BH} resistance to force a Low state during power-up or any of these other modes.

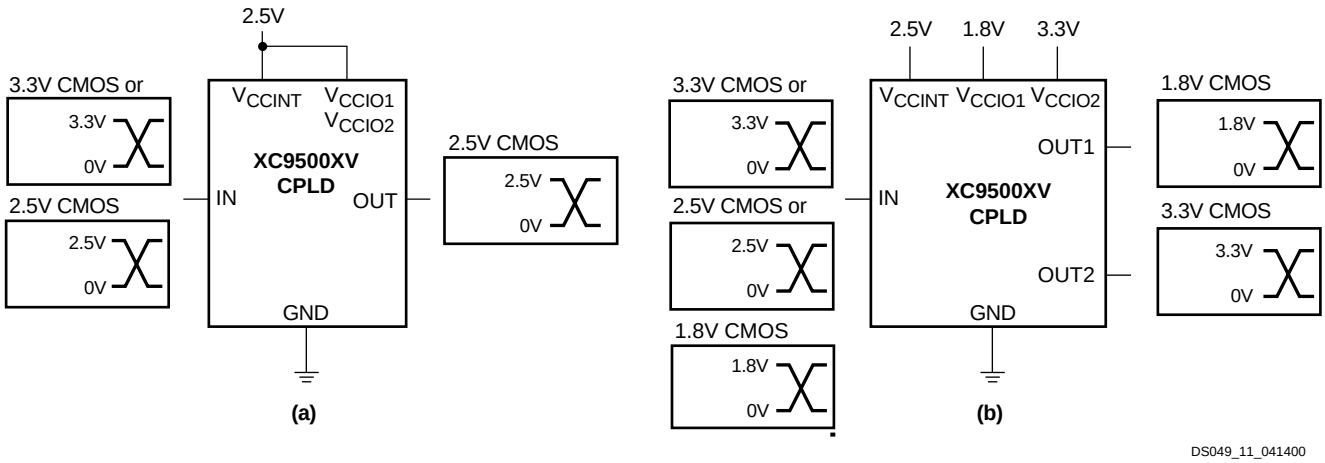

Figure 11: **XC9500XV Devices in (a) 2.5V only and (b) Mixed 3.3V/2.5V/1.8V Systems**

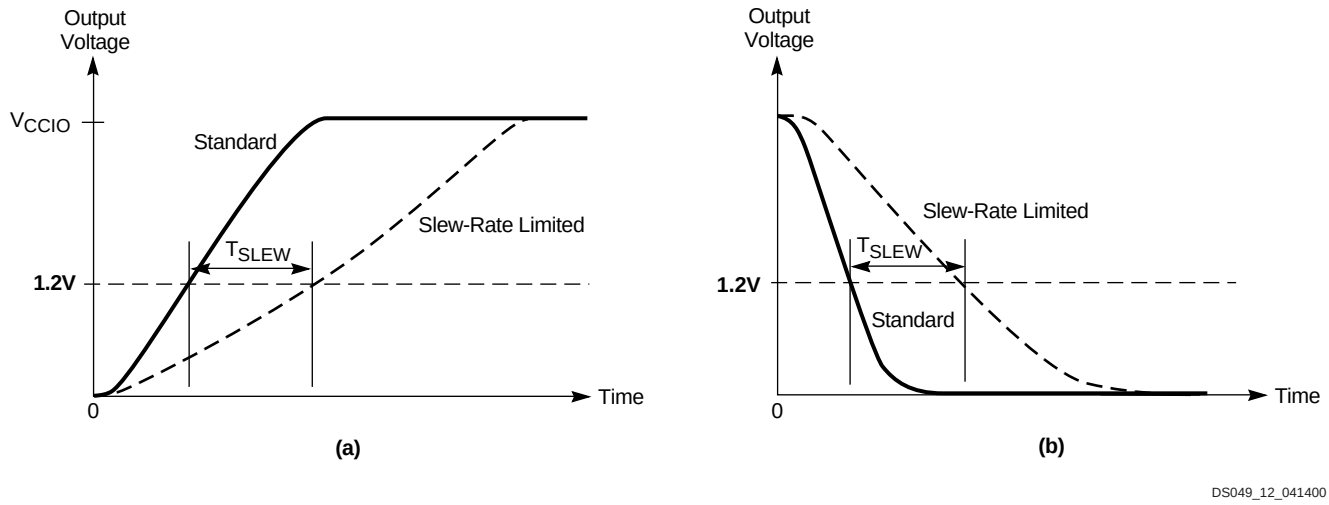

Figure 12: **Output Slew-Rate Control For (a) Rising and (b) Falling Outputs**

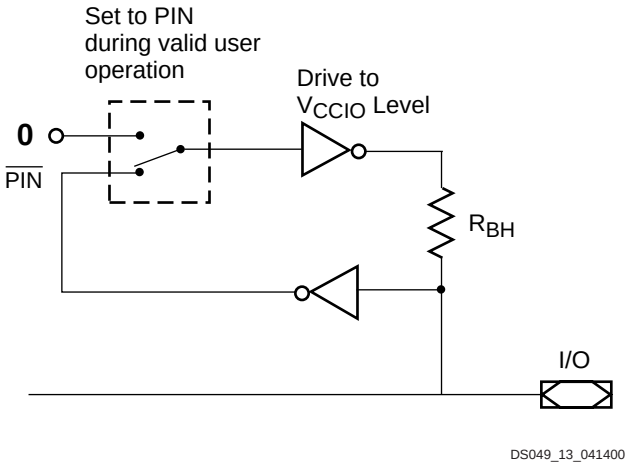

Figure 13: **Bus-Hold Logic**

Output Banking

XC95288XV and XC95144XV devices are designed with a split-rail I/O structure. This permits the utilization of multiple output drive levels for systems able to operate best in that environment. The output partitioning is by function blocks (FB). With this arrangement, designers can have some sets of outputs driving to 2.5V and others set to 1.8V. Naturally, it is possible to tie all rails to a single output voltage and get all outputs driving to that level. Should designs be migrated from one density to another in the same package, care should be taken to remember the voltage assignments chosen at the outset to assure consistency (Figure 14).

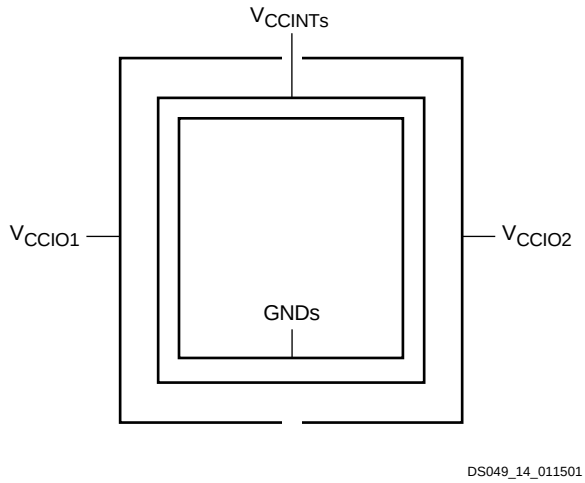

Figure 14: **Split Rail V_{CC} Output Power Connections in XC95144XV and XC95288XV Devices**

Mixed Voltage

The I/Os on each XC9500XV device are fully 3.3V tolerant even though the core power supply is 2.5V. This allows 3.3V CMOS signals to connect directly to the XC9500XV inputs without damage. In addition, the 2.5V V_{CCINT} power supply can be applied before or after 2.5V signals are applied to the I/Os. In mixed 3.3V/2.5V/1.8V systems, the user pins, the core power supply (V_{CCINT}), and the output power supply (V_{CCIO}) may have power applied in any order. This makes the XC9500XV devices immune to power supply sequencing problems (see Figure 11b).

Xilinx proprietary ESD circuitry and high impedance initial state permit hot plugging cards using XC9500XV CPLDs.

Pin-Locking Capability

The capability to lock the user defined pin assignments during design iteration depends on the ability of the architecture to adapt to unexpected changes. The XC9500XV devices incorporate architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500XV architecture provides for superior pin-locking characteristics with a combination of large number of routing switches in the FastCONNECT II switch matrix, a 54-wide input Function Block, and flexible, bi-directional product term allocation within each macrocell. These features address design changes that require adding or changing internal routing, including additional signals into existing equations, or increasing equation complexity, respectively.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments. The same board may be used with a higher density device without the expense of board rework.

In-System Programming

One or more XC9500XV devices can be daisy chained together and programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 15. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a Xilinx download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All I/Os are set to a high-impedance state and pulled High by the bus-hold circuitry during in-system programming. If a particular signal must remain Low during this time, then a pull-down resistor may be added to the pin.

Reliability and Endurance

All XC9500XV CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

IEEE 1149.1 Boundary-Scan (JTAG)

XC9500XV devices fully support IEEE 1149.1 boundary-scan (JTAG). EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, HIGHZ and CLAMP instructions are supported in each device. Additional instructions are included for in-system programming operations.

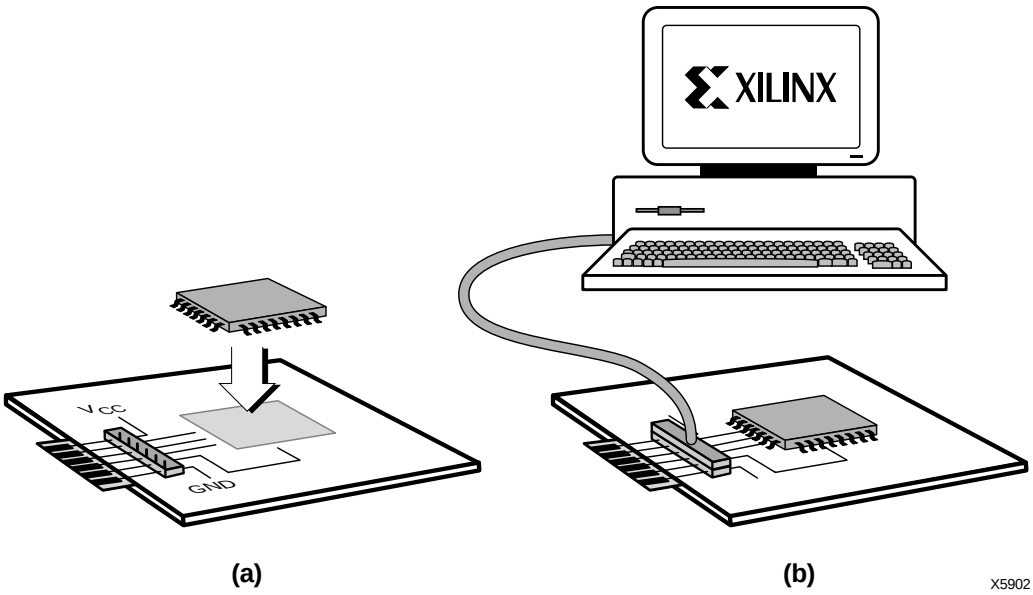

Figure 15: **In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

Design Security

XC9500XV devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. When set, they also inhibit further program operations but allow device erase. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern with a specific sequence of JTAG instructions

Table 3: **Data Security Options**

		Read Security	
		Default	Set
Write Security	Default	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Inhibited
	Set	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Inhibited

Low Power Mode

All XC9500XV devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay (T_{LP}) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

Timing Model

The uniformity of the XC9500XV architecture allows a simplified timing model for the entire device. The basic timing model, shown in Figure 16, is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is "0". The example in Figure 6 shows that up to 15 product terms are available with a span of "1". In the case of Figure 7, the 18 product term function has a span of "2".

Detailed timing information may be derived from the full timing model shown in Figure 17. The values and explanations for each parameter are given in the individual device data sheets.

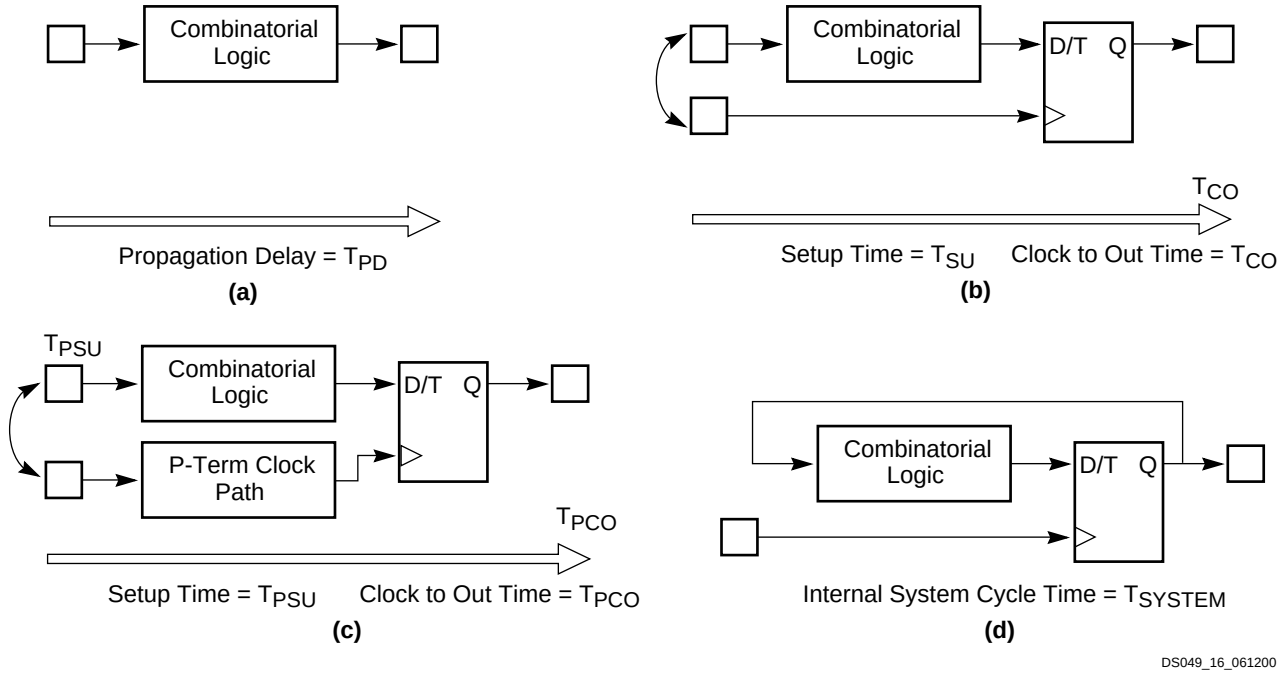

Figure 16: **Basic Timing Model**

Table 4: **Timing Model Parameters**

Description	Parameter	Product Term Allocator(1)	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	T_{PD}	+ T_{PTA} * S	+ T_{LP}	+ T_{SLEW}
Global Clock Setup Time	T_{SU}	+ T_{PTA} * S	+ T_{LP}	-
Global Clock-to-output	T_{CO}	-	-	+ T_{SLEW}
Product Term Clock Setup Time	T_{PSU}	+ T_{PTA} * S	+ T_{LP}	-
Product Term Clock-to-Output	T_{PCO}	-	-	+ T_{SLEW}
Internal System Cycle Period	T_{SYSTEM}	+ T_{PTA} * S	+ T_{LP}	-

Notes:
1. S = the logic span of the function, as defined in the text.

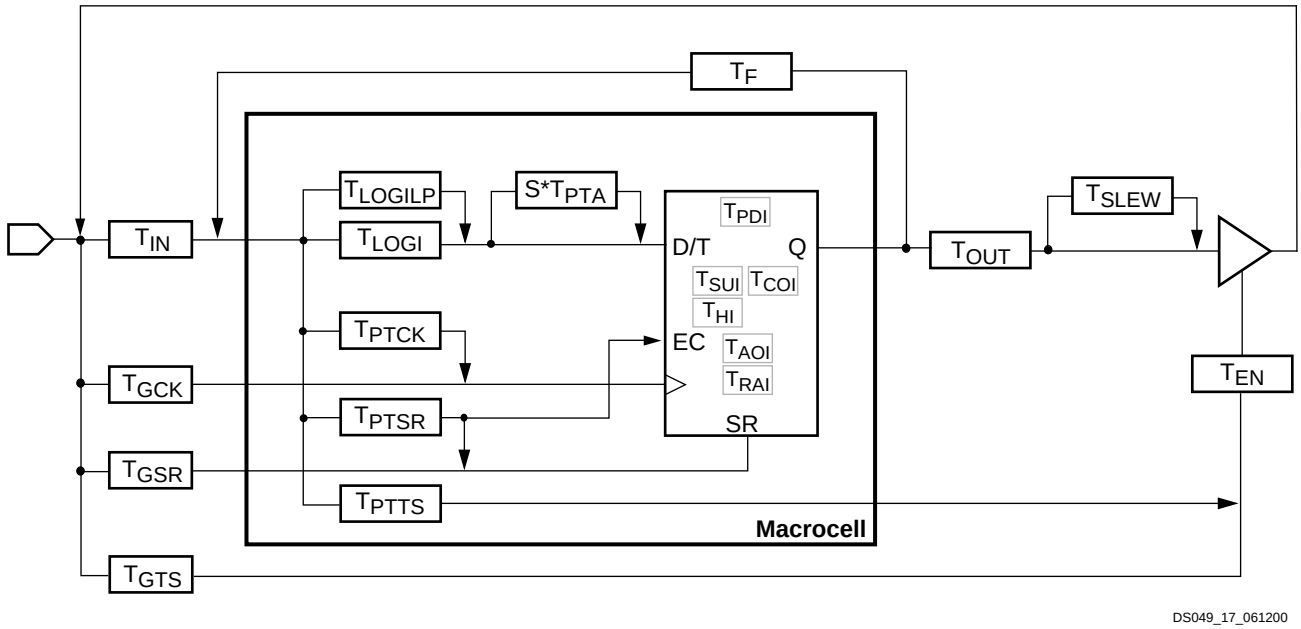

Figure 17: **Detailed Timing Model**

Power-Up Characteristics

The XC9500XV devices are well behaved under all operating conditions. During power-up each XC9500XV device employs internal circuitry which keeps the device in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 1.9V). During this time, all device pins and JTAG pins are disabled and all device outputs are disabled with the pins weakly pulled High, as shown in Table 5. When the supply voltage reaches a safe level, all user registers become initialized (typically within 300 µs), and the device is immediately available for operation, as shown in Figure 18.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

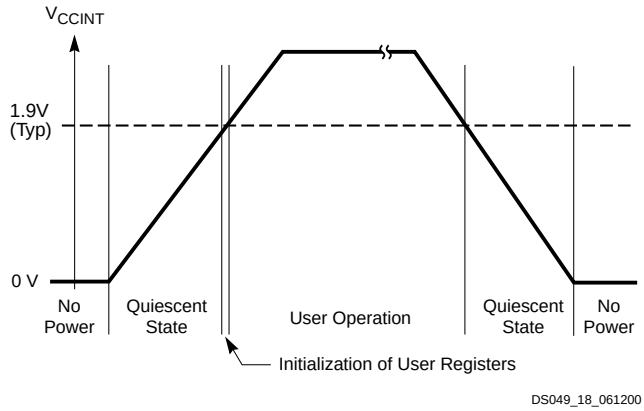

Figure 18: **Device Behavior During Power-up**

Table 5: **XC9500XV Device Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold	Pull-up	Pull-up	Bus-Hold
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

Power-Up Guidelines

Figure 19 shows a block diagram of the internal configuration controller, which transfers the EPROM bits to the latches. Some important things to note are:

- The V_{CCINT} is sensed to determine when to begin the loading.
- An internal clock source drives a state machine that controls the overall process.
- The bit loading process takes about 100 microseconds.
- Internal configuration latches are automatically reset at the beginning of the process.
- The state machines, counters and strobes are built from CMOS transistors, so they need voltage, setup time, hold time, and propagation delay time to work properly.

When V_{CCINT} passes a threshold, it automatically enables. The state machine cycles through addresses, delivers load strobes to internal latches and completes the process by enabling the I/O pins.

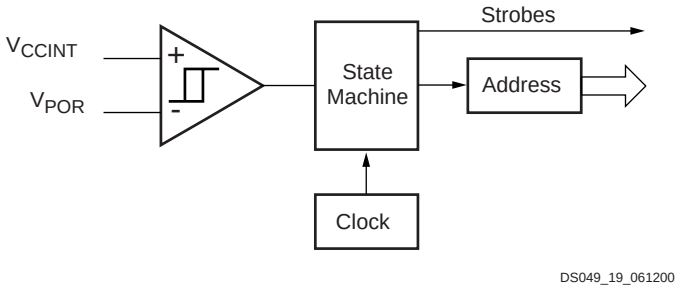

Figure 19: **Configuration Controller**

Figure 20 describes what happens inside the chip as the supply rises to its final value. At low voltage, the transistors do not behave like transistors. As V_{CC} passes about a volt, the transistors begin to wake up, but are not yet fully functional. Above 1V, they can amplify and form basic gates. Near 1.8V, they work correctly and can make reliable latches. Above 2V, they can be reliably loaded with EPROM bits. It is in this voltage neighborhood the POR circuits begin transferring EPROM bits to the latches. XC9500XV POR begins about 1.8V.

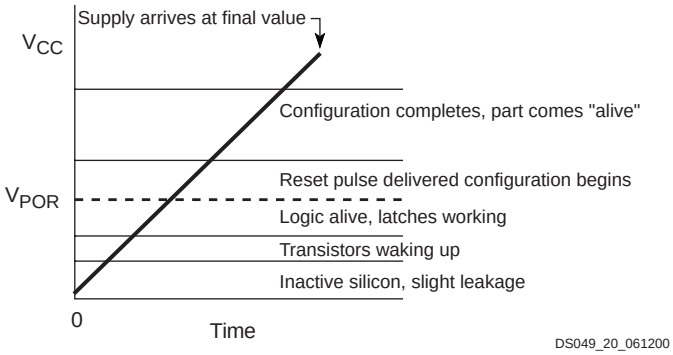

Figure 20: **Power-up Activity**

Development System Support

The XC9500XV family and associated in-system programming capabilities are fully supported in either software solutions available from Xilinx.

The Foundation Series is an all-in-one development system containing schematic entry, HDL (VHDL, Verilog, and ABEL), and simulation capabilities. It supports the XC9500XV family as well as other CPLD and FPGA families.

The Alliance Series includes CPLD and FPGA implementation technology as well as all necessary libraries and interfaces for Alliance partner EDA solutions.

The Xilinx WebPOWERED Software Solution offer designers the flexibility to target the XC9500 and CoolRunner® Series CPLDs on-line with WebFITTER or on the desktop with WebPACK. WebFITTER is an on-line device fitting and evaluation tool which accepts HDL, ABEL, or netlist files and provides all reports, simulation models, and programming files. WebPACK downloadable desktop solutions offer FREE CPLD software modules for ABEL and HDL synthesis, device fitting and JTAG programming.

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
01/19/99	1.0	Initial Xilinx release. Advance Information Specification.
06/12/00	1.1	Updated 3.3V information, added Output Banking, added DS049 number. Added WebPACK information and minor edits. Added "Power-Up Guidelines" on page 17.
01/15/01	2.0	New performance and package options, removed references to "Fast Flash".