

## INTRODUCTION

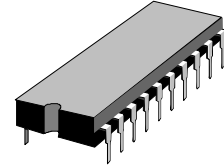
The S5T8555 is a per channel Time Slot Assignment Circuit (TSAC) that produces 8-bit receive and transmit time slots for four 1 CHIP CODEC.

Each frame synchronization pulse may be independently assigned to a time slot in a frame of up to 64 time slots

## FEATURES

- Single, 5V operation
- Low power consumption: 5mW
- Controls four 1 CHIP CODEC
- Independent transmit and receive frame syncs
- channel unidirectional mode
- Up to 64 time slots per frame
- Compatible with S5T8554B/7B CODECs
- TTL and CMOS compatible

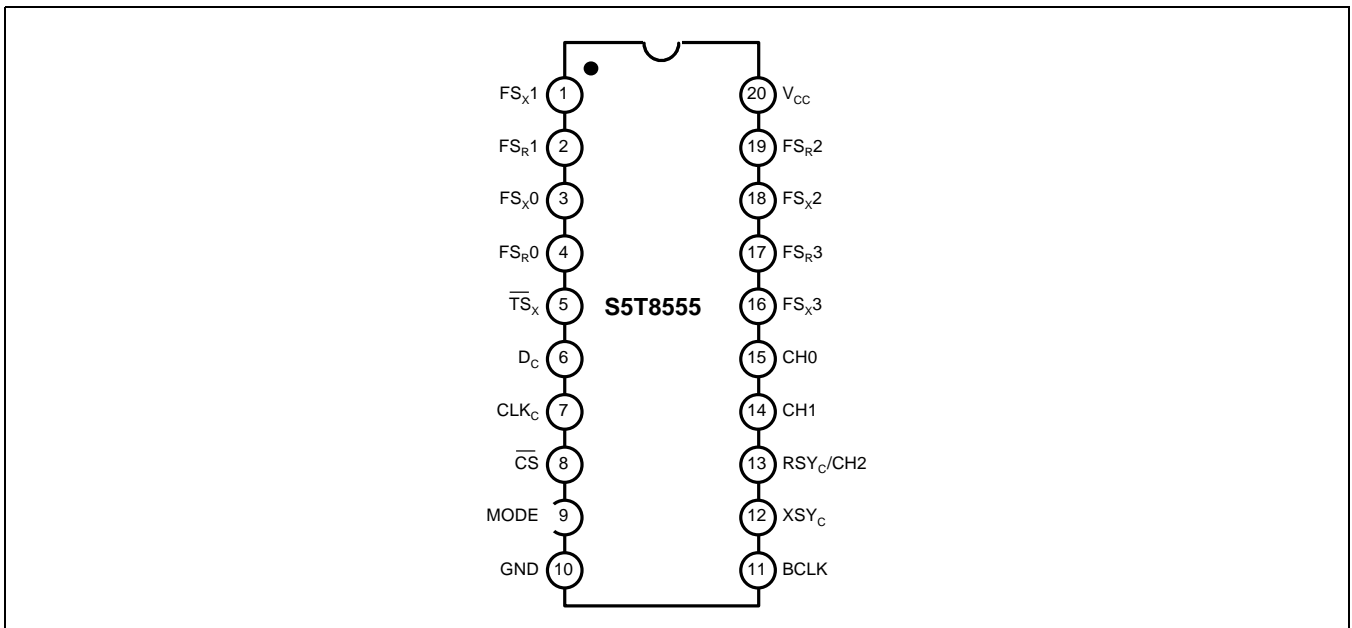
20-CERDIP



## ORDERING INFORMATION

Device	Package	Operating Temperature
S5T8555X01-L0B0	20-CERDIP	-20°C to 125°C

PIN CONFIGURATION



## PIN DISCRIPTION

Pin No	Symbol	Description
3 1 18 16	FS <sub>X</sub> 0 FS <sub>X</sub> 1 FS <sub>X</sub> 2 FS <sub>X</sub> 3	A Transmit frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
4 2 19 17	FS <sub>R</sub> 0 FS <sub>R</sub> 1 FS <sub>R</sub> 2 FS <sub>R</sub> 3	A Receive frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
5	TS <sub>X</sub>	This pin pulls low during any active transmit time slot. (N-channel open drain)
6	D <sub>C</sub>	The input for an 8 bit serial control word. X is the first bit clocked in.
7	CLK <sub>C</sub>	The clock input for the control interface.
8	CS	The active-low chip select for the control interface.
9	MODE	Mode 1 = Open or V <sub>CC</sub> Mode 2 = Gnd
10	GND	Ground
11	BCLK	The bit clock input (2.048 MHz)
12	XSY <sub>C</sub>	The transmit Time Slot Output sync pulse input. Must be synchronous with BCLK.
13	RSY <sub>C</sub> /CH2	The receive time slot sync pulse input. Must be synchronous with BCLK. In mode 1 this input is the receive time slot 0 sync pulse, RSY <sub>C</sub> , which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
14	CH1	The input for the NSB (next significant bit) of the channel select word.
15	CH0	The input for the LSB (last significant bit) of the channel select word, which defines the frame sync output affected by the following control word.
20	V <sub>CC</sub>	Power supply pin. 5V ± 5%

**ABSOLUTE MAXIMUM RATING (Ta = 25°C)**

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	$V_{CC}$	70.	V
Input Voltage	$V_I$	$V_{CC} + 0.3 \sim -0.3$	V
Output Voltage	$V_O$	$V_{CC} + 0.3 \sim -0.3$	V
Operating Temperature Range	$T_{OPR}$	- 25 ~ 125	°C
Storage Temperature Range	$T_{STG}$	- 65 ~ 150	°C
Lead Temperature (Soldering, 10 secs)	$T_{LEAD}$	300	°C

## ELECTRICAL CHARACTERISTICS

(Unless otherwise noted;  $V_{CC} = 5.0V \pm 5\%$ ,  $T_a = 0^\circ C$  to  $70^\circ C$ )

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Current	$I_{CC}$	BCLK = 2.048MHz, all output open	–	1	1.5	mA
Input Voltage High	$V_{IH}$	–	2.0	–	–	V
Input Voltage Low	$V_{IL}$	–	–	–	0.7	V
Input Current 1	$I_{I1}$	All Inputs Except Mode, $V_{IL} \leq V_{IN} \leq V_{IH}$	–1	–	1	$\mu A$
Input Current 2	$I_{I2}$	Mode, $V_{IN} = 0V$	–100	–	–	$\mu A$
Output Voltage High	$V_{OH}$	$FS_X$ and $FS_R$ Outputs, $I_{OH} = 3mA$	2.4	–	–	V
Output Voltage Low		$FS_X$ and $FS_R$ Outputs, $I_{OH} = 3mA$	–	–	0.4	V
		$TS_X$ output, $I_{OL} = 3mA$	–	–	0.4	V
Rise and Fall Time of Clock	$t_R (CK)$ $t_F (CK)$	BCLK, $CLK_C$	–	–	50	nS
Delay to $TS_X$ Low	$t_D (TSXL)$	$C_L = 50pF$	–	–	140	nS
Delay to $TS_X$ High	$t_D (TSXH)$	$R_L = 1k\Omega$	30	–	100	nS
Hold Time BCLK to Frame Sync	$t_H (BFS)$	–	50	–	–	nS
Set-Up Time from Frame Sync BCLK	$t_H (FSB)$	–	30	–	–	nS
Delay Time from BCLK Low to $FS_{X/R}0-3$ High or Low	$t_D$	$C_L = 50pF$	–	–	50	nS
Hold Time from Channel Select to CLK	$t_H (CSC)$	–	50	–	–	nS
Set-Up Time from Channel Select to CLK	$t_{SU} (CSC)$	–	30	–	–	nS
Period of Clock	$t_{CK}$	BCLK, $CLK_C$	240	–	–	nS
Width of Clock High	$t_W (CKH)$	BCLK, CLK	50	–	–	nS
Width of Clock Low	$t_W (CKL)$	BCLK, CLK	50	–	–	nS
Set-Up Time from $D_C$ to CLK	$t_{SU} (DCC)$	–	30	–	–	nS
Hold Time from CLK to $D_C$	$t_H (CDC)$	–	50	–	–	nS
Set-Up Time from CS to CLK	$t_{SU} (CC)$	–	30	–	–	nS
Hold Time from CLK to CS	$t_H (CC)$	–	100	–	–	nS

TIMING DIAGRAM

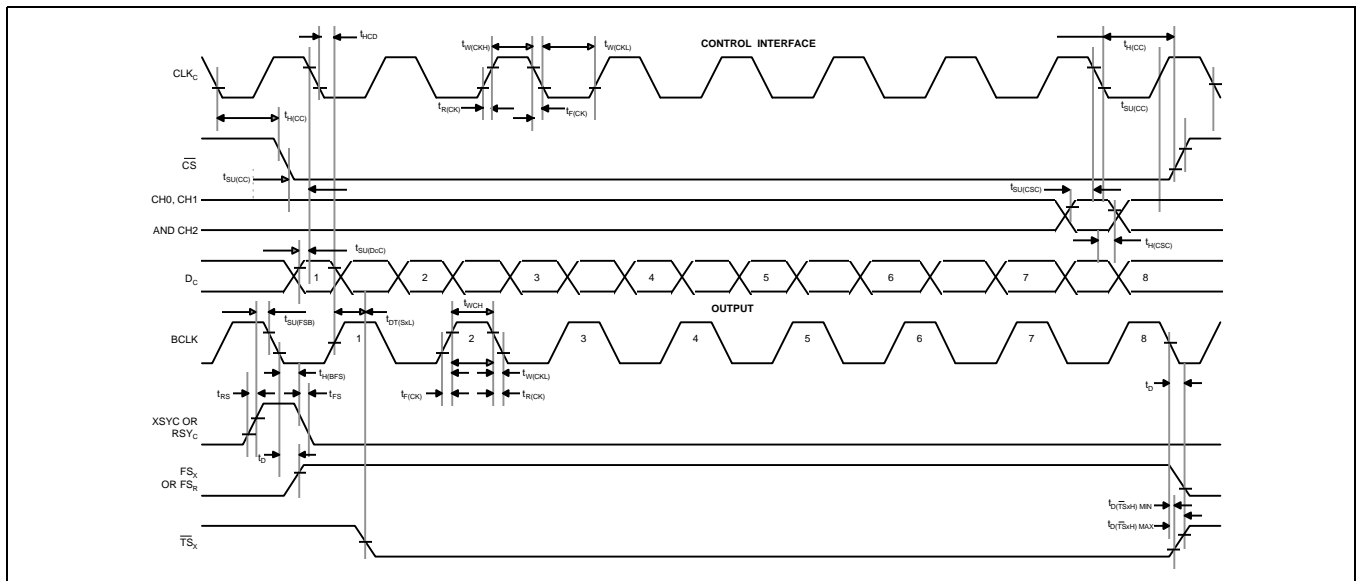


Figure 1.

APPLICATION INFORMATION

OPERATING CONTROL MODE 1

The S5T8555 is a control interface which requires an 8 bit serial control word. Either one of the frame sync output group, FS<sub>X</sub>0 to FS<sub>X</sub>3 or FS<sub>R</sub>0 to FS<sub>R</sub>3, affected by the control word is defined by the two bits, X and R. Time slot selected from 0 to 63 is specified. A frame sync output is highly active for one time slot which is equivalent to 8 cycles of BCLK. Up to 64 time slots are allowed to form a frame. There are two operational mode. In mode 1, each channel of transmit and receive direction has different time slot assigned. This mode can be selected by either leaving pin 9 (MODE) opened or connecting it with V<sub>CC</sub>. In such a case, pin 13 is RSYC input defining the start of each receive frame while four out-put, FS<sub>R</sub>0 to FS<sub>R</sub>3, are assigned with respect to RSYC. On the other hand, start of each transmit frame is defined by XSYC input by which output FS<sub>X</sub>0 to FS<sub>X</sub>3, are assigned. XSYC and RSYC can be phase related. Channels from 0-3 are selected by the input CH0 and CH1 (refer to the table 1).

X	R	T5	T4	T3	T2	T1	T0
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X is the first bit clocked into D<sub>C</sub> input

CH1	CH0	Channel Selected
0	0	Assign to FS <sub>X</sub> 0 and/or FS <sub>R</sub> 0
0	1	Assign to FS <sub>X</sub> 1 and/or FS <sub>R</sub> 1
1	0	Assign to FS <sub>X</sub> 2 and/or FS <sub>R</sub> 2
1	1	Assign to FS <sub>X</sub> 3 and/or FS <sub>R</sub> 3

Control Data Format

Table 1. OPERATING CONTROL MODE 1

T5	T4	T3	T2	T1	T1	Time Slot	X	R	Action
0	0	0	0	0	0	0	0	0	Assign time slot to both selected FS <sub>X</sub> and FS <sub>R</sub>
0	0	0	0	0	1	1	0	1	Assign time slot to selected FS <sub>X</sub> only
0	0	0	0	1	0	2	1	0	Assign time slot to selected FS <sub>R</sub> only
							1	1	Assign time slot to selected FS <sub>X</sub> and FS <sub>R</sub>
									.
									.
									.
0	1	1	1	1	0	30			
0	1	1	1	1	1	31			
1	0	0	0	0	0	32			
1	0	0	0	0	1	33			
									.
									.
									.
1	1	1	1	1	1	63			

OPERATING CONTROL MODE 2

In mode 2, all 8 frame sync outputs can be assigned with respect to XSYNC input. The mode 2, selected by connecting pin 9 (MODE) to GND, enables the S5T8555 TSAC suitable for an 8-channel unidirectional controller and for a system where both transmit and receive direction of each channel have same time slot assigned. For instance, FS<sub>X</sub> and FSR input of 1 CHIP CODEC are hard wired together. The channel assigned has its channel selected by CH0, CH1 and CH2 (refer to table 2).

CH2	CH1	CH0	Channel Selected	X	R	Action
0	0	0	Assign to FS <sub>X0</sub>	0	0	Assign time slot to selected output
0	0	1	Assign to FS <sub>X1</sub>	0	1	Assign time slot to selected output
0	1	0	Assign to FS <sub>X2</sub>	1	0	Assign time slot to selected output
0	1	1	Assign to FS <sub>X3</sub>	1	1	Disable both selected output
1	0	0	Assign to FS <sub>R0</sub>			
1	0	1	Assign to FS <sub>R1</sub>			
1	1	0	Assign to FS <sub>R2</sub>			
1	1	1	Assign to FS <sub>R3</sub>			

**APPLICATION CIRCUIT**

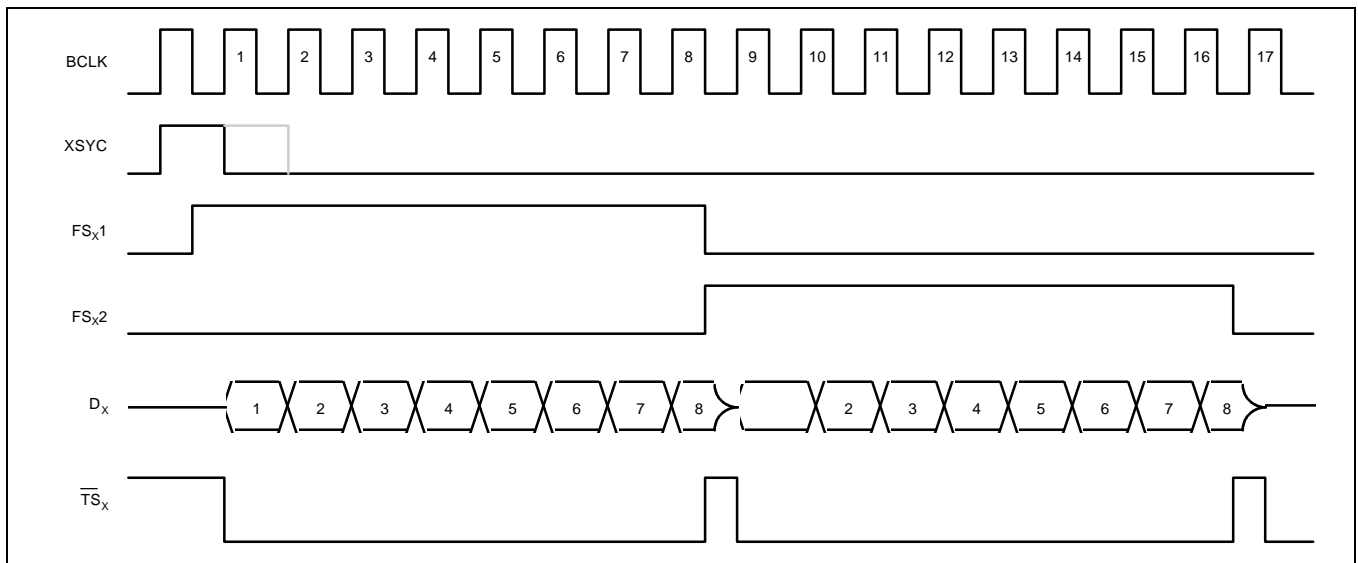
The S5T8555 TSAC combined with any kind of 1 CHIP CODEC from S5T8554B/7B series can obtain data timing as illustrated in Fig. 3. Even though  $FS_x$  output goes high before BCLK gets high, the  $D_x$  output of the 1 CHIP CODEC remains in the TRI-STATE mode until both outputs are high.

The eight bit period is shortened to avoid PCM data clash at PCM pre-highway.

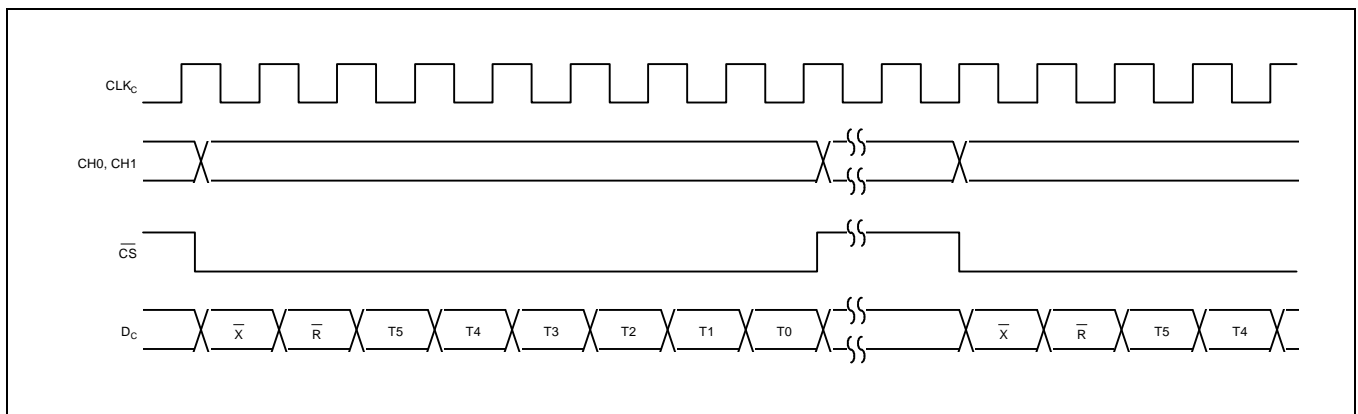
Alternatively, full 8 bits can be obtained by inverting the BCLK to the 1 CHIP CODEC devices, thereby rising edges of BCLK and  $FS_{x/R}$  are aligned.

Fig. 4 is typical timing of the control data interface.

Fig. 5 is the typical application circuit at operating control mode 2.



**Figure 2. Transmit Data Timing**



**Figure 3. Control Data Timing**



APPLICATION CIRCUIT

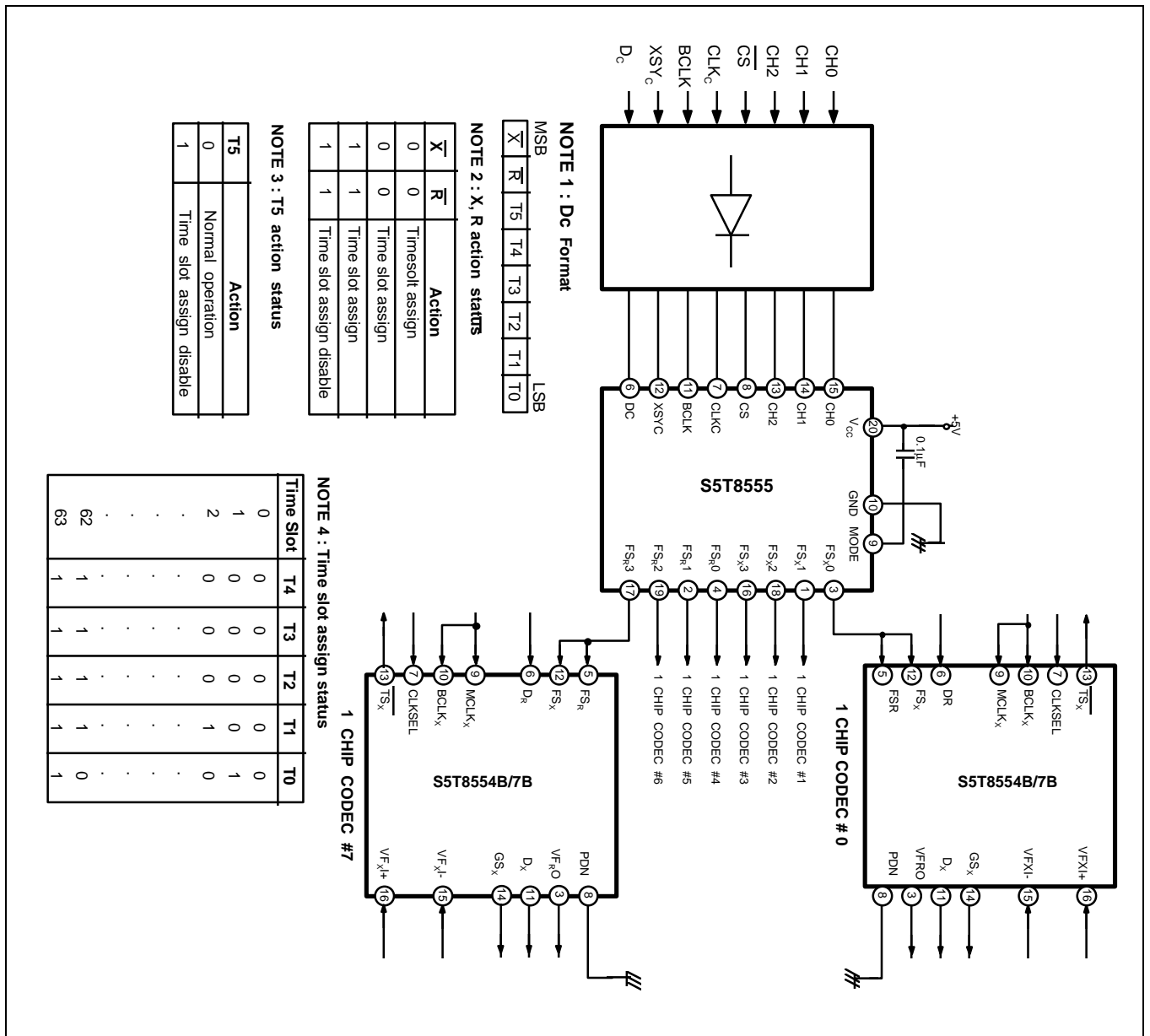


Figure 4. Digital Interface on a Typical Subscriber Linecard

NOTES: Different time slot assign for RX and TX respectively

NOTES