FAIRCHILD SEMICONDUCTOR®

June 2004

RMWB33001

33 GHz Buffer Amplifier MMIC

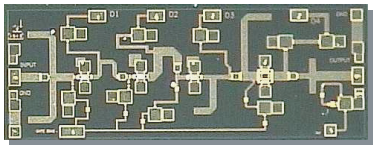
General Description

The RMWB33001 is a 4-stage GaAs MMIC amplifier designed as a 33 GHz Buffer Amplifier for use in point to point and point to multi-point radios, and various communications applications. In conjunction with other Fairchild RF amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWB33001 utilizes our 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of medium power amplifier applications.

Features

- 4 mil Substrate
- Small-signal Gain 24dB (typ.)
- Saturated Power Out 19dBm (typ.)
- Voltage Detector Included to Monitor Pout
- Chip size 3.2mm x 1.2mm

Device



Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Positive DC Voltage (+4V Typical)	+6	V
Vg	Negative DC Voltage	-2	V
Vdg	Simultaneous (Vd–Vg)	8	V
I_D	Positive DC Current	173	mA
P_{IN}	RF Input Power (from 50Ω source)	+8	dBm
T_C	Operating Baseplate Temperature	-30 to +85	°C
T_{STG}	Storage Temperature Range	-55 to +125	°C
R_{JC}	Thermal Resistance (Channel to Backside)	130	°C/W

Electrical Characteristics (At 25°C), 50Ω system, Vd = +4V, Quiescent Current Idq = 112mA

Parameter	Min	Typ	Max	Units
Frequency Range	32		35	GHz
Gate Supply Voltage[1] (Vg)		-0.2		V
Gain Small Signal (Pin = -15dBm)	20	24		dB
Gain Variation vs. Frequency		2.0		dB
Power Output Saturated: (Pin = +1dBm)	17	19		dBm
Drain Current at Psat		120		mA
Power Added Efficiency (PAE): at Psat		15		%
Input Return Loss (Pin = -15dBm)		12		dB
Output Return Loss (Pin = -15dBm)		12		dB
DC Detector Voltage at Pout = 18dBm		1.0		V

Note:
1: Typical range of gate voltage is -0.5 to 0V to set Idq of 112mA.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.

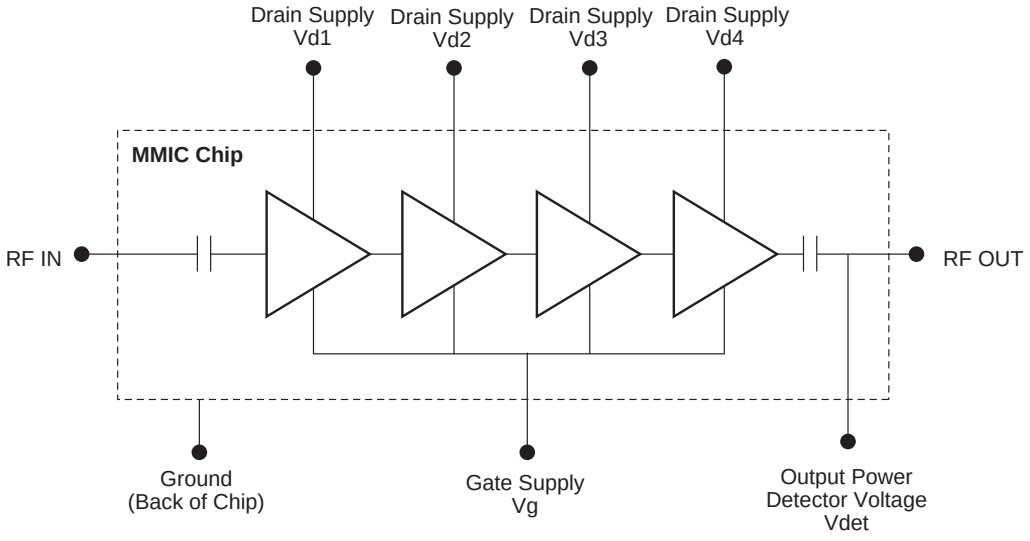
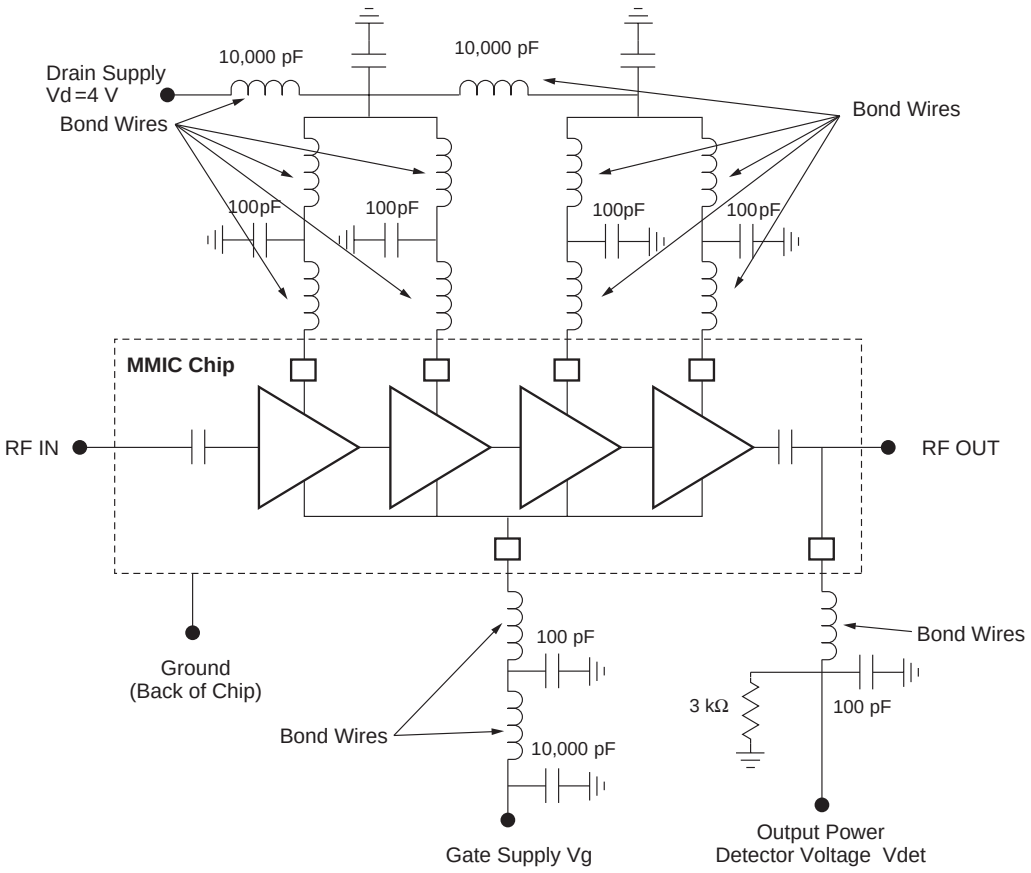


Figure 1. Functional Block Diagram[1]

Note:
1: Detector delivers >0.1V DC into 3kΩ load resistor for > +18dBm output power. If output power level detection is not desired, do not connect to detector bond pad.

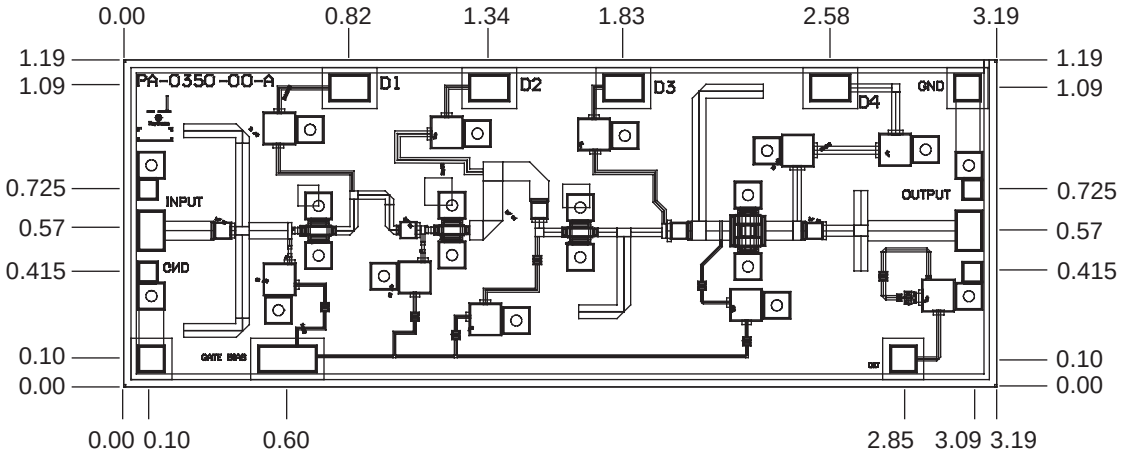
Figure 2. Schematic of Application Circuit



Note:
1: Detector delivers >0.1V DC into 3kΩ load resistor for > +18dBm output power. If output power level detection is not desired, do not connect to detector bond pad.

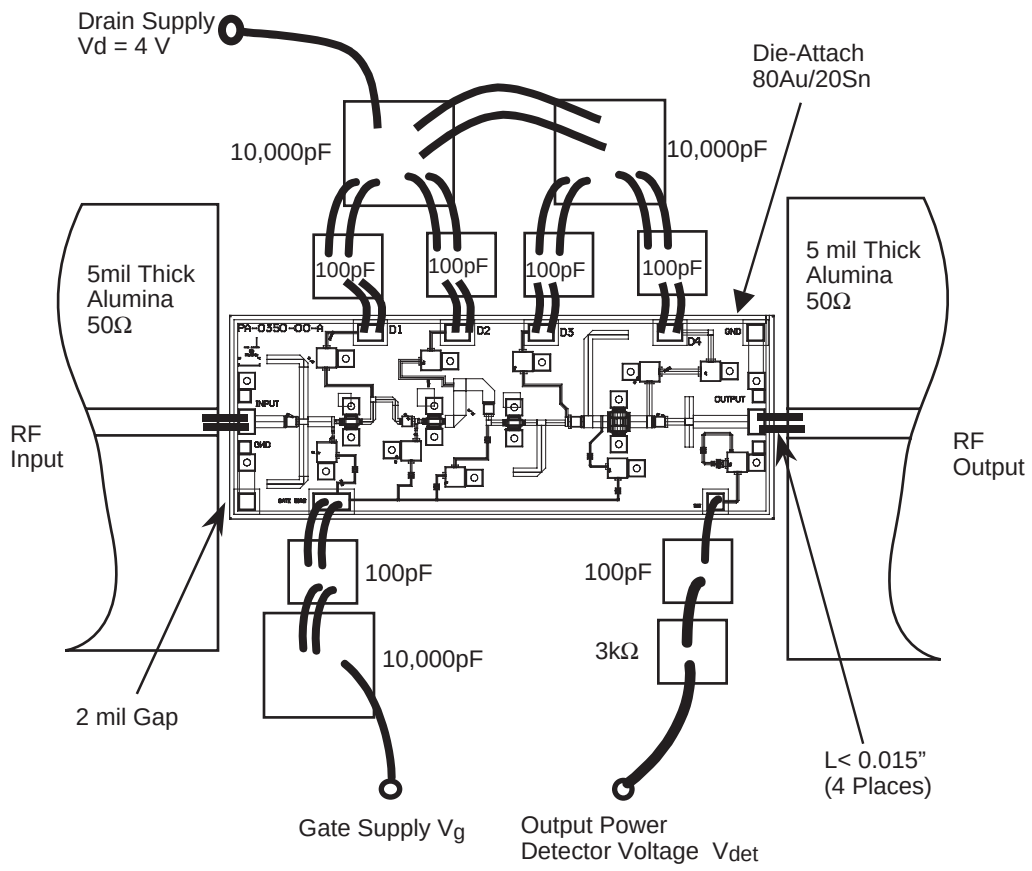
Figure 3. Chip Layout and Bond Pad Locations

Dimensions in mm



Chip Size is 3.19mm x 1.19mm X 100µm. Back of chip is RF and DC Ground.

Figure 4. Recommended Assembly Diagram



Note:
Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

Test Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +4V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 112mA.

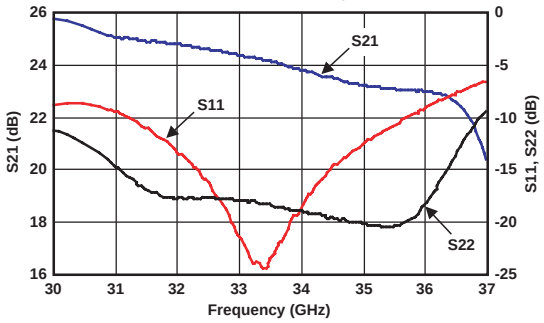
Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

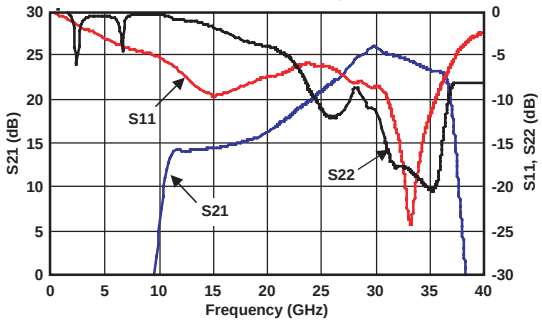
(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

Performance Data

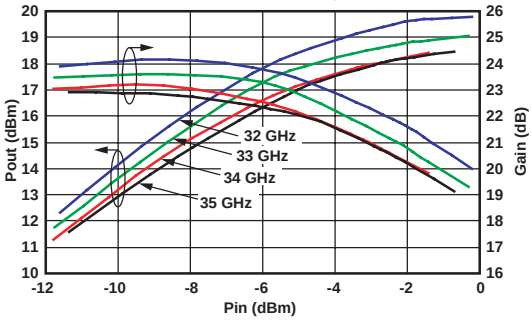
RMWB33001 33 GHz BA, Typical Small Signal Performance
50Ω Fixture Measurements, Vd=4 V, Idq = 112 mA, T=25°C



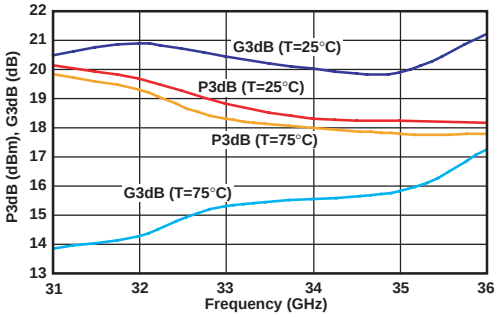
RMWB33001 33 GHz BA, Typical Small Signal Performance
50Ω Fixture Measurements, Vd=4 V, Idq = 112 mA, T=25°C



RMWB33001 33 GHz BA, Power Output and Gain vs. Power In
50Ω Fixture Measurements, Vd=4 V, Idq = 112 mA, T=25°C



RMWB33001 33 GHz BA, Power Output and Gain at 3 dB
Compression vs. Frequency and Temperature,
50Ω FixtureMeasurements, Vd=4 V, Idq = 112 mA



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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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