RF2642

3V 900MHz UPCONVERTER/
DRIVER AMPLIFIER WITH BYPASS MODE

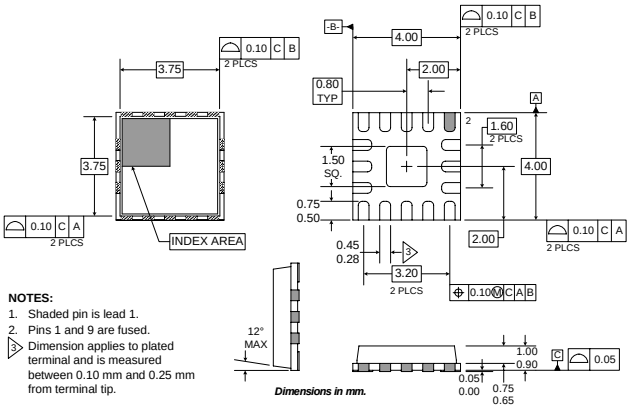
RoHS Compliant & Pb-Free Product

Typical Applications

- CDMA/AMPS Cellular Systems
- TDMA/AMPS Cellular Systems
- General Purpose Upconverter/Driver
- Portable Battery-Powered Equipment

Product Description

The RF2642 is a complete upconverter and power amplifier driver designed for CDMA applications. The design features driver amplifier high and low gain states. In the low gain state, the gain is adjustable and the device draws less current. The upconverter is always on. The power down mode turns off the driver amplifier. The device features balanced IF inputs, single-ended LO input and RF output for ease of interface. Packaged in an industry standard 4mmx4mm, 16-pin, leadless chip carrier, the device provides a low-cost solution while easing board space limitations.

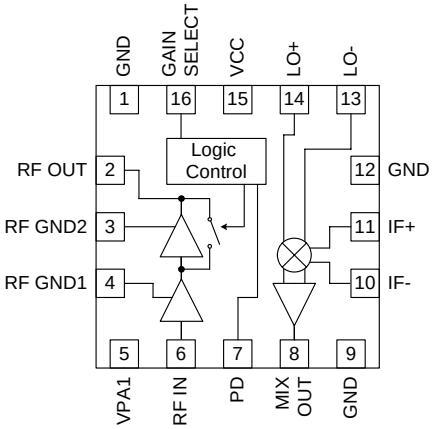


NOTES:
1. Shaded pin is lead 1.
2. Pins 1 and 9 are fused.
3. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ InGaP/HBT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☐ Si CMOS
- ☐ SiGe Bi-CMOS

Package Style: QFN, 16-Pin, 4x4



Functional Block Diagram

Features

- Single Supply 3.0V Operation
- Step Gain Control
- Power Down Control
- ACPR1=61dBc@885kHz with P_{OUT}=+5dBm
- Small QFN 16-Pin Package

Ordering Information

RF2642	3V 900MHz Upconverter/ Driver Amplifier with Bypass Mode
RF2642PCBA41X	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +4.5	V_{DC}
Input RF Power	+3	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

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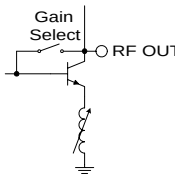
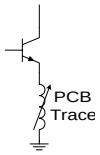
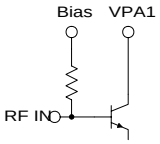
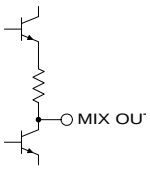
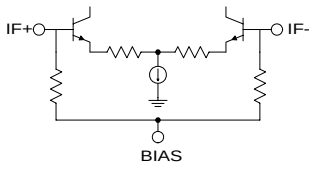
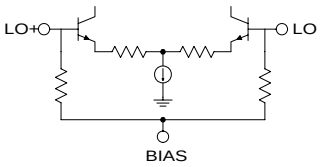
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF_{OUT}=830MHz, LO=960MHz@-3dBm, IF=130MHz
RF Output Frequency Range		824 to 849		MHz	
IF Frequency Range		130		MHz	
Output Power	+5			dBm	CW
High Gain Mode					GAIN SELECT=2.7V, V_{PD}=2.7V
Gain	33	34.5	36	dB	
Noise Figure		12	14	dB	
IF Input Impedance		250		Ω	Differential @ 130MHz
RF Output VSWR		1.5	2:1		824MHz to 849MHz, external components required
Current Consumption		52		mA	
Adjacent Channel Power Rejection (ACPR1)	55	61		dBc	P_{OUT}=+5dBm, 885kHz offset
Alternate Channel Power Rejection (ACPR2)	65	78	80	dBc	P_{OUT}=+5dBm, 1.98MHz offset
Bypass Mode					GAIN SELECT=0V, V_{PD}=2.7V
Gain		11.9		dB	
Noise Figure		11.9	14	dB	
IF Input Impedance		250		Ω	Differential @ 130MHz
RF Output VSWR		1.5	2:1		824MHz to 849MHz, external components required
Output IP3	-4	+5.4		dBm	
Current Consumption		26		mA	
LO Input					954MHz to 979MHz
LO Frequency Range		954 to 979		MHz	
LO Level	-6	-3	0	dBm	
LO Input Impedance		50		Ω	
LO to Mixer RF Output Leakage		-33	-20	dBm	
LO Input VSWR		1.4	2:1		GAIN SELECT=0V
		1.7	2:1		GAIN SELECT=2.7V
Power Supply					
Voltage	2.7	3.0	3.3	V	
Current Consumption			18	mA	V_{PD}=0V

NOTE: The measured results do not include the losses from the IF balun and SAW filter. On the evaluation board, those losses are as follows: IF Balun=1dB, SAW Filter=2.5dB to 3.5dB.

Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane. This pin is internally connected to the die flag.	
2	RF OUT	Output match of the second stage of the power amplifier driver. This amplifier output pin is open collector. It is matched to 50Ω externally using a simple LC match. Refer to the application schematic.	
3	RF GND2	The ground connection for the second stage of the power amplifier driver. The inductance between this pin and the ground plane determines the gain of the second stage. Increased inductance results in reduced gain. On the evaluation board, the emitter ground inductance is set by the length of the PCB trace connected between this pin and the ground. By sliding a 0Ω ground jumper along this line, the inductance, and hence the gain, may be varied. The evaluation board is shipped with the 0Ω jumper very close to the part, resulting in minimum inductance, and therefore maximum second stage gain. This translates to higher output IP3 and maximum ACPR1. This setting results in performance 6dB better than the ACPR1 minimum specification of 50dBc in the CDMA IS-95 specification for a P_{OUT}=+5dBm.	
4	RF GND1	The ground connection for the first stage of the power amplifier driver. The inductance between this pin and the ground plane determines the gain of the first stage. Increased inductance results in reduced gain. On the evaluation board, the emitter ground inductance is set by the length of the PCB trace connected between this pin and the ground. By sliding a 0Ω ground jumper along this line, the inductance, and hence the gain, may be varied. The evaluation board is shipped with the 0Ω jumper far away from the part, resulting in maximum inductance, and therefore minimum first stage gain. More gain may be obtained by shifting the 0Ω jumper toward the part. A maximum total gain of 40dB may be achieved if the first stage is set to minimum emitter inductor trace length.	See pin 3.
5	VPA1	Power supply pin for the first stage power amplifier. External components provide tuning for the interstage match.	
6	RF IN	RF input to the power amplifier. This input is DC-coupled, so an external blocking capacitor is needed if the pin is connected to a DC path.	
7	PD	Power Down control When this pin is low, the amplifier section of the IC is shut off. When this pin is high, the amplifier section of the IC is turned on. The upconverter portion of the IC remains on regardless of the state of PD.	
8	MIX OUT	Output for the upconverting mixer. This input is DC-coupled, so an external blocking capacitor is needed if the pin is connected to a DC path. The output impedance is 50Ω.	
9	GND	Same as pin 1.	

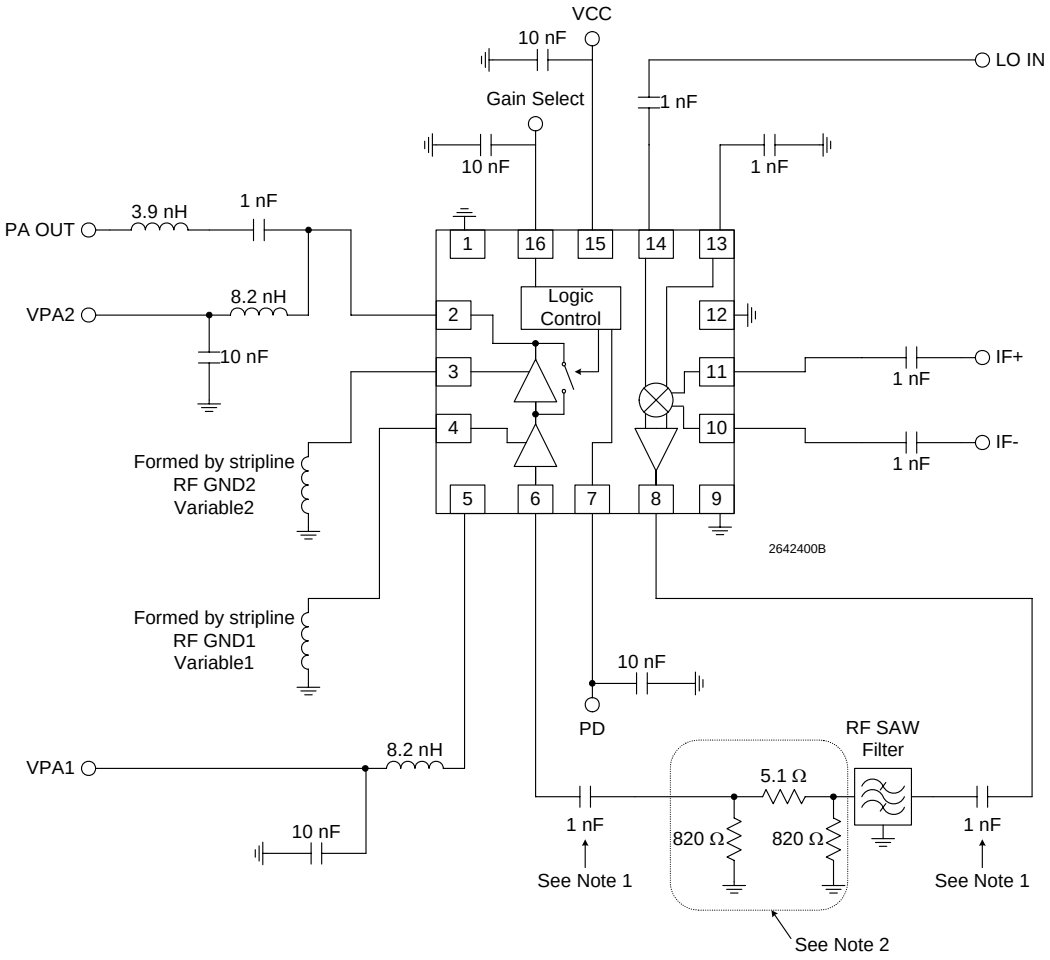
Pin	Function	Description	Interface Schematic
10	IF-	Balanced IF Input Pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other IF input is AC coupled to ground. The input impedance is 250Ω in both the balanced and single-ended modes.	
11	IF+	Same as pin 10, except complementary input.	
12	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
13	LO-	Balanced LO Input Pin. This pin is internally DC-biased and should be DC-blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The input impedance is 50Ω in both the balanced and single-ended modes.	
14	LO+	Same as pin 13, except complementary input.	
15	VCC	Supply voltage for all bias circuits and logic circuits.	
16	GAIN SELECT	When GAIN SELECT is high: the driver amplifier is switched to high gain mode; both amplifier stages are active; the gain is maximized; and, the entire device draws approximately 51mA. When GAIN SELECT is low, the second stage of the PA driver is turned off and bypassed. This results in a device current of 26mA, which is approximately a 50% current reduction. The upconverting mixer remains on in both the high and low gain modes to prevent VCO pulling.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

PD	Gain Select	Mixer	Amplifier First Stage	Amplifier Second Stage	Gain (dB)*
0	0	ON	OFF	OFF	
0	1	ON	OFF	OFF	
1	0	ON	ACTIVE	BYPASSED	11.9
1	1	ON	ACTIVE	ACTIVE	34.5

*See parameter specifications for conditions.

Application Schematic

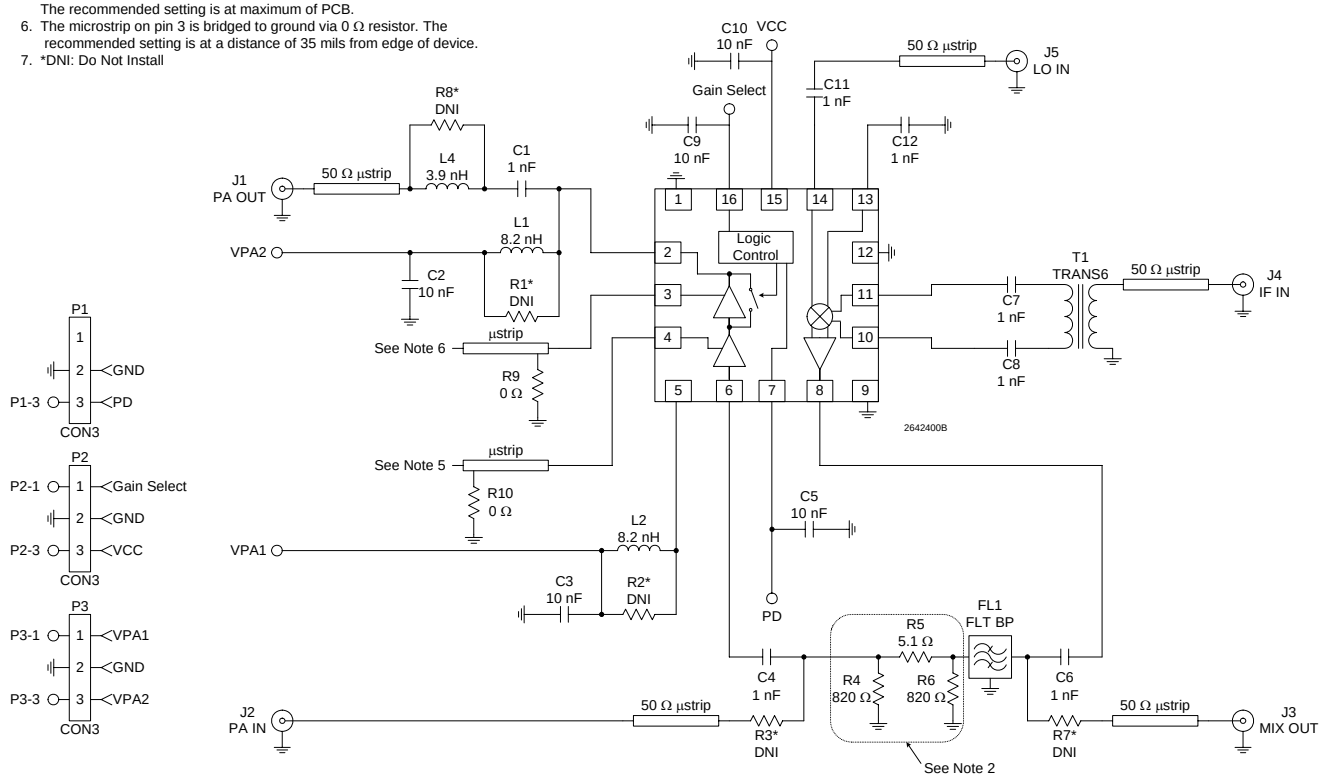
NOTE:
1. 1 nF: DC blocking capacitor - this can be removed if the filter is DC blocked.
2. T-attenuator - this is to control the overall gain of the upconverter + PA driver. This can be set to zero if it is desired.



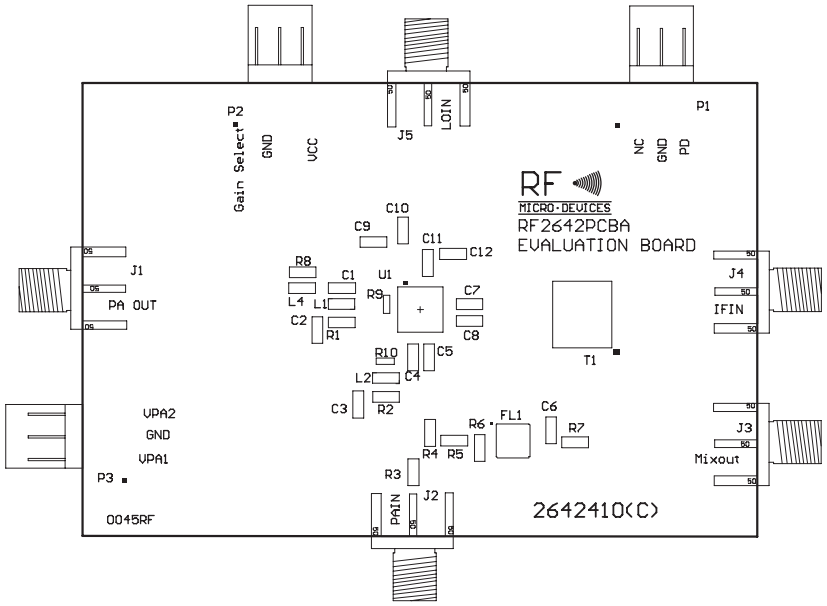
Evaluation Board Schematic

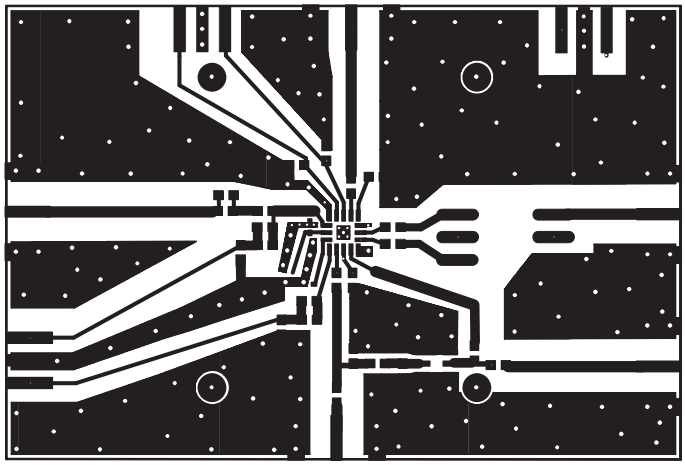
(Download Bill of Materials from www.rfmd.com.)

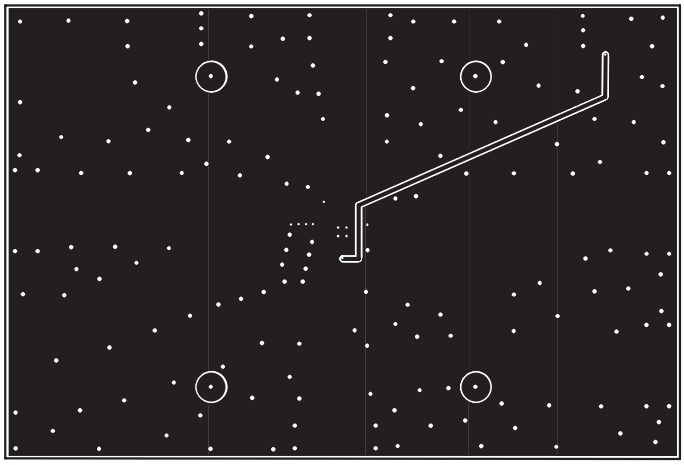
NOTE:
1. R1, R2 and R8 are optional.
2. R4, R5 and R6 form T-attenuator with a loss of 1 dB.
   For 0 dB loss, R4 and R6 are removed, and R5 is a 0 Ω short.
3. R3 and R7 are normally open.
4. FLT BP recommended is a Murata filter: SAFC836.5MC90T-TC12.
5. The microstrip on pin 4 is bridged to ground via 0 Ω 0402 size resistor.
   The recommended setting is at maximum of PCB.
6. The microstrip on pin 3 is bridged to ground via 0 Ω resistor. The
   recommended setting is at a distance of 35 mils from edge of device.
7. *DNI: Do Not Install



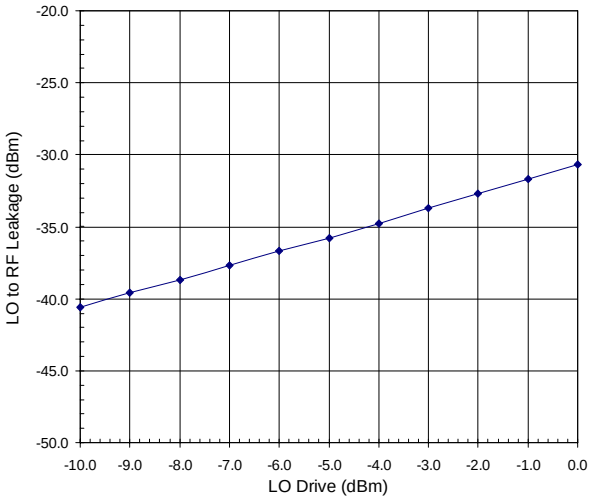
Evaluation Board Layout
Board Size 2.981" x 2.981"
Board Thickness 0.031", Board Material FR-4



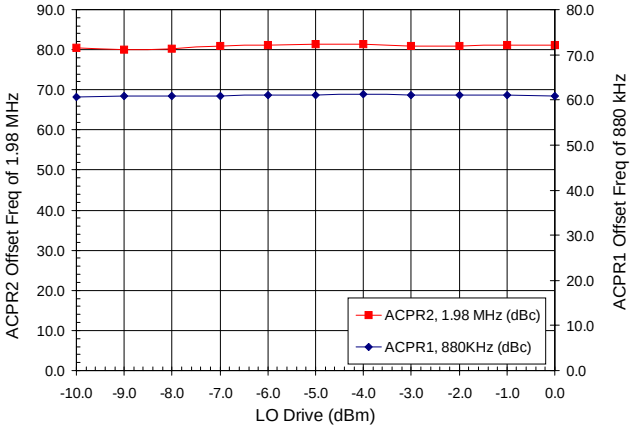




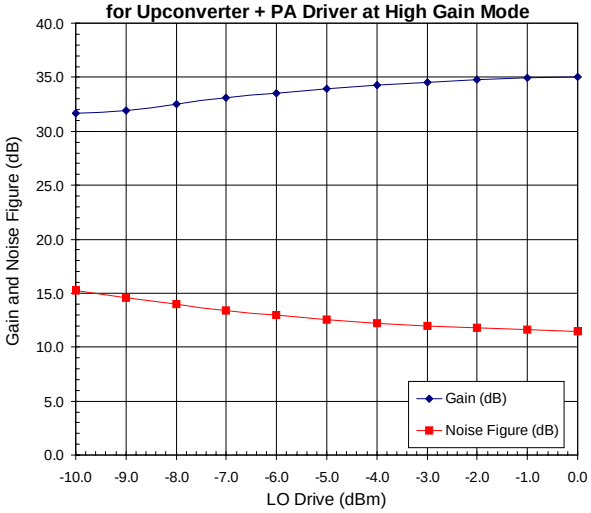
LO to RF Leakage for Upconverter Mixer Alone



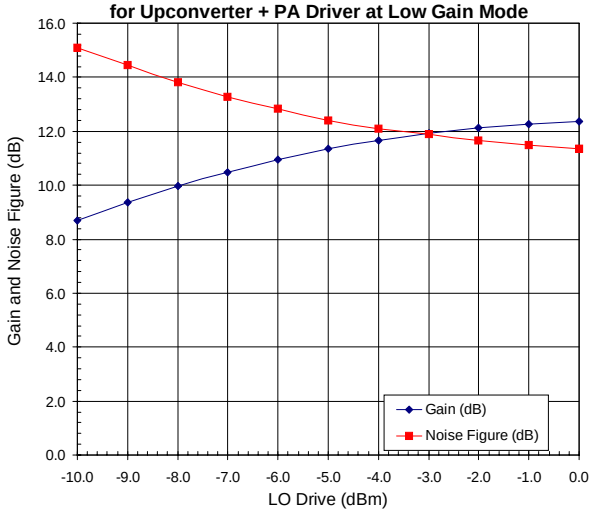
ACPR1 and ACPR2 versus LO Drive at V_{CC}=3.0V for Upconverter + PA Driver at High Gain Mode



Gain and Noise Figure versus LO Drive at V_{CC}=3.0V for Upconverter + PA Driver at High Gain Mode



Gain and Noise Figure versus LO Drive at V_{CC}=3.0V for Upconverter + PA Driver at Low Gain Mode



Output IP3 versus Drive Level at V_{CC}=3.0V for Upconverter + PA Driver at Low Gain Mode