PI6CV855

PLL Clock Driver for 2.5V SSTL_2 DDR SDRAM Memory

Product Features

- PLL clock distribution optimized for SSTL_2 DDR SDRAM applications.
- Distributes one differential clock input pair to five differential clock output pairs.
- Inputs (CLK,$\overline{CLK}$) and (FBIN,$\overline{FBIN}$): SSTL_2
- Outputs (Yx, $\overline{Yx}$), (FBOUT, $\overline{FBOUT}$): SSTL_2
- External feedback pins (FBIN,$\overline{FBIN}$) are used to synchronize the outputs to the clock input.
- Operates at AV_{DD} = 2.5V for core circuit and internal PLL, and V_{DDQ} = 2.5V for differential output drivers
- Available Package:
  – Plastic 28-pin TSSOP

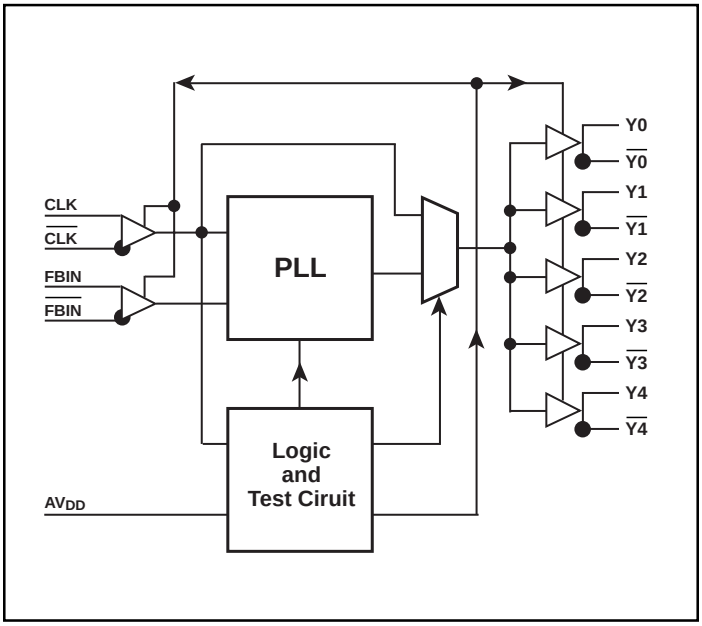
Product Description

PI6CV855 PLL clock device is developed for SSTL_DDR SDRAM applications. This PLL Clock Buffer is designed for 2.5 V_{DDQ} and 2.5V AV_{DD} operation and differential data input and output levels. The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{CLK}$) to five differential pairs of clock outputs (Y[0:4], $\overline{Y}$[0:4]) and one differential pair feedback clock outputs (FBOUT, $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CLK, $\overline{CLK}$), the feedback clocks (FBIN,$\overline{FBIN}$), and the Analog Power input (AV_{DD}). When the AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

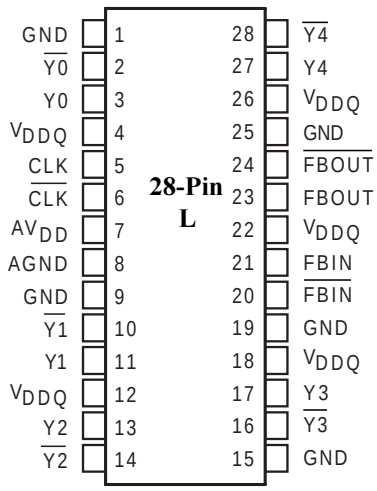
When the input frequency falls below a suggested detection frequency that is below the operating frequency of the PLL, the device will enter a low power mode. In low power mode, PLL is turned OFF, Y[0:4] and $\overline{Y}$[0:4] outputs are 3-stated.

The PI6CV855 is able to track Spread Spectrum Clocking to reduce EMI.

Block Diagram



Pin Configuration



Pinout Table

Pin Name	Pin No.	I/O Type	Description
CLK $\overline{CLK}$	5 6	I	Reference Clock input
Y[0:4]	3,11,13,17,27	O	Clock outputs.
$\overline{Y[0:4]}$	2,10,14,16,28		Complement Clock outputs.
FBOUT $\overline{FBOUT}$	23 24		Feedback output, and Complement Feedback Output
FBIN $\overline{FBIN}$	21 20	I	Feedback input, and Complement Feedback input
V_{DDQ}	4,12,18,22,26	Power	Power Supply for I/O pins.
AV_{DD}	7		Analog/core power supply. AV_{DD} can be used to bypass the PLL for testing purposes. When AV_{DD} is strapped to ground, PLL is bypassed & CLK is buffered directly to the device outputs.
AGND	8	Ground	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	1,9,15,19,25		Ground for I/O pins.

Function Table

Inputs			Outputs				PLL State
AV_{DD}	CLK	$\overline{CLK}$	Y[0:4]	$\overline{Y[0:4]}$	FBOUT	$\overline{FBOUT}$	
GND	L	H	Z	Z	Z	Z	Bypassed/Off
GND	H	L	Z	Z	Z	Z	Bypassed/Off
2.5V(nom)	L	H	L	H	L	H	on
2.5V(nom)	H	L	H	L	H	L	on
2.5V(nom)	<20 MHz		Z	Z	Z	Z	off

Notes: For testing and power saving purposes, PI6CV855 will power down if the frequency of the reference inputs CLK, $\overline{CLK}$ is well below the operating frequency range. The maximum power down clock frequency is below 20 MHz. For example, PI6CV855 will be powered down when the CLK,$\overline{CLK}$ stop running.

Z = High impedance
X = Don't care

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V_{DDQ}, AV_{DD}	I/O supply voltage range and analog/core supply voltage range	– 0.5	3.6	V
V_I	Input voltage range	– 0.5	V_{DDQ}+0.5	
V_O	Output voltage range	– 0.5		
Tstg	Storage temperature	– 65	150	°C

Note: Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Timing Requirements (Over recommended operating free-air temperature)

Symbol	Description	AV_{DD}, V_{DDQ} = 2.5V ±0.2V		Units
		Min.	Max.	
f_{CK}	Operating clock frequency(1,2)	60	170	MHz
	Application clock frequency(3)	95	170	
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	PLL stabilization time after powerup		100	µs

Notes:
1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

DC Specifications

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
AV_{DD}	Analog/core supply voltage	2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	
V_{OH}	High-level output voltage	1.8		V_{DDQ}	
V_{OL}	Low-level output voltage	0		0.5	
V_{IX}	Input differential-pair crossing voltage	$(V_{DDQ}/2)$ –0.2		$(V_{DDQ}/2)$ +0.2	
V_{OX}	Output differential-pair crossing voltage at the SDRAM clock input	$(V_{DDQ}/2)$ –0.2		$(V_{DDQ}/2)$ +0.2	
V_{IN}	Input voltage level	–0.3		V_{DDQ} +0.3	
V_{ID}	Input differential voltage between CLK and $\overline{CLK}$	0.36		V_{DDQ} +0.6	
V_{OD}	Output differential voltage between Y[n] and $\overline{Y[n]}$ and FBOUT and $\overline{FBOUT}$	0.7		V_{DDQ} +0.6	
T_A	Operating free air temperature	0		70	°C

Electrical Characteristics

Parameter		Test Conditions	A_{VDD}, V_{DDQ}	Min.	Typ.	Max.	Units
V_{IK}	All inputs	I_I = –18mA	2.3V			–1.2	V
I_I	CLK, FBIN	$V_I = V_{DDQ}$ or GND	2.7V			±10	µA
I_{DDQ}	Dynamic supply current of V_{DDQ}	V_{DD} = 2.7V (1)				300	mA
	Static supply current	CLK & $\overline{CLK}$ <20 MHz				100	µA
I_{ADD}	Dynamic supply current of AV_{DD}	V_{DD} = 2.7V (1)				12	mA
	Static supply current	CLK & $\overline{CLK}$ <20 MHz				100	µA
C_I	CLK and $\overline{CLK}$	$V_I = V_{DD}$ or GND	2.5V	2.0		3.0	pF
	FBIN and $\overline{FBIN}$						

Notes:
1. Driving 9 or 18 DDR SDRAM memory chips with 120-ohm termination resistor for each clock output pair at 134 MHz.
2. The maximum power down clock frequency is below 20 MHz.

AC Specifications

Switching characteristics over recommended operating free-air temperature range, f_{CLK} > 100 MHz (unless otherwise noted). (See Figure 1 and 2)

Parameter	Description	Diagram	AV_{CC}, V_{DDQ} = 2.5V ±0.2V			Units
			Min.	Nom.	Max	
t(θ)	Static phase offset(1)	Figure 4	–50	0	50	ps
tjit(cc)	Cycle-to-cycle jitter	Figure 3	–75		75	
tjit(per)	Period jitter	Figure 6	–75		75	
tjit(hper)	Half-period jitter	Figure 7	–100		100	
tsl(i)	Input clock slew rate(2)	Figure 8	1.0		2.0	V/ns
tsl(o)	Output clock slew rate(2)	Figure 8	1.0		2.0	
tsk(o)	Output clock skew	Figure 5			100	ps
The PLL on the PI6CV855 meets all the above parameters while supporting SSC synthesizers with the following parameters(3).						
	SSC modulation frequency		30.0		50.0	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
	PLL loop bandwidth			2		MHz
	Phase angle				–0.031	degrees

Notes:

1. Static Phase offset does not include jitter.
2. The slew rate is determined from the IBIS model with test load shown in Figure 1.
3. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

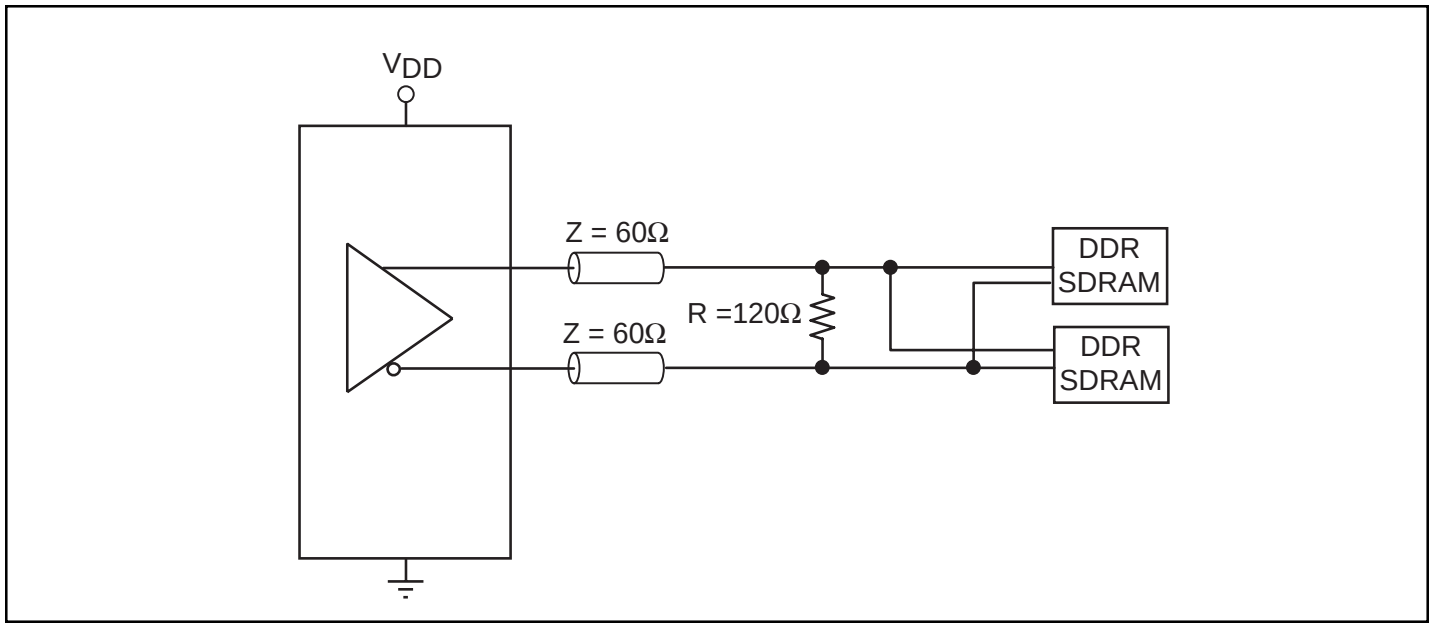


Figure 1. IBIS Model Output Load

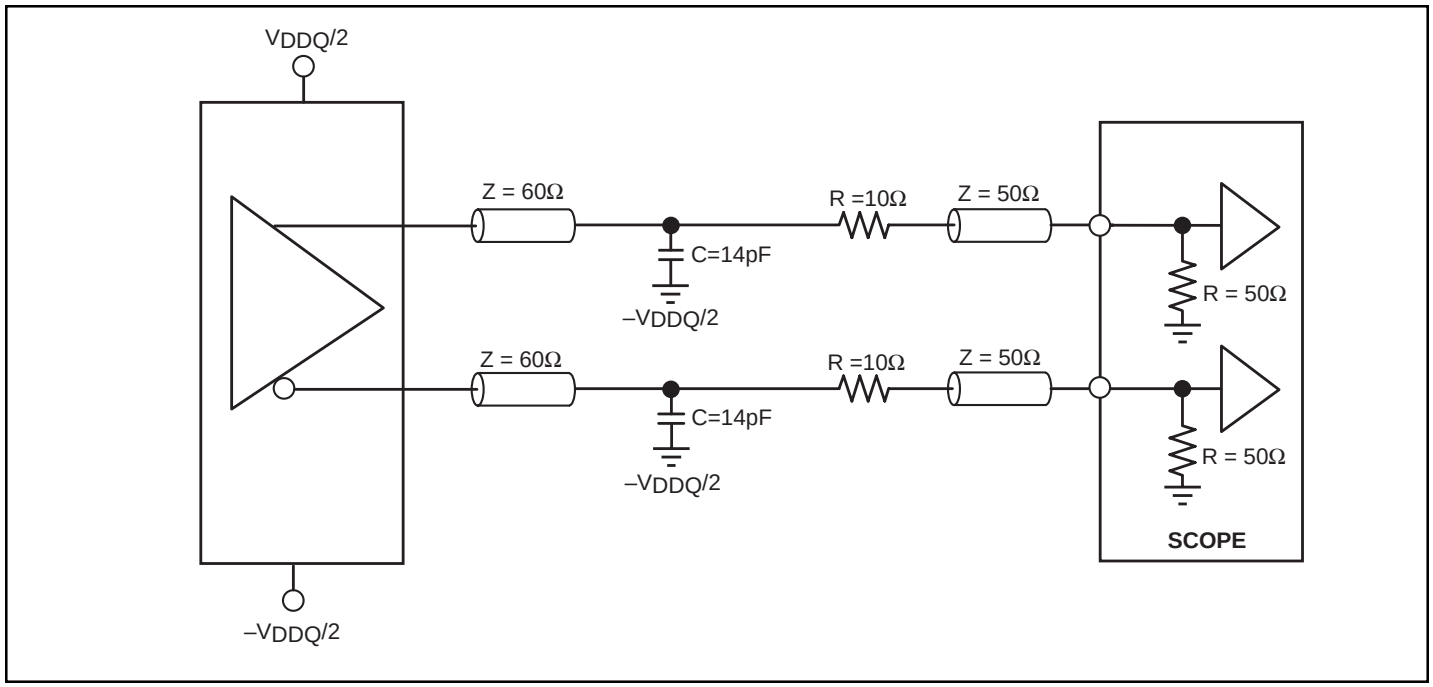


Figure 2. Output Load Test Circuit

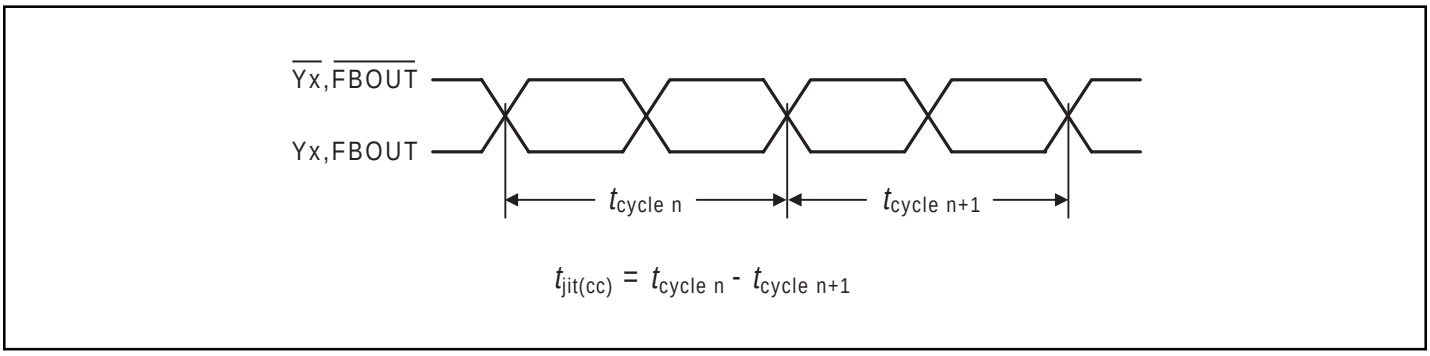


Figure 3. Cycle-to-Cycle Jitter

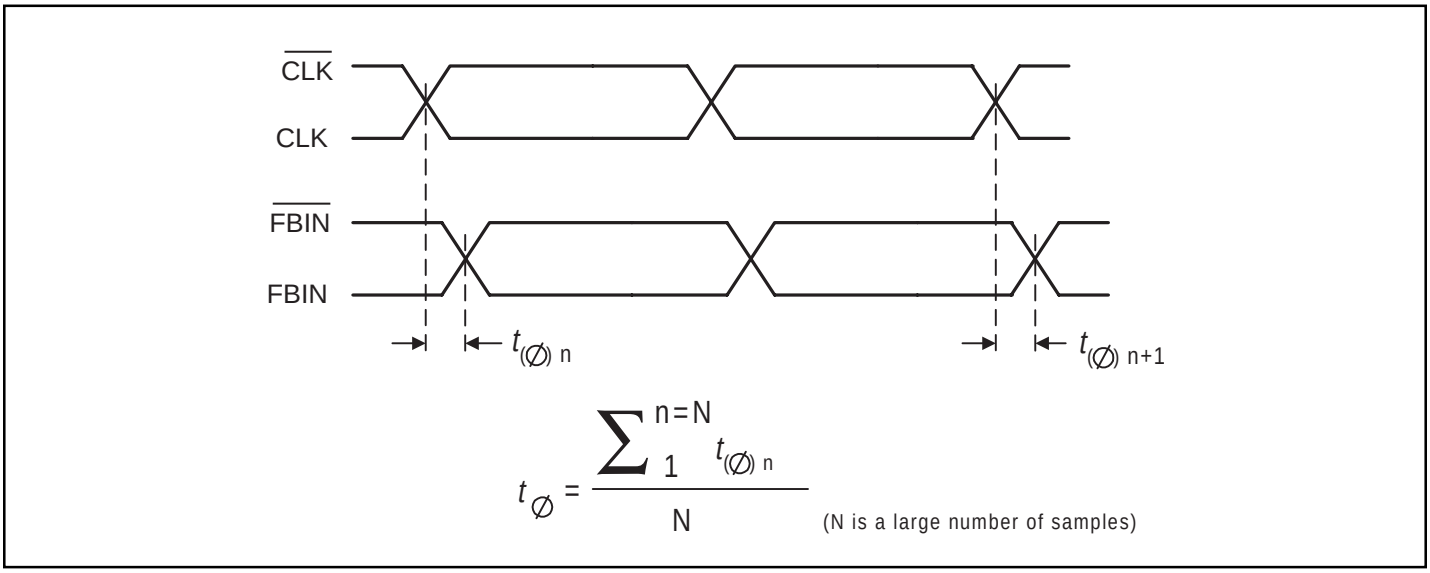


Figure 4. Static Phase Offset

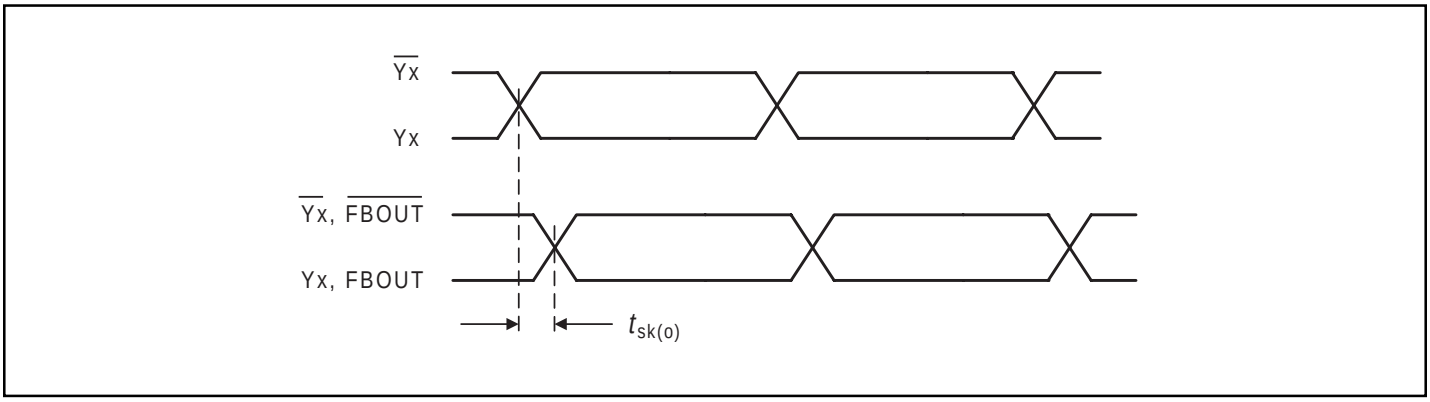


Figure 5. Output Skew

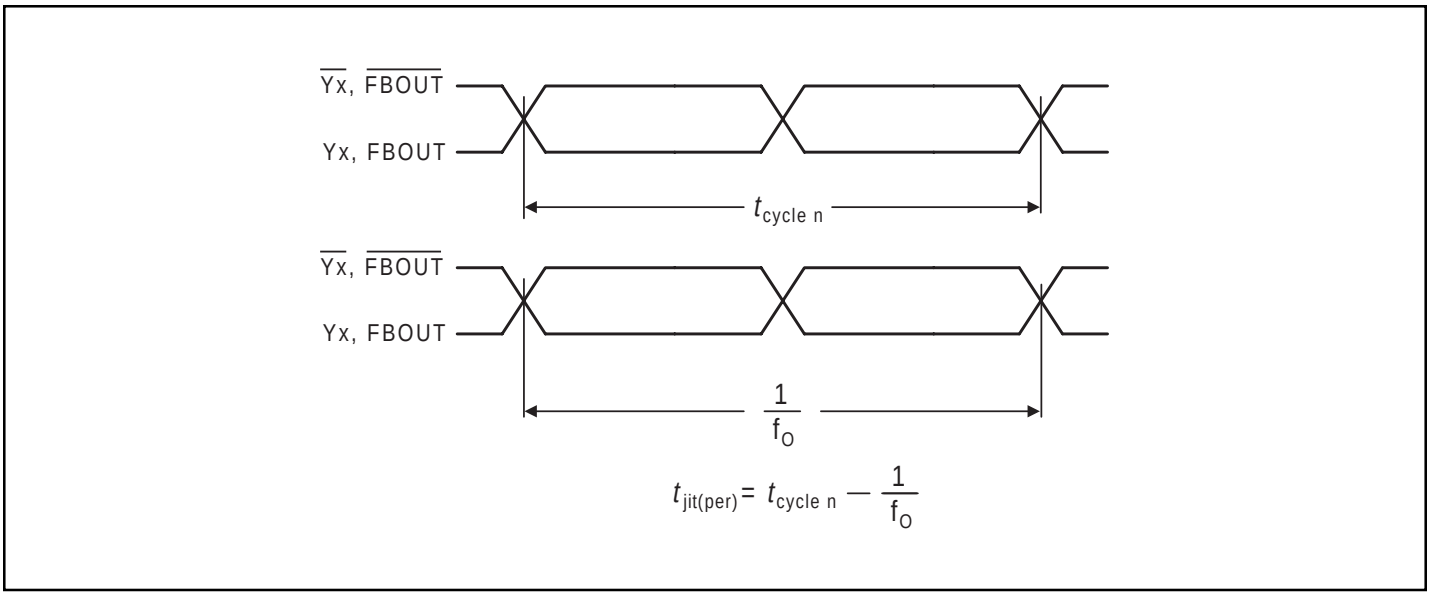


Figure 6. Period Jitter

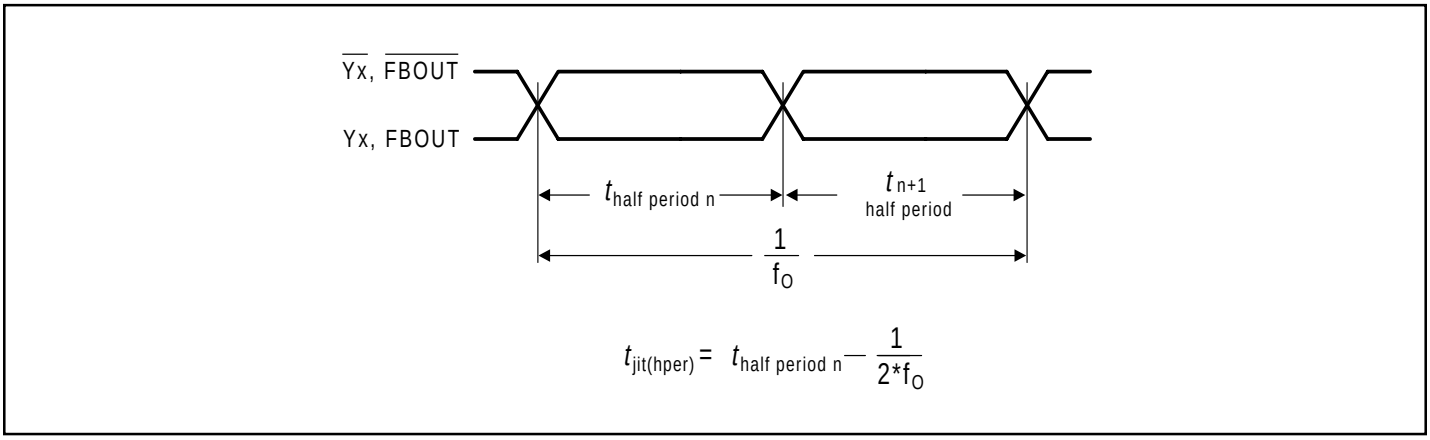


Figure 7. Half-Period Jitter

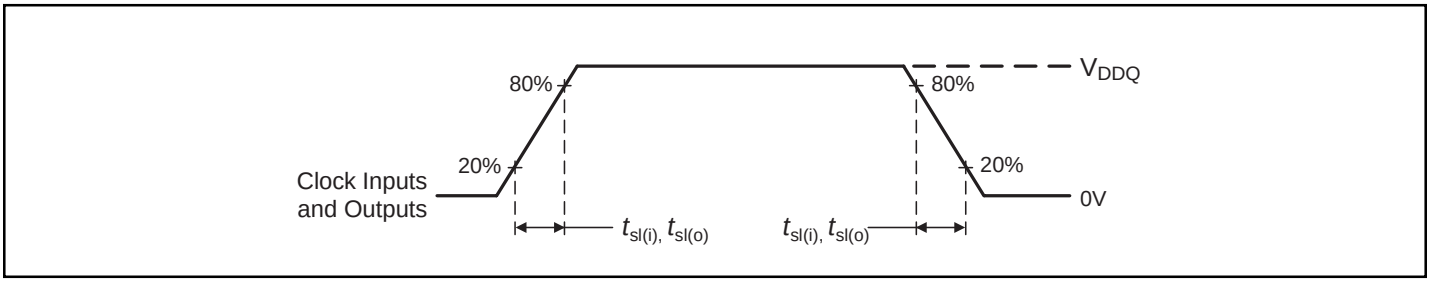
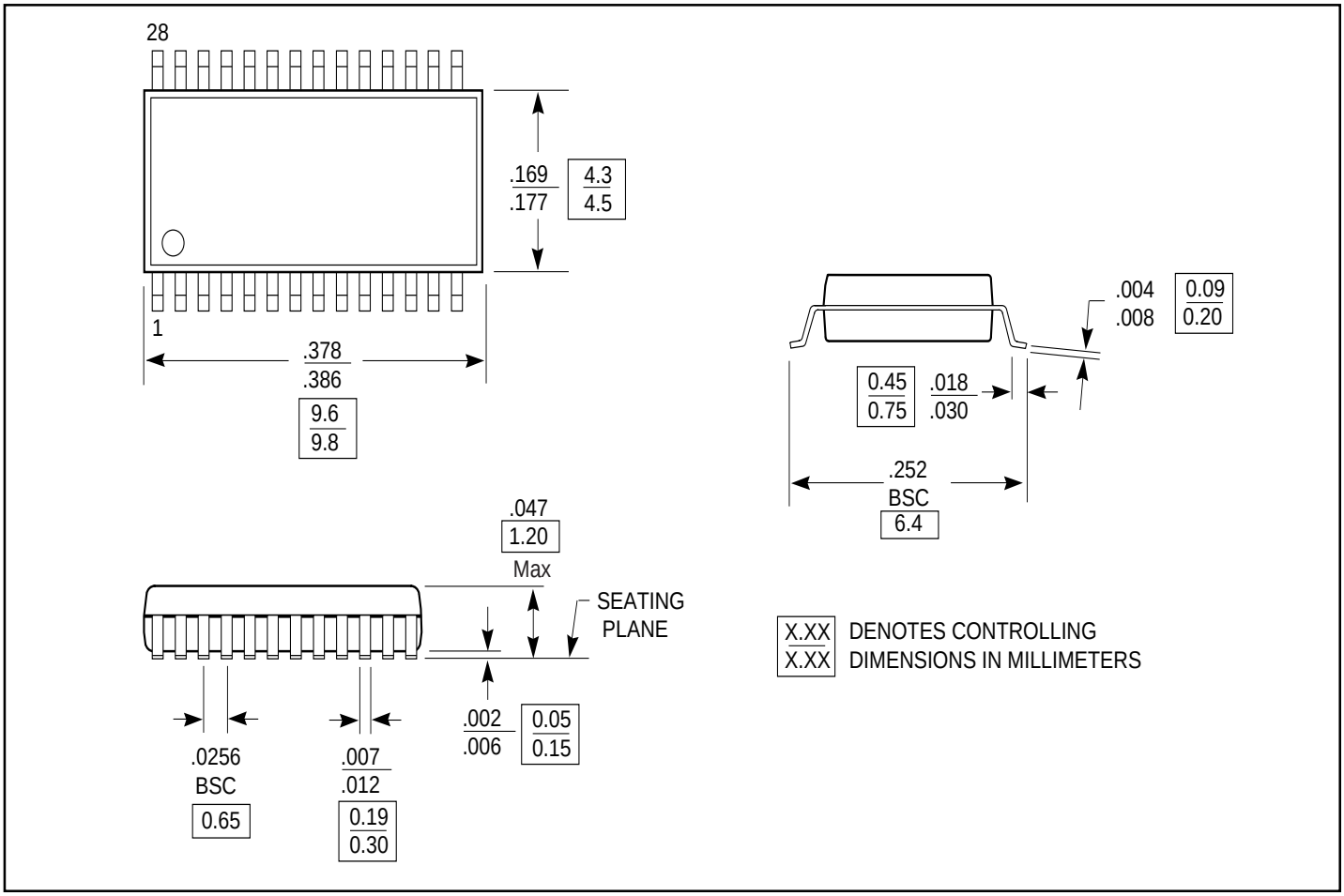


Figure 8. Input and Output Slew Rates

Packaging Mechanical: 28-Pin TSSOP (L)



Ordering Information

Ordering Code	Package Name	Package Type
PI6CV855L	L28	28-pin, 4.4mm wide TSSOP