

**PowerMOS transistors  
Avalanche energy rated**

**PHP4N40E, PHB4N40E**

**FEATURES**

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

**SYMBOL**



**QUICK REFERENCE DATA**

$V_{DSS} = 400\text{ V}$
$I_D = 4.4\text{ A}$
$R_{DS(ON)} \leq 1.8\ \Omega$

**GENERAL DESCRIPTION**

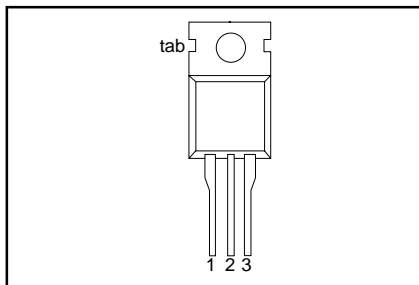
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP4N40E is supplied in the SOT78 (TO220AB) conventional leaded package.  
The PHB4N40E is supplied in the SOT404 surface mounting package.

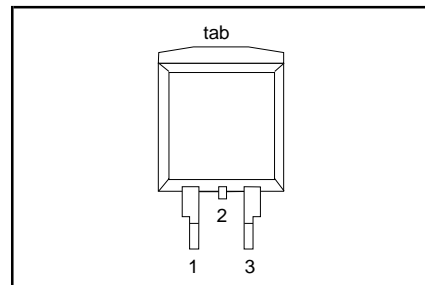
**PINNING**

PIN	DESCRIPTION
1	gate
2	drain <sup>1</sup>
3	source
tab	drain

**SOT78 (TO220AB)**



**SOT404**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DSS}$	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	400	V
$V_{DGR}$	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	400	V
$V_{GS}$	Gate-source voltage		-	$\pm 30$	V
$I_D$	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$	-	4.4	A
$I_{DM}$	Pulsed drain current	$T_{mb} = 100\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$	-	2.7	A
$P_D$	Total dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	18	W
$T_j, T_{stg}$	Operating junction and storage temperature range	$T_{mb} = 25\text{ }^\circ\text{C}$	-55	150	$^\circ\text{C}$

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### AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{AS}$	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 2.7$ A; $t_p = 0.28$ ms; $T_j$ prior to avalanche = 25°C; $V_{DD} \leq 50$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; refer to fig:17	-	195	mJ
$E_{AR}$	Repetitive avalanche energy <sup>1</sup>	$I_{AR} = 4.4$ A; $t_p = 2.5$ μs; $T_j$ prior to avalanche = 25°C; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; refer to fig:18	-	5.7	mJ
$I_{AS}, I_{AR}$	Repetitive and non-repetitive avalanche current		-	4.4	A

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 package, pcb mounted, minimum footprint	-	60 50	-	K/W K/W

<sup>1</sup> pulse width and repetition rate limited by  $T_j$  max.

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### ELECTRICAL CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	400	-	-	V
$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	$V_{GS} = 10\text{ V}; I_D = 2.2\text{ A}$	-	1.3	1.8	$\Omega$
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	2.0	3.0	4.0	V
$g_{fs}$	Forward transconductance	$V_{DS} = 30\text{ V}; I_D = 2.2\text{ A}$	1.3	2.2	-	S
$I_{DSS}$	Drain-source leakage current	$V_{DS} = 400\text{ V}; V_{GS} = 0\text{ V}$	-	1	25	$\mu\text{A}$
$I_{GSS}$	Gate-source leakage current	$V_{DS} = 320\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ °C}$ $V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	30	250	$\mu\text{A}$
$Q_{g(tot)}$	Total gate charge	$I_D = 4.4\text{ A}; V_{DD} = 320\text{ V}; V_{GS} = 10\text{ V}$	-	26	30	nC
$Q_{gs}$	Gate-source charge		-	2	4	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	14	17	nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}; R_D = 47\text{ }\Omega;$	-	10	-	ns
$t_r$	Turn-on rise time	$R_G = 18\text{ }\Omega$	-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
$t_f$	Turn-off fall time		-	38	-	ns
$L_d$	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	310	-	pF
$C_{oss}$	Output capacitance		-	60	-	pF
$C_{rss}$	Feedback capacitance		-	36	-	pF

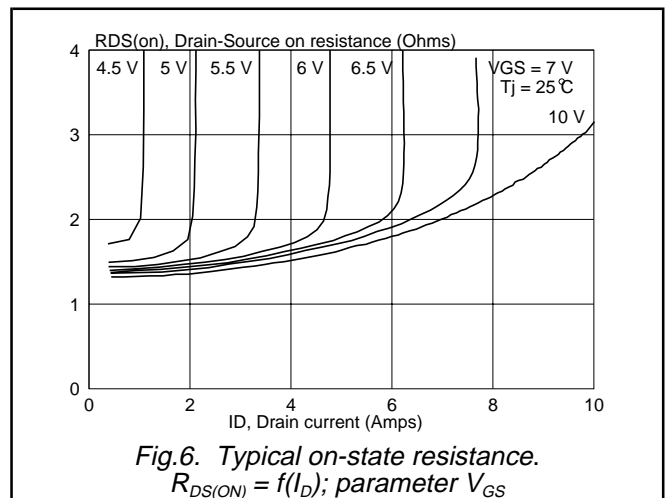
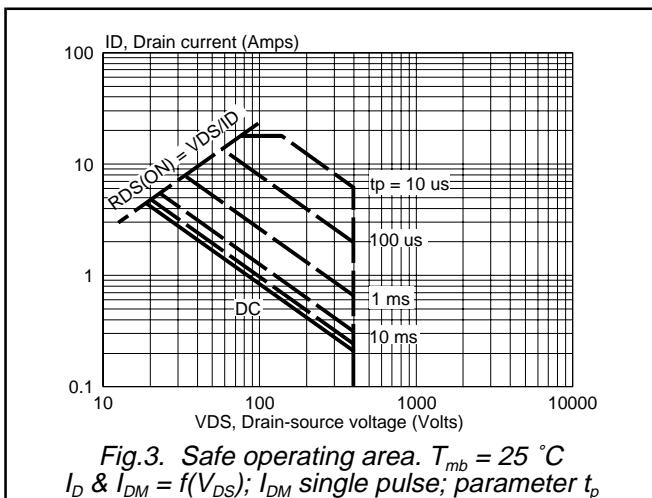
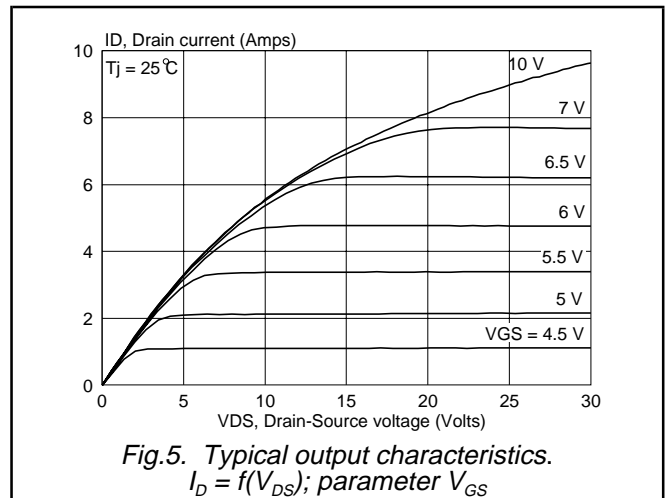
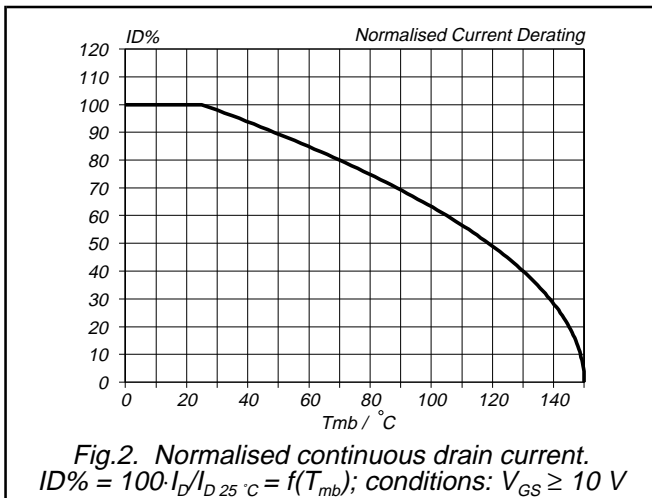
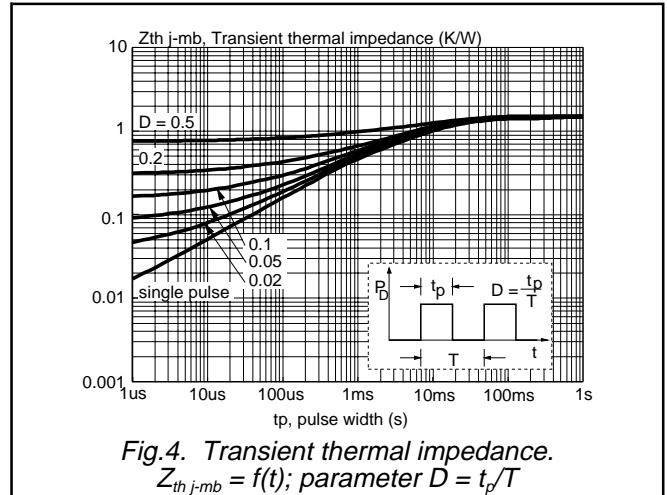
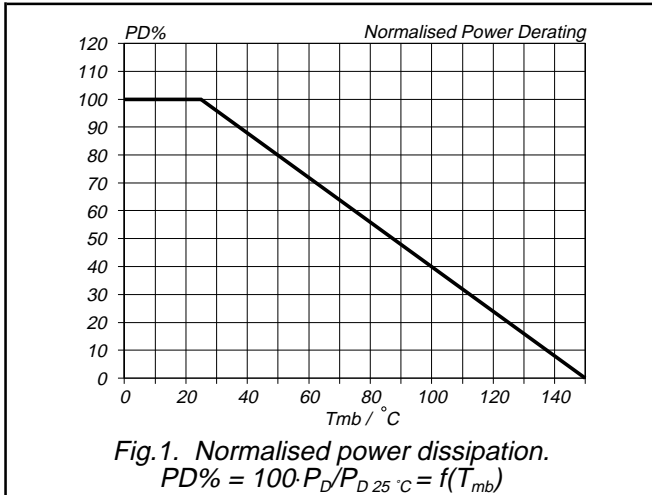
### SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_S$	Continuous source current (body diode)	$T_{mb} = 25\text{ °C}$	-	-	4.4	A
$I_{SM}$	Pulsed source current (body diode)	$T_{mb} = 25\text{ °C}$	-	-	18	A
$V_{SD}$	Diode forward voltage	$I_S = 4.4\text{ A}; V_{GS} = 0\text{ V}$	-	-	1.2	V
$t_{rr}$	Reverse recovery time	$I_S = 4.4\text{ A}; V_{GS} = 0\text{ V}; di/dt = 100\text{ A}/\mu\text{s}$	-	250	-	ns
$Q_{rr}$	Reverse recovery charge		-	2.2	-	$\mu\text{C}$

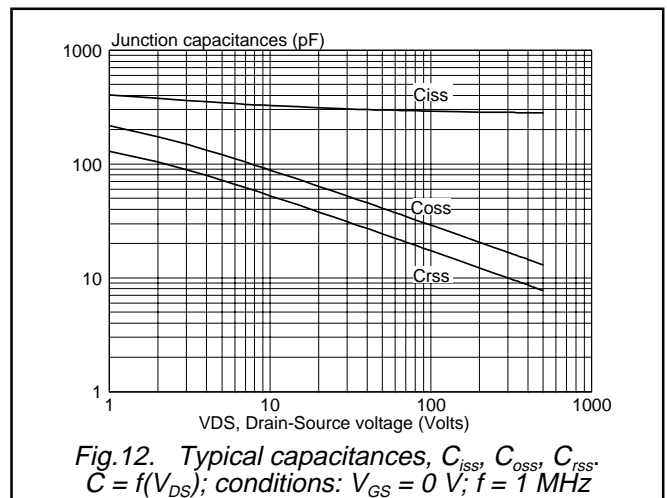
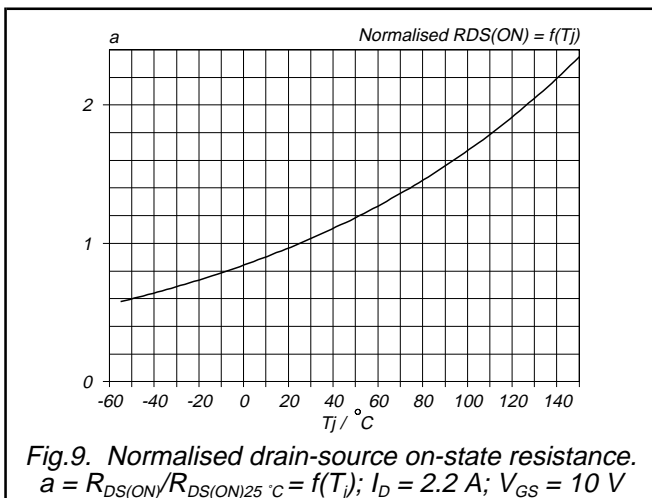
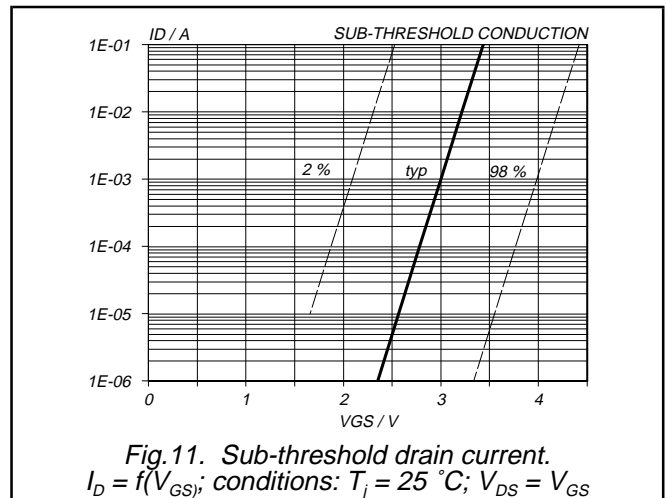
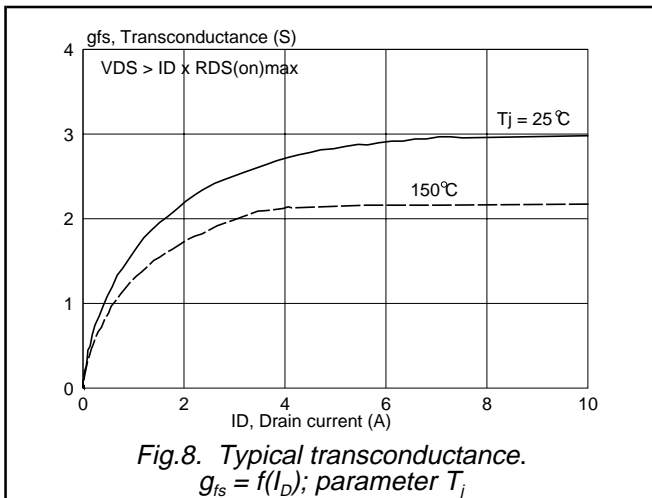
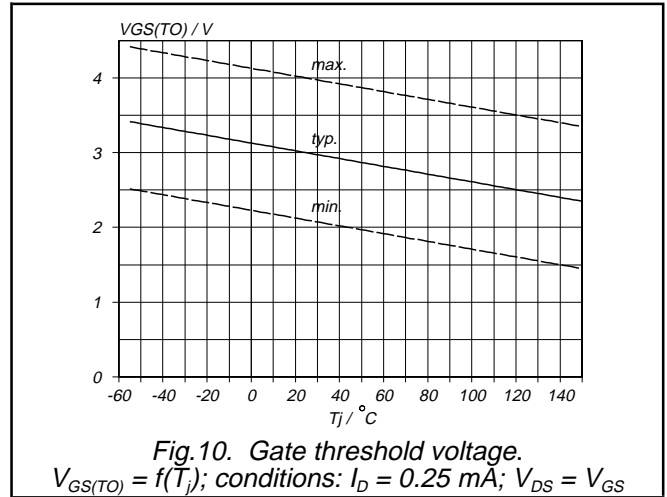
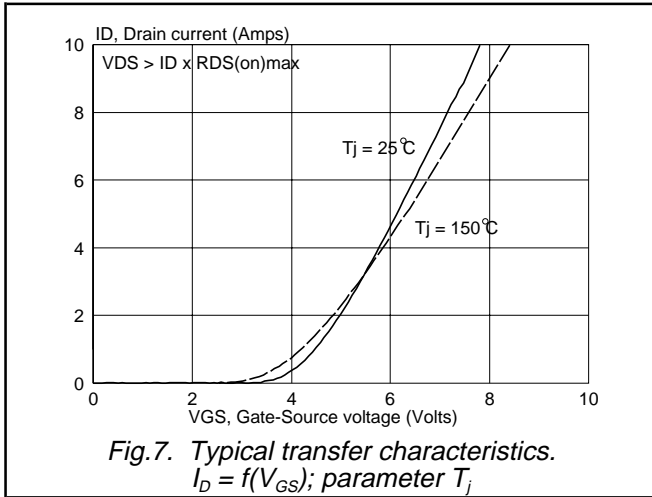
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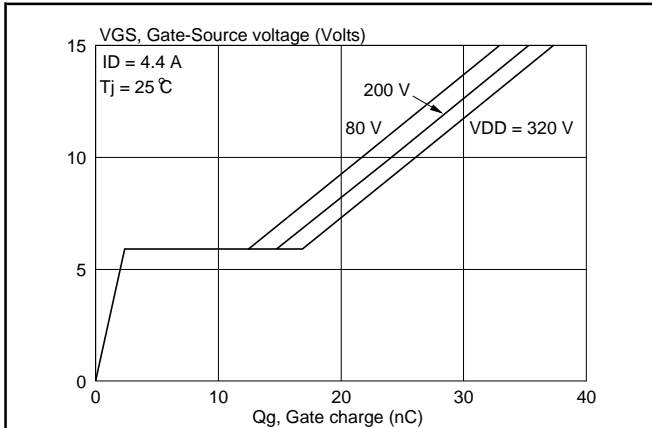


Fig. 13. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; parameter  $V_{DS}$

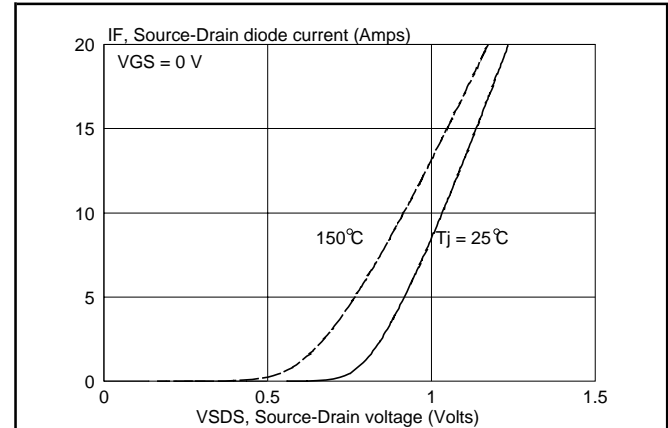


Fig. 16. Source-Drain diode characteristic.  
 $I_F = f(V_{SDS})$ ; parameter  $T_j$

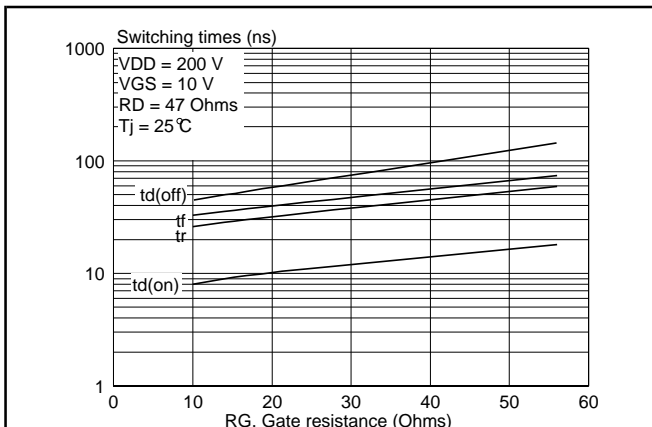


Fig. 14. Typical switching times;  $t_{d(on)}$ ,  $t_r$ ,  $t_{d(off)}$ ,  $t_f = f(R_G)$

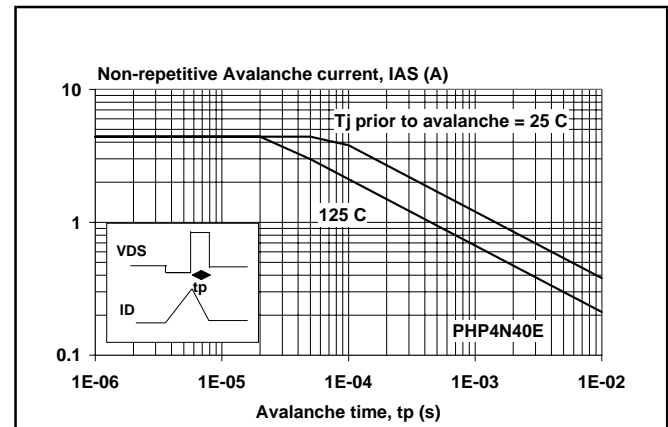


Fig. 17. Maximum permissible non-repetitive avalanche current ( $I_{AS}$ ) versus avalanche time ( $t_p$ ); unclamped inductive load

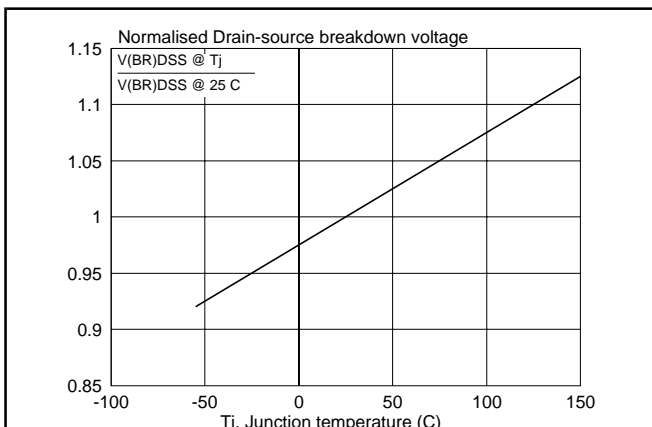


Fig. 15. Normalised drain-source breakdown voltage;  
 $V_{(BR)DSS} / V_{(BR)DSS 25 °C} = f(T_j)$

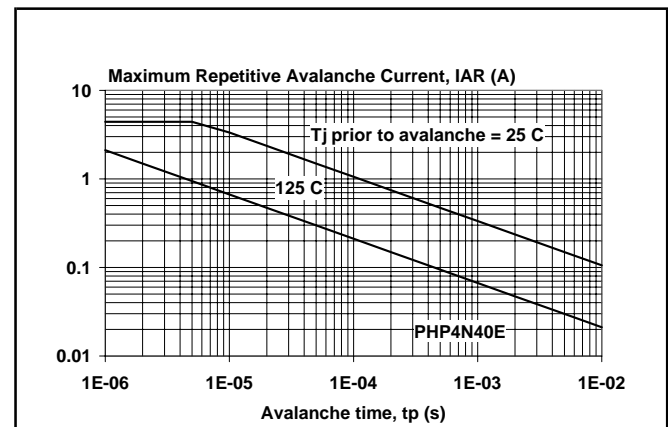


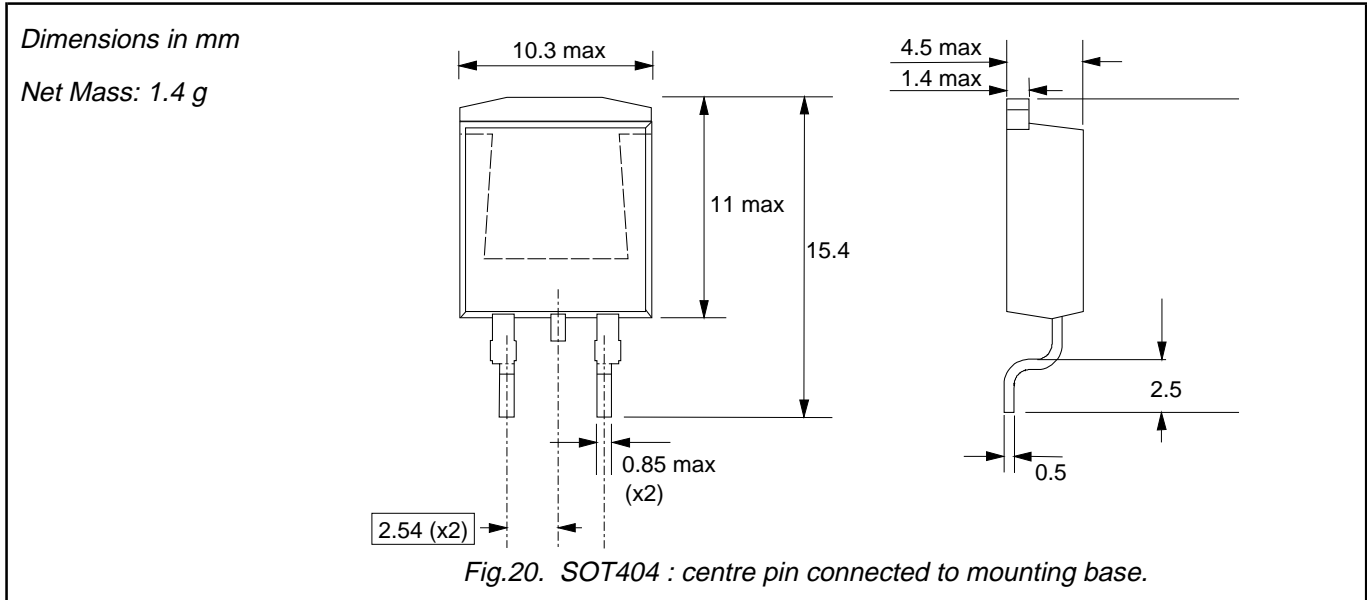
Fig. 18. Maximum permissible repetitive avalanche current ( $I_{AR}$ ) versus avalanche time ( $t_p$ )



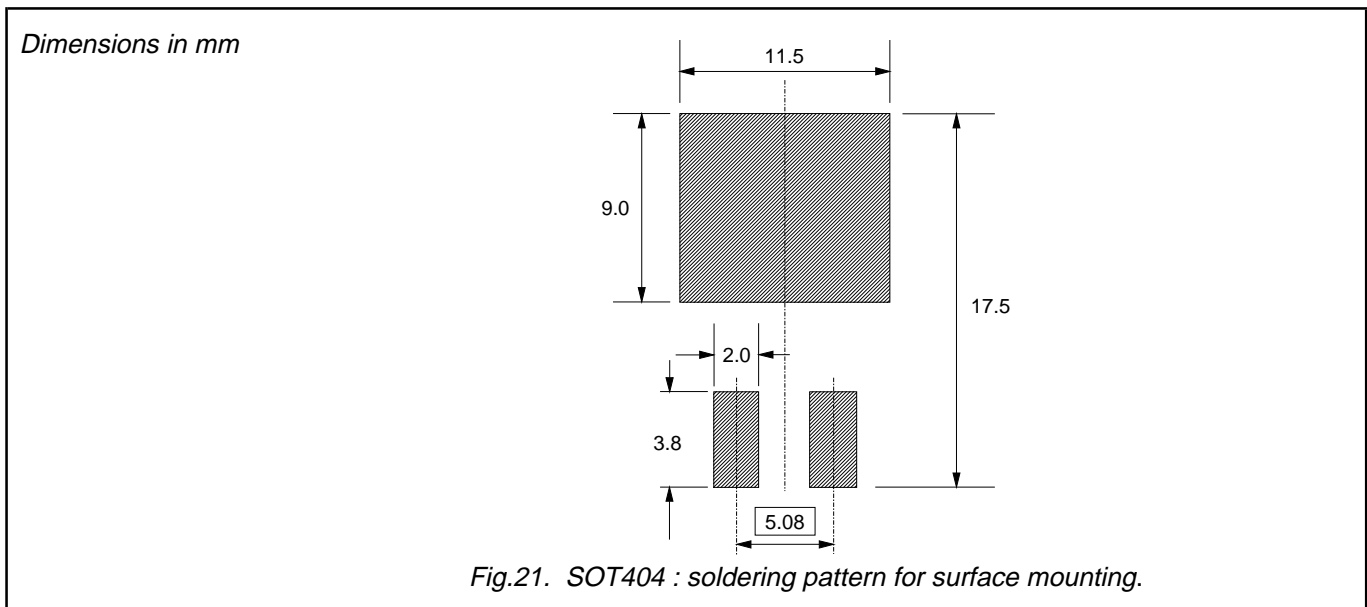
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**MECHANICAL DATA**



**MOUNTING INSTRUCTIONS**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".



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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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