PEREGRINE SEMICONDUCTOR

PRODUCT SPECIFICATION

# PE83512

**Military Operating Temperature Range**

## DC - 1500 MHz Low Power CMOS Divide-by-4 Prescaler

### Features

- DC to 1500 MHz operation
- Fixed divide ratio of 4
- Low-power operation: 14mA typical @ 3.0 V
- Ultra small package: 8-lead plastic MSOP

## Product Description

*The PE83512 is a high-performance static CMOS prescaler with a fixed divide ratio of 4. Its operating frequency range is DC to 1500 MHz. The PE83512 operates on a nominal 3 V supply and draws only 14mA. It is packaged in a small 8-lead plastic MSOP and is ideal for frequency scaling and clock generation solutions.*

*The PE83512 is manufactured in Peregrine's patented Ultra-Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.*

**Figure 1. Functional Schematic Diagram**

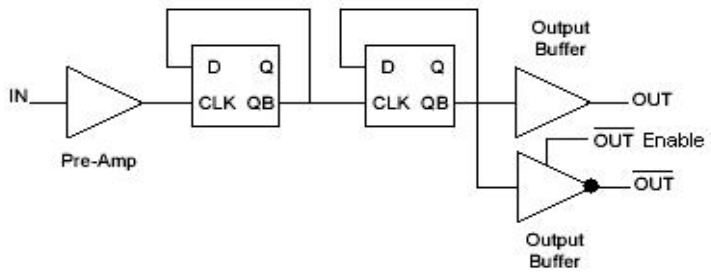



**Figure 2. Package Type**

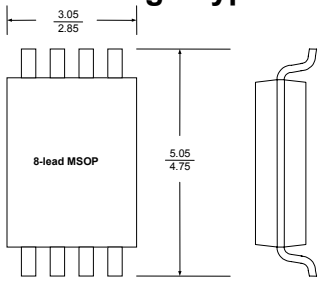
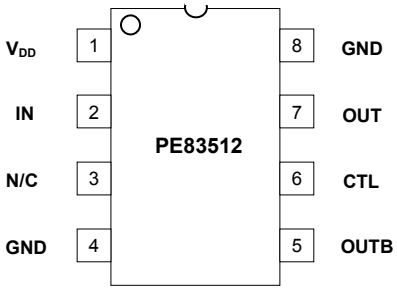



**Table 1. Electrical Specifications** ($Z_S = Z_L = 50\ \Omega$)

2.85V ≤ $V_{DD}$ ≤ 3.15 V; -55° C ≤ $T_A$ ≤ 125° C, unless otherwise specified

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Supply Voltage | | 2.85 | 3.0 | 3.15 | V |
| Supply Current[1] | OUTB Disabled | | 7 | 12 | mA |
| | OUTB Enabled | | 14 | 25 | mA |
| Input Frequency ($F_{IN}$) | | DC | | 1500 | MHz |
| Input Power ($P_{IN}$) | 100 MHz ≤ $F_{in}$ ≤ 1200 MHz<br>-55°C ≤ $T_A$ ≤ 85°C | -5 | | +10 | dBm |
| | 100 MHz ≤ $F_{in}$ ≤ 1200 MHz<br>85°C ≥ $T_A$ ≥ 125°C | 0 | | +10 | dBm |
| | 1200 MHz < $F_{in}$ ≤ 1500 MHz<br>-55°C ≤ $T_A$ ≤ 85°C | +5 | | +10 | dBm |
| Output Power | DC < Fin ≤ 1500MHz | +2 | | | dBm |

## Figure 3. Pin Configuration




## Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{DD}$ | Power supply pin. Bypassing is required (eg 1000 pF & 100 pF). |
| 2 | IN | Input signal pin. Should be coupled with a capacitor (eg 1000 pF). |
| 3 | N/C | No connection. This pin should be left open. |
| 4 | GND | Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance. |
| 5 | OUTB | Inverted divided frequency output. This pin should be coupled with a capacitor (eg 1000 pF). |
| 6 | CTL | Control pin. When grounded OUTB is enabled. |
| 7 | OUT | Divided frequency output pin. This pin should be coupled with a capacitor (eg 1000 pF). |
| 8 | GND | Ground Pin. |

## Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| VDD | Supply voltage | | 4.0 | V |
| $P_{in}$ | Input Power | | 15 | dBm |
| $V_{IN}$ | Voltage on input | -0.3 | VDD +0.3 | V |
| $T_{ST}$ | Storage temperature range | -65 | 150 | °C |
| $T_{OP}$ | Operating temperature range | -55 | 125 | °C |
| VESD | ESD voltage (Human Body Model, MIL-STD 883) | | 2000 | V |

## Electrostatic Discharge (ESD) Precautions

When handling this *UTSi®* device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

## Latch-Up Avoidance

Unlike conventional CMOS devices, *UTSi®* CMOS devices are immune to latch-up.

## Device Functional Considerations

The *PE83512* divides an input signal, up to a frequency of 1500 MHz, by a factor of four thereby producing an output frequency at one fourth the input frequency. To work properly at higher frequency, the input and output signals (pins 2 , 7 & optional 5) must be AC coupled via an external capacitor, as shown in the test circuit in Figure 4. The input may be DC coupled for low frequency operation with care taken to remain within the specified DC input range for the device.

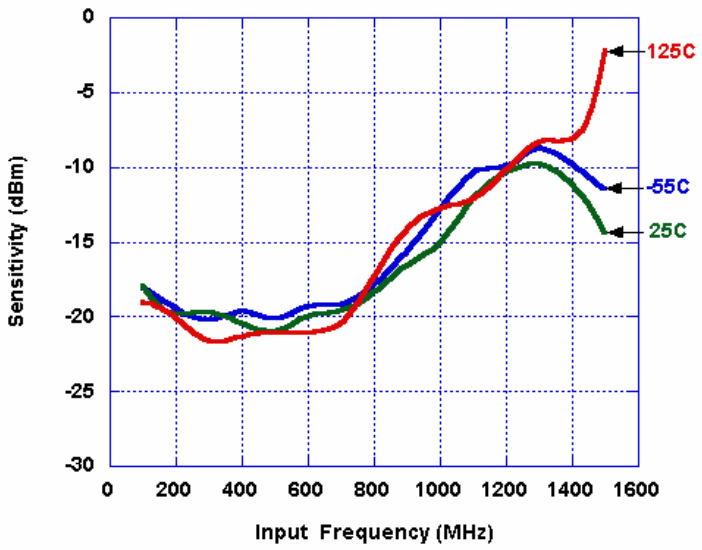
The ground pattern on the board should be made as wide as possible to minimize ground impedance. See Figure 7 for a layout example.

## OUTB Control

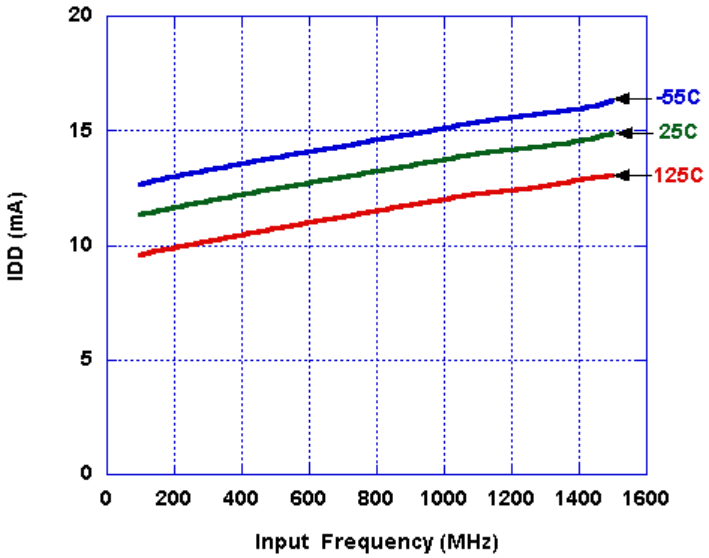
Pin 6 controls weather OUTB is enabled or disabled. Pin 6 has an internal pull-up resistor. With no connection (floating), OUTB is disabled. By grounding pin 6, OUTB is enabled. By enabling OUTB, this part will use roughly 5 mA more current.

## Typical Performance Data: $V_{DD}$ = 3.0V

### Figure 4. Input Sensitivity




### Figure 5. Device Current (OUTB Enabled)




### Figure 6. Output Power (OUT or OUTB)

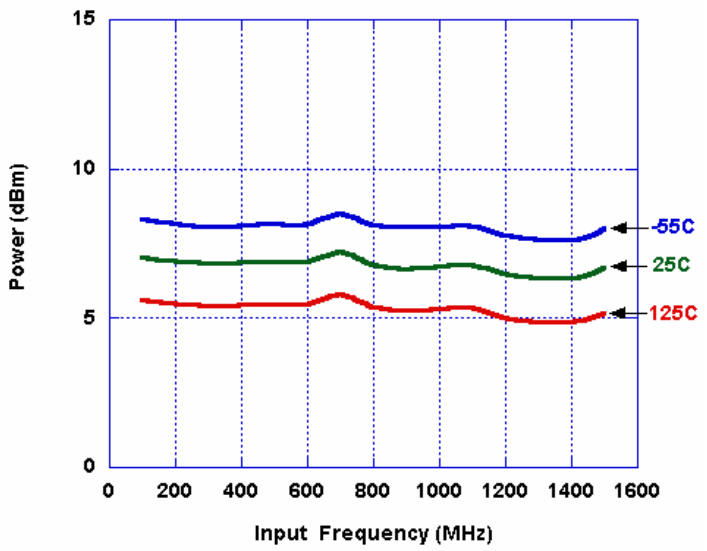


**Figure 7. Evaluation Board Schematic Diagram**

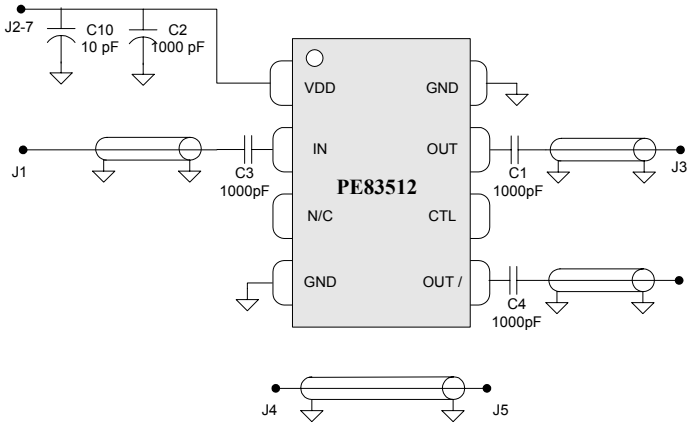
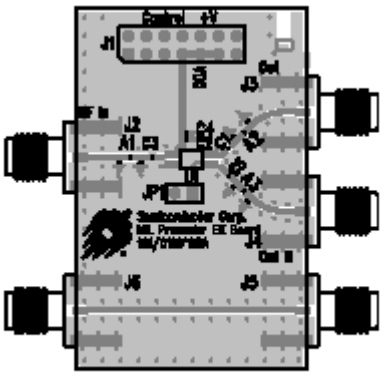



**Figure 8. Evaluation Board Layout**



## Evaluation Kit Operation

The *PE83512* EK board was designed to ease customer evaluation of Peregrine's high performance Military Grade divide-by-4 Prescaler. On this board, the device input (pin 2) is connected via J1 and a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. It is important to note that the value of this capacitance will impact the performance of the device. A value of 1000 pF was found to be optimal for this board layout; other applications may require a different value.

The device output (pin 7) is connected to connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. Note that this capacitor must be chosen to have low impedance at the desired output frequency the device. The value of 1000pF was chosen to provide a wide operating range for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.007", dielectric thickness of 0.028", metal thickness of 0.0014" and $\varepsilon_r$ of 4.4. Note that the predominate mode for these transmission lines is coplanar waveguide.

J2 provides DC power to the device. Starting from the lower left pin, the second pin to the right (J2-3) is connected to the device VDD pin (1). Two decoupling capacitors (10pF, 1000pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

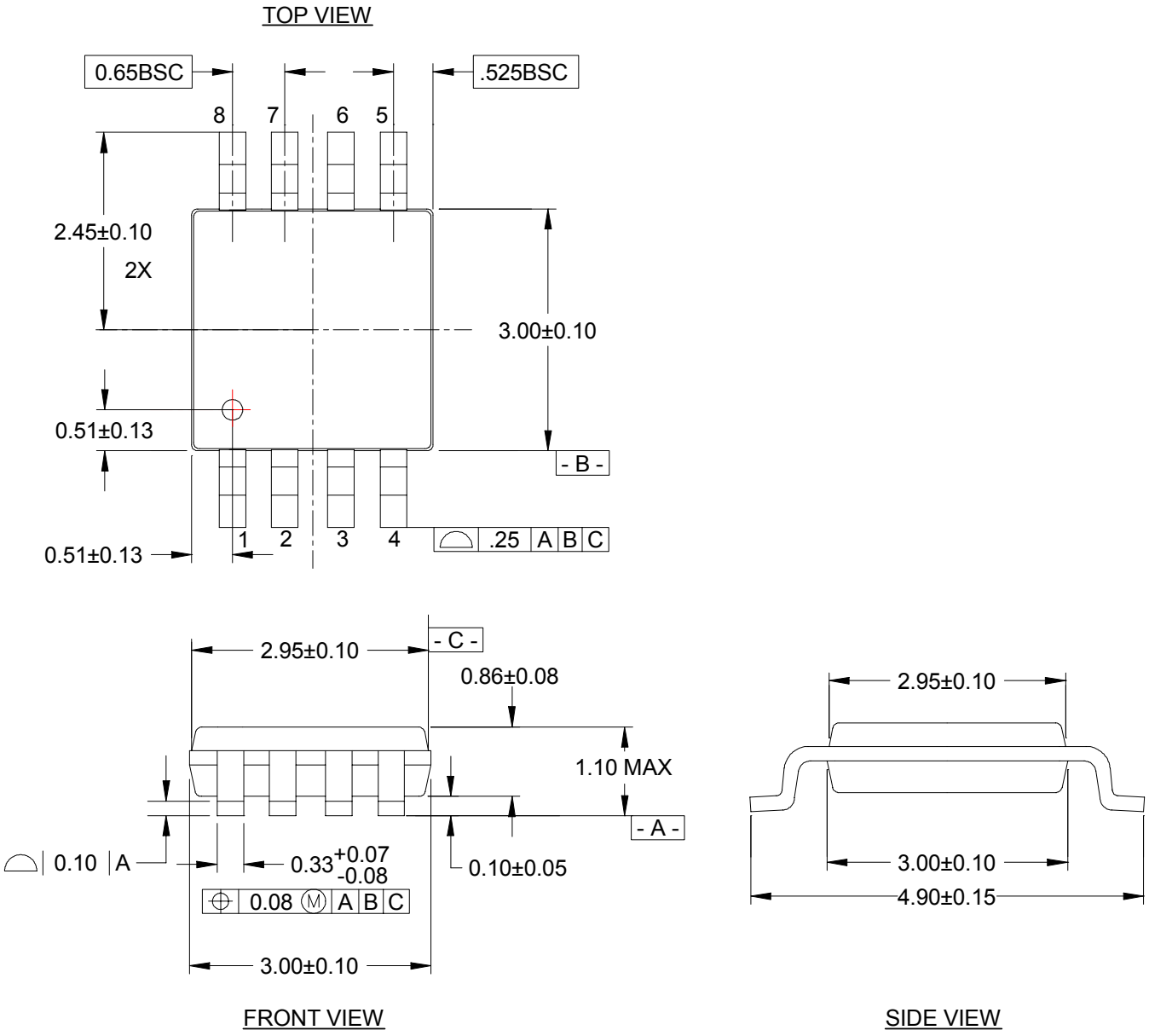
## Applications Support

If you have a problem with your evaluation kit or if you have applications questions call (858) 455-0660 and ask for applications support. You may also contact us by fax or e-mail:

**Fax:** (858) 455-0770
**E-Mail:** help@peregrine-semi.com

## Figure 9. Package Drawing

8 Lead Plastic MSOP




## Table 4. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|---|---|---|---|---|
| 83512-01 | PE83512 | PE83512-08MSOP-50A | 8-lead MSOP | 50 units / Tube |
| 83512-02 | PE83512 | PE83512-08MSOP-2000C | 8-lead MSOP | 2000 units / T&R |
| 83512-00 | PE83512-EK | PE83512-08MSOP-EK | Evaluation Kit | 1 / Box |

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# Data Sheet Identification

### *Advance Information*

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### *Product Specification*

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).