DATA SHEET

PCK2022RA

CK00 (100/133 MHz) spread spectrum differential system clock generator

Product data
2003 Jul 31

Supersedes data of 2001 Jun 12

Philips
Semiconductors

PHILIPS

FEATURES

- 3.3 V operation
- Eight differential CPU clock pairs
- One IO clock at 33 MHz and 66 MHz
- Two 48 MHz clocks at 3.3 V
- One 14.318 MHz reference clock
- Power management control pins
- Host clock jitter less than 200 ps cycle-to-cycle
- Host clock skew less than 150 ps pin-to-pin
- Spread Spectrum capability
- Optimized frequency and spread spectrum performance

DESCRIPTION

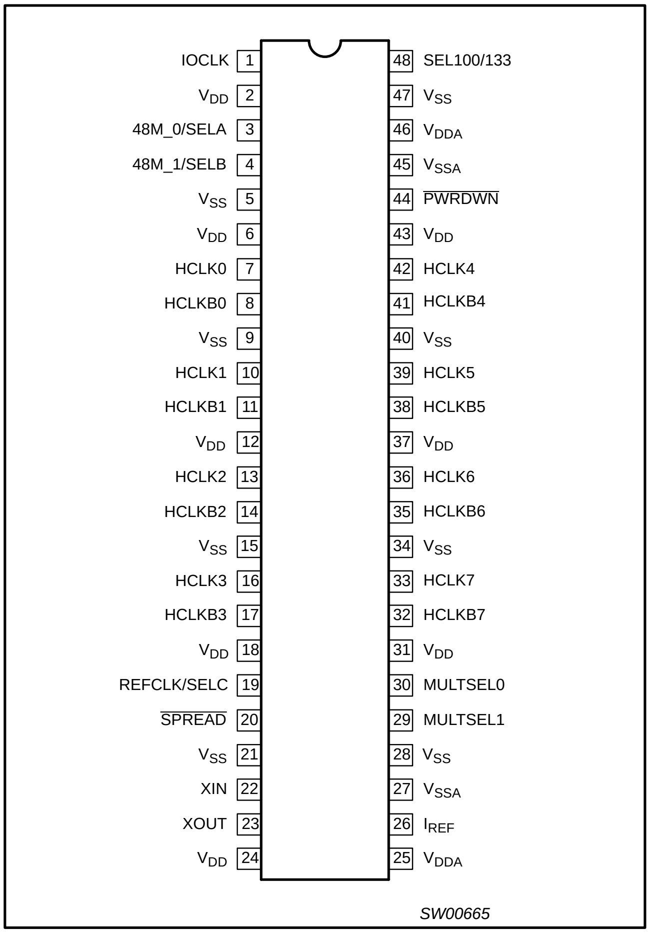
This part replaces PCK2022R with improved frequency and spread spectrum performance.

The PCK2022RA is a clock synthesizer/driver for a Pentium III™ and other similar processors.

The PCK2022RA has eight differential pair CPU current source outputs, one 33/66 MHz output which is configurable on power-up, two 48 MHz clocks which can be disabled on power-up, and one 3.3 V reference clock at 14.318 MHz which can also be disabled on power-up. All clock outputs meet Intel's drive strength, rise/fall times, jitter, accuracy, and skew requirements.

The part possesses a dedicated power-down input pin for power management control. This input is synchronized on chip, and ensures glitch-free output transitions. In addition, the part can be configured to disable the 48 MHz outputs for lower power operation and an increase in the performance of the functioning outputs. The IOCLK and REFCLK can also be disabled for the highest performance of the Host outputs.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-Pin Plastic TSSOP	0 to +70 °C	PCK2022RADGG	SOT362-1

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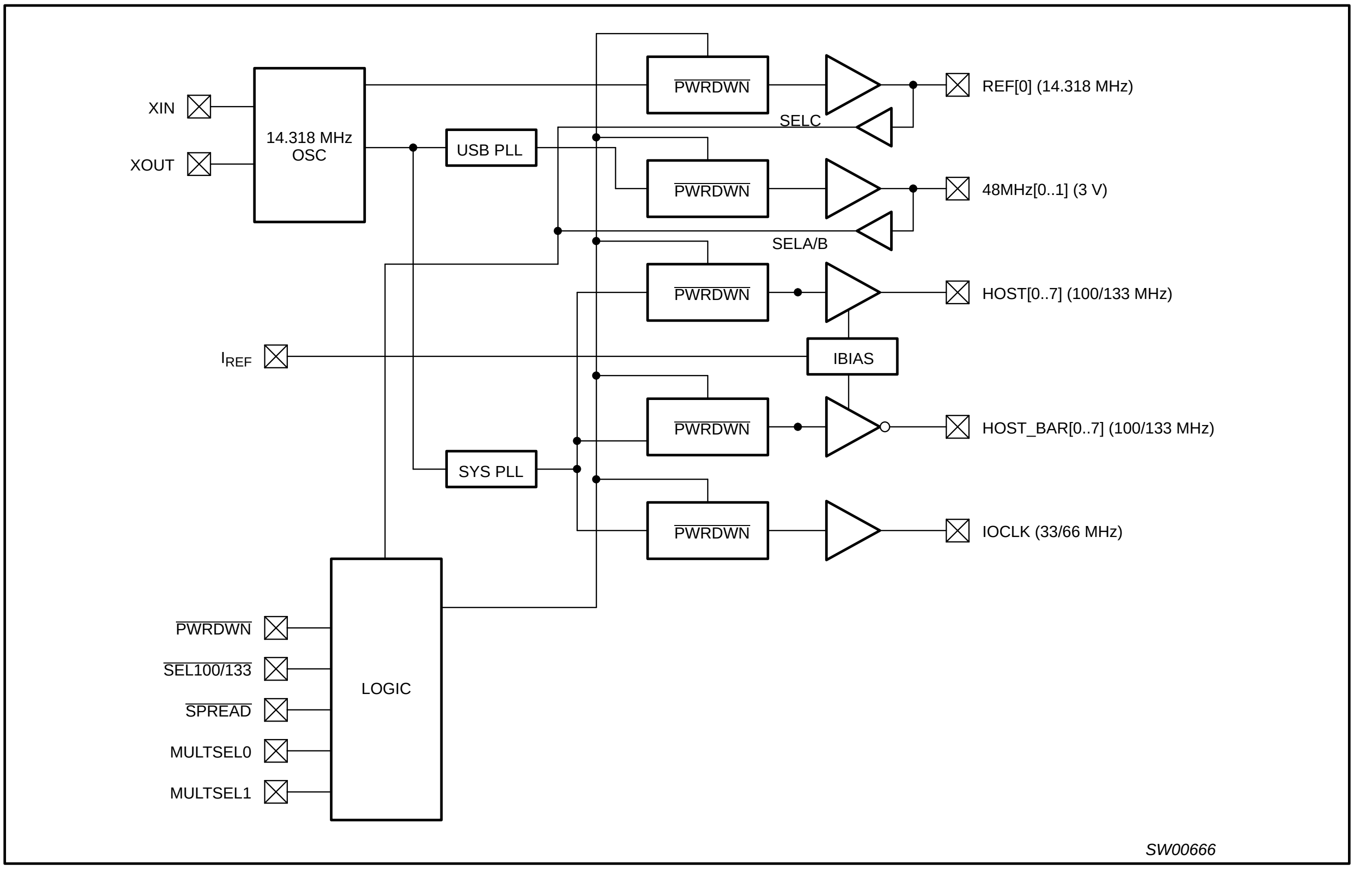
PIN DESCRIPTION

PIN(S)	SYMBOL	FUNCTION
1	IOCLK	Dual frequency pin which can operate at either 33 MHz or 66 MHz per the selection table.
3, 4	48M_0/SELA 48M_1/SELB	3.3 V fixed 48 MHz clock outputs. During power-up pins function as latched inputs that enable SELA and SELB prior to the pins being used for output of 3 V at 48 MHz. Part must be clocked to latch data in.
7, 8	HCLK0 HCLKB0	Host output pair 0
10, 11	HCLK1 HCLKB1	Host output pair 1
13, 14	HCLK2 HCLKB2	Host output pair 2
16, 17	HCLK3 HCLKB3	Host output pair 3
42, 21	HCLK4 HCLKB4	Host output pair 4
39, 38	HCLK5 HCLKB5	Host output pair 5
36, 35	HCLK6 HCLKB6	Host output pair 6
33, 32	HCLK7 HCLKB7	Host output pair 7
19	REFCLK/SELC	3.3 V fixed 14.318 MHz output. During power-up, pin functions as a latched input that enables SELC prior to the pin being used for the clock output. Part must be clocked to latch data in.
20	$\overline{\text{SPREAD}}$	Enables spread spectrum mode when held LOW on differential host outputs and 33 MHz IOCLK clocks. Asserts LOW.
21	XIN	Crystal input
22	XOUT	Crystal output
26	I_{REF}	This pin controls the reference current for the host pairs. This pin requires a fixed precision resistor tied to ground in order to establish the correct current.
29, 30	MULTSEL0 MULTSEL1	Select input pin used to control the scaling of the HCLK and HCLKB output current.
44	$\overline{\text{PWRDWN}}$	Device enters power-down mode when held LOW. Asserts LOW.
48	SEL100/133	Select input pin for enabling 133 MHz or 100 MHz CPU outputs
2, 6, 12, 18, 24, 31, 37, 43	V_{DD3}	3.3 V power supply
5, 9, 15, 21, 28, 34, 40, 47	GND	Ground
25, 46	AV_{DD}	3.3 V power supply for analog circuits
27, 45	AGND	Ground for analog circuits

BLOCK DIAGRAM



FUNCTION TABLE

SEL100/133	SELA	SELB	SELC	HOST	48MHz	IOCLK	REFCLK
0	0	0	0	100 MHz	48 MHz	33.3 MHz	14.318 MHz
0	0	0	1	100 MHz	48 MHz	66.7 MHz	14.318 MHz
0	0	1	0	100 MHz	Hi-Z	33.3 MHz	14.318 MHz
0	0	1	1	100 MHz	Hi-Z	66.7 MHz	14.318 MHz
0	1	0	0	100 MHz	Hi-Z	LOW	LOW
0	1	0	1	100 MHz	48 MHz[1]	33.3 MHz	14.318 MHz
0	1	1	0	LOW	Hi-Z	Hi-Z	Hi-Z
0	1	1	1	100 MHz	48 MHz[1]	66.7 MHz	14.318 MHz
1	0	0	0	133 MHz	48 MHz	33.3 MHz	14.318 MHz
1	0	0	1	133 MHz	48 MHz	66.7 MHz	14.318 MHz
1	0	1	0	133 MHz	Hi-Z	33.3 MHz	14.318 MHz
1	0	1	1	133 MHz	Hi-Z	66.7 MHz	14.318 MHz
1	1	0	0	200 MHz	48 MHz	33.3 MHz	14.318 MHz
1	1	0	1	133 MHz	48 MHz[1]	33.3 MHz	14.318 MHz
1	1	1	0	TCLK/2	TCLK/4	TCLK/4	TCLK
1	1	1	1	133 MHz	48 MHz[1]	66.7 MHz	14.318 MHz

NOTE:
1. These frequencies are for debug, and thus can vary a small amount from the values listed at the vendor’s discretion.

Table 1. Host swing select functions

MULTSEL0	MULTSEL1	BOARD IMPEDANCE	I_{REF}	I_{OH}	V_{OH} @ IREF = 2.32 mA
0	0	60 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 5*I_{REF}$	0.71 V
0	0	50 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 5*I_{REF}$	0.59 V
0	1	60 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 6*I_{REF}$	0.85 V
0	1	50 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 6*I_{REF}$	0.71 V
1	0	60 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 4*I_{REF}$	0.56 V
1	0	50 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 4*I_{REF}$	0.47 V
1	1	60 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 7*I_{REF}$	0.99 V
1	1	50 Ω	R_{REF} = 475 1% I_{REF} = 2.32 mA	$I_{OH} = 7*I_{REF}$	0.82 V
0	0	30 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 5*I_{REF}$	0.75 V
0	0	25 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 5*I_{REF}$	0.62 V
0	1	30 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 6*I_{REF}$	0.90 V
0	1	25 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 6*I_{REF}$	0.75 V
1	0	30 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 4*I_{REF}$	0.60 V
1	0	25 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 4*I_{REF}$	0.50 V
1	1	30 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 7*I_{REF}$	1.05 V
1	1	25 Ω	R_{REF} = 221 1% I_{REF} = 5 mA	$I_{OH} = 7*I_{REF}$	0.84 V

NOTE:
The outputs are optimized for the configurations shown shaded.

	CONDITIONS	CONFIGURATION	LOAD	MIN.	MAX.
I_{OUT}	V_{DD} = 3.3 V	All combinations; see Table 1 above	Nominal test load for given configuration	-7% of I_{OH} see Table 1 above	+7% of I_{OH} see Table 1 above
I_{OUT}	V_{DD} = 3.3 V ±5%	All combinations; see Table 1 above	Nominal test load for given configuration	-12% of I_{OH} see Table 1 above	+12% of I_{OH} see Table 1 above

POWER-DOWN MODE

PWRDWN	HCLK/HCLKB	IOCLK	48MHz	REFCLK
Asserts LOW 0 = Active	Host = $2*I_{REF}$ Host_bar = undriven	LOW	LOW	LOW

NOTE:
The differential outputs should have a voltage forced across them when power-down is asserted.

SPREAD SPECTRUM FUNCTION

SPREAD #	FUNCTION	48 MHz PLL REFCLK
1	Host/IOCLK No Spread	No Spread
0	Host/IOCLK Down spread -0.5%	No Spread

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3 V supply		-0.5	4.6	V
I_{IK}	DC input diode current	$V_I < 0$	—	-50	mA
V_I	DC input voltage	Note 2	-0.5	V_{DD}	V
I_{OK}	DC output diode current	$V_O > V_{DD}$ or $V_O < 0$	—	±50	mA
V_O	DC output voltage	Note 2	-0.5	V_{DD}+0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{DD}	—	±50	mA
T_{stg}	Storage temperature range		-65	+150	°C
P_{tot}	Power dissipation per package plastic medium-shrink (SSOP)	For temperature range -40°C to +125°C; above +55°C derate linearly with 11.3 mW/K	—	850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated under “recommended operating condition” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage rating may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3 V supply voltage[1]		3.135	3.465	V
AV_{DD}	DC 3.3 V analog supply voltage[1]		3.135	3.465	V
C_L	Capacitive load on: IOCLK 48 MHz clock REF	 Must meet IOCLK 2.1 requirements 1 device load 1 device load	 10 10 10	 30 20 20	 pF pF pF
f_{ref}	Reference frequency, oscillator normal value		14.31818	14.31818	MHz
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

NOTE:
1. Supply voltage needs to be less than 20 mV before powering on to ensure proper PLL start-up.

POWER MANAGEMENT

CONDITION	MAXIMUM 3.3 V SUPPLY CONSUMPTION MAXIMUM DISCRETE CAPACITANCE LOADS V_{DDL} = 3.465 V ALL STATIC INPUTS = V_{DD3} OR V_{SS}
Power-down mode (PWRDWN = 0)	60 mA
Full active 100/133 MHz	250 mA

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0 to +70 °C

SYMBOL	PARAMETER	CONDITIONS			LIMITS			UNIT
		V_{DD} (V)	OTHER		MIN	TYP	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465			2.0	—	V_{DD}+0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465			V_{SS}-0.3	—	0.8	V
V_{OH3}	3.3 V output HIGH voltage REF, 48M	3.135 to 3.465	I_{OH} = -1 mA		2.0	—	—	V
V_{OL3}	3.3 V output LOW voltage REF, 48M	3.135 to 3.465	I_{OH} = 1 mA		—	—	0.4	V
V_{OHP}	3.3 V output HIGH voltage IOCLK	3.135 to 3.465	I_{OH} = -1 mA		2.4	—	—	V
V_{OLP}	3.3 V output LOW voltage IOCLK	3.135 to 3.465	I_{OH} = 1 mA		—	—	0.55	V
I_{OH}	HIGH-level output current IOCLK	3.135	V_{OUT} = 1.0 V	Type 5 12 - 55 Ω	-33	—	—	mA
		3.465	V_{OUT} = 3.135 V		—	—	-33	mA
I_{OH}	HIGH-level output current 48 MHz, REF	3.135	V_{OUT} = 1.0 V	Type 3 20 - 60 Ω	-29	—	—	mA
		3.465	V_{OUT} = 3.135 V		—	—	-23	mA
I_{OH}	HIGH-level output current HOST/HOST_BAR	3.135 to 3.465	0.66 V	Type X1	11	—	—	mA
			0.76 V		—	—	12.7	mA
I_{OL}	LOW-level output current IOCLK	3.135	V_{OUT} = 1.95 V	Type 5 12 - 55 Ω	30	—	—	mA
		3.465	V_{OUT} = 0.4 V		—	—	38	mA
I_{OL}	LOW-level output current 48 MHz, REF	3.135	V_{OUT} = 1.95 V	Type 3 20 - 60 Ω	29	—	—	mA
		3.465	V_{OUT} = 0.4 V		—	—	27	mA
V_{OL}	LOW-level output voltage HOST/HOST_BAR	V_{SS} = 0 V	R_S = 33.2 Ω R_P = 49.9 Ω	Type X1	—	—	0.05	V
$\pm I_I$	Input leakage current	3.465	$0 < V_{IN} < V_{DD3}$		-50	—	50	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{DD} or GND	I_O = 0	—	—	10	µA
C_{in}	Input pin capacitance				—	—	5	pF
C_{out}	Output pin capacitance				—	—	6	pF
C_{xtal}	Crystal input capacitance				13.5	—	22.5	pF

AC ELECTRICAL CHARACTERISTICS

V_{DD3} = 3.3 V ±5%; $f_{crystal}$ = 14.31818 MHz

Host clock outputs

T_{amb} = 0 to +70 °C; see Figure 1 for waveforms and Figure 6 for test setup.

SYMBOL	PARAMETER	LIMITS				UNITS	NOTES
		133 MHz MODE		100 MHz MODE			
		MIN	MAX	MIN	MAX		
t_{PKP}	HOST CLK average period	7.5	7.65	10.0	10.2	ns	11, 14, 20
Abs Min Period	Absolute minimum host clock period	7.35	N/A	9.85	N/A	ns	11, 14, 20
t_{RISE}	HOST CLK rise time	175	700	175	700	ns	11, 15, 20
t_{FALL}	HOST CLK fall time	175	700	175	700	ps	11, 15, 20
t_{JITTER}	HOST_CLK cycle-to-cycle jitter	—	150	—	150	ps	11, 12, 14, 20
DUTY CYCLE	Output duty cycle	45	55	45	55	%	11, 14, 20
t_{SKEW}	HOST CLK pin-to-pin skew	—	150	—	150	ps	11, 14, 20
Rise/Fall Matching	Rise and Fall time matching	—	20%	—	20%		11, 16, 20
$V_{crossover}$		40% V_{OH}	55% V_{OH}	40% V_{OH}	55% V_{OH}	V	11, 14, 20

REFER TO NOTES ON PAGE 9.

IOCLK outputs

T_{amb} = 0 to +70 °C

SYMBOL	PARAMETER	LIMITS				UNITS	NOTES
		33 MHz MODE		66 MHz MODE			
		MIN	MAX	MIN	MAX		
t_{PKP}	IOCLK period	30.0	N/A	15.0	N/A	ns	2, 3, 9, 20
t_{PKH}	IOCLK HIGH time	12.0	N/A	6.0	N/A	ns	5, 10, 20
t_{PKL}	IOCLK LOW time	12.0	N/A	6.0	N/A	ns	6, 10, 20
t_{RISE}	IOCLK rise time	0.5	2.0	0.5	2.0	ns	8, 20
t_{FALL}	IOCLK fall time	0.5	2.0	0.5	2.0	ns	8, 20
t_{JITTER}	Cycle-to-cycle jitter	—	200	—	200	ps	18, 20
DUTY CYCLE	Output duty cycle	45	55	45	55	%	18, 20

REFER TO NOTES ON PAGE 9.

USB clock output, 48MHz

T_{amb} = 0 to +70 °C; lump capacitance test load = 20 pF

SYMBOL	PARAMETER	LIMITS		UNITS	NOTES
		48 MHz MODE			
		MIN	MAX		
f	Frequency, actual	48.08		MHz	4
f_D	Deviation from 48 MHz	+167		ppm	4
t_{HKL}	3V48MHZCLK LOW time	5.05	N/A	ns	20
t_{RISE}	3V48MHZCLK rise time	1.0	4.0	ns	8, 20
t_{FALL}	3V48MHZCLK fall time	1.0	4.0	ns	8, 20
t_{JITTER}	Cycle-to-cycle jitter	—	250	ps	18, 20
DUTY CYCLE	Output duty cycle	45	55	%	18, 20

REFER TO NOTES ON PAGE 9.

REF clock output

T_{amb} = 0 to +70 °C; lump capacitance test load = 20 pF

SYMBOL	PARAMETER	LIMITS 48 MHz MODE MIN	MAX	UNITS	NOTES
f	Frequency, actual	14.318		MHz	17, 20
t_{HKL}	REFCLK LOW time	30	37	ns	20
t_{HKH}	REFCLK HIGH time	30	37	ns	20
t_{JITTER}	Cycle-to-cycle jitter	—	300	ps	18, 20
DUTY CYCLE	Output duty cycle	45	55	%	18, 20

REFER TO NOTES ON PAGE 9.

All outputs

T_{amb} = 0 to +70 °C

SYMBOL	PARAMETER	LIMITS 133 MHz MODE MIN	MAX	100 MHz MODE MIN	MAX	UNITS	NOTES
t_{PZL}, t_{PZH}	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	ns	20
t_{PZL}, t_{PZH}	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	ns	20
t_{STABLE}	All clock stabilization from power-up	—	3	—	3	ms	7, 20

REFER TO NOTES ON PAGE 9.

Group offset limits

GROUP	OFFSET	MEASUREMENT LOADS (LUMPED)	MEASUREMENT POINTS	NOTES
Host to IOCLK	1.5 - 3.5 ns Host leads	IOCLK @ 30 pF	Host @ Cross point IOCLK @ 1.5 V	19, 20

NOTES TO THE AC TABLES:

1. Output drivers must have monotonic rise/fall times through the specified V_{OL}/V_{OH} levels.
2. Period, jitter, offset, and skew measured on rising edge at 1.5 V for 3.3 V clocks.
3. The IOCLK clock is the Host clock divided by 4 in 33 MHz mode and divided by 2 in 66 MHz mode at Host = 133 MHz. IOCLK clock is the Host clock divided by 3 in 33 MHz and divided by 2/3 in 66 MHz mode at Host = 100 MHz.
4. Frequency accuracy of 48 MHz must be +167 ppm to match USB default.
5. t_{HKH} is measured at 2.4 V for 3.3 V outputs, as shown in Figure 7.
6. t_{HKL} is measured at 0.4 V for all outputs as shown in Figure 7.
7. the time is specified from when V_{DDQ} achieves its normal operating level (typical condition V_{DDQ} = 3.3 V) until the frequency output is stable and operating within specification.
8. t_{RISE} and t_{FALL} are measured as a transition through the threshold region V_{OL} = 0.4 V and V_{OH} = 2.4 V (1 mA) JEDEC specification.
9. The average period over any 1 μs period of time must be greater than the minimum specified period.
10. Calculated at minimum edge rate (1 V/ns) to guarantee 45-55% duty cycle. Pulse width is required to be wider at faster edge rate to ensure duty specification is met.
11. Test load is R_S = 33.2 Ω, R_P = 49.9 Ω.
12. Must be guaranteed in a realistic system environment.
13. Configured for V_{OH} = 0.71 V in a 50 Ω environment.
14. Measured at crossing points.
15. Measured at 20% to 80%.
16. Determined as a fraction of $2*(t_{RP} - t_{RN}) / (t_{RP} + t_{RN})$, where t_{RP} is a rising edge, and t_{RN} is an intersecting falling edge.
17. Frequency generated by crystal oscillator
18. Voltage measure point (V_M = 1.5 V). V_{DD} = 3.3 V.
19. All offsets are to be measured at rising edges.
20. Parameters are guaranteed by design.

AC WAVEFORMS

V_M = 1.25 V @ V_{DDL} and 1.5 V @ V_{DD3}
$V_X = V_{OL}$ + 0.3 V
$V_Y = V_{OH}$ - 0.3 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

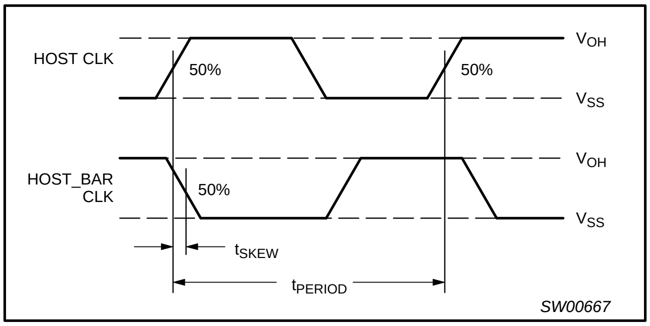


Figure 1. HOST CLOCK

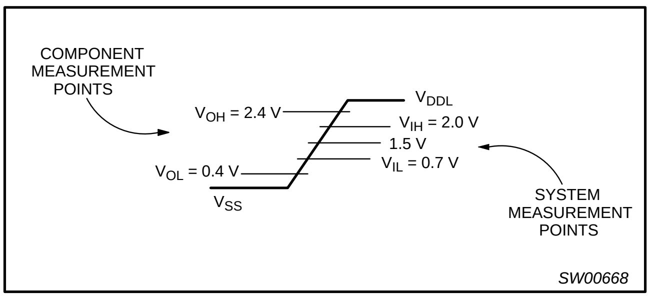


Figure 2. 3.3 V clock waveforms

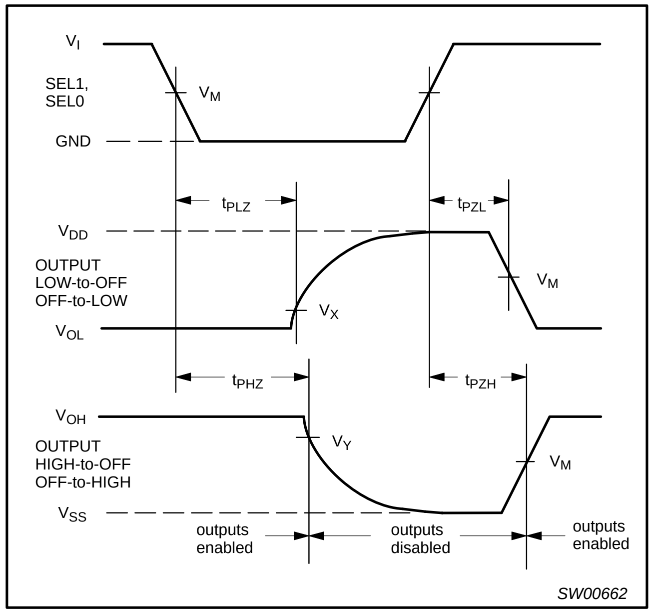
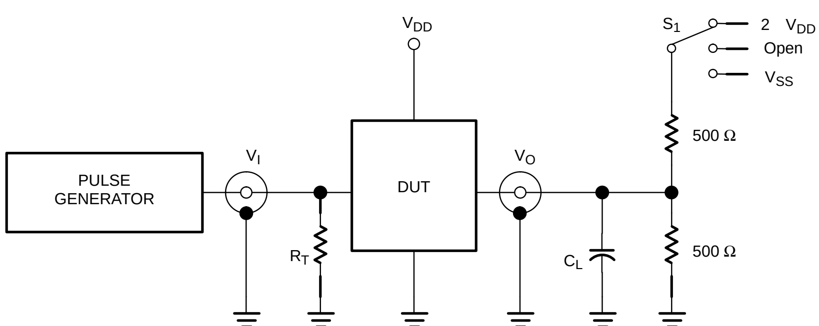


Figure 3. State enable and disable times



TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 V_{DD}
t_{PHZ}/t_{PZH}	V_{SS}

$V_{DD} = V_{DDL}$ or V_{DD3}, depending on the output.

Figure 4. Load circuitry for switching times

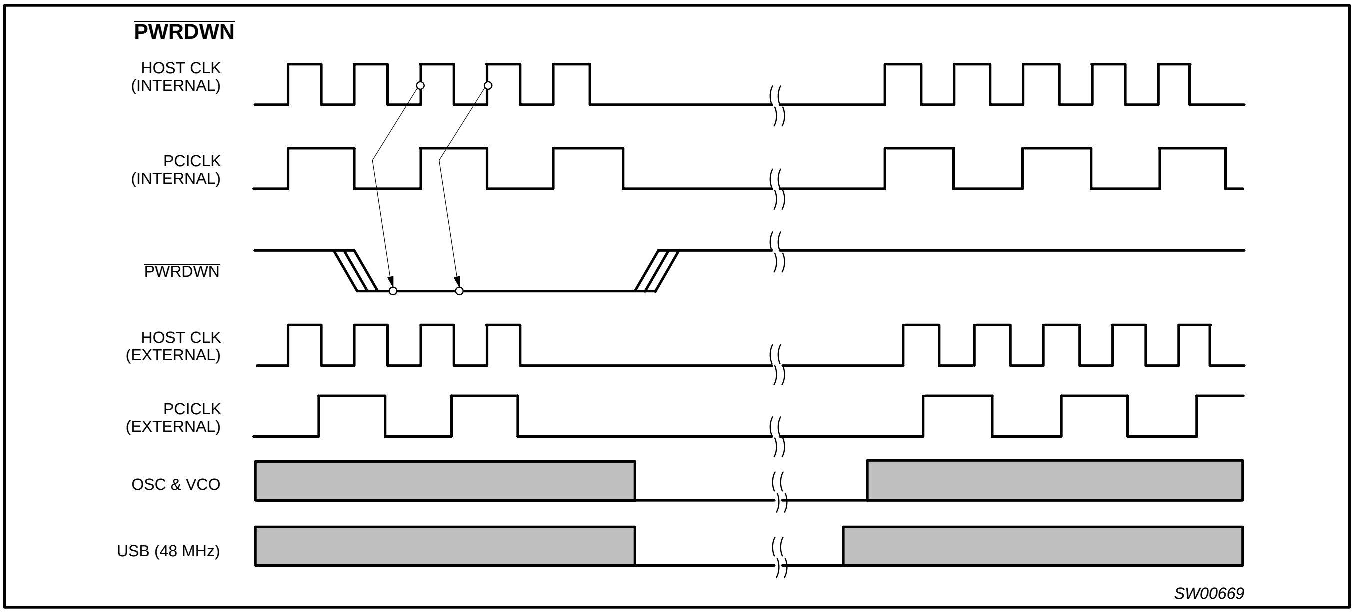


Figure 5. Power management

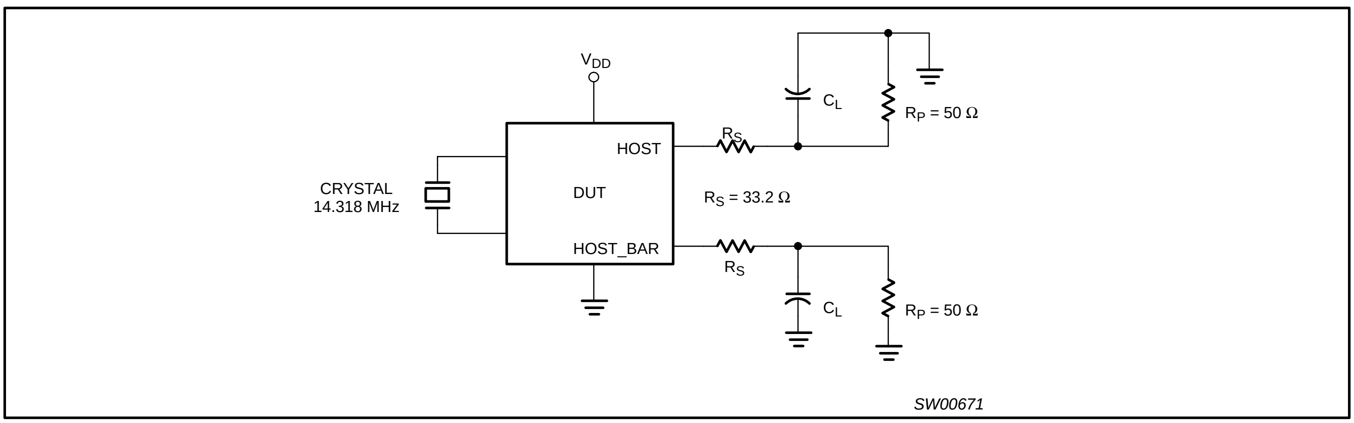


Figure 6. HOST CLOCK measurements

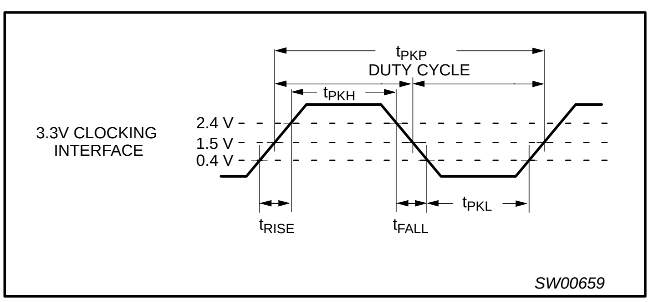
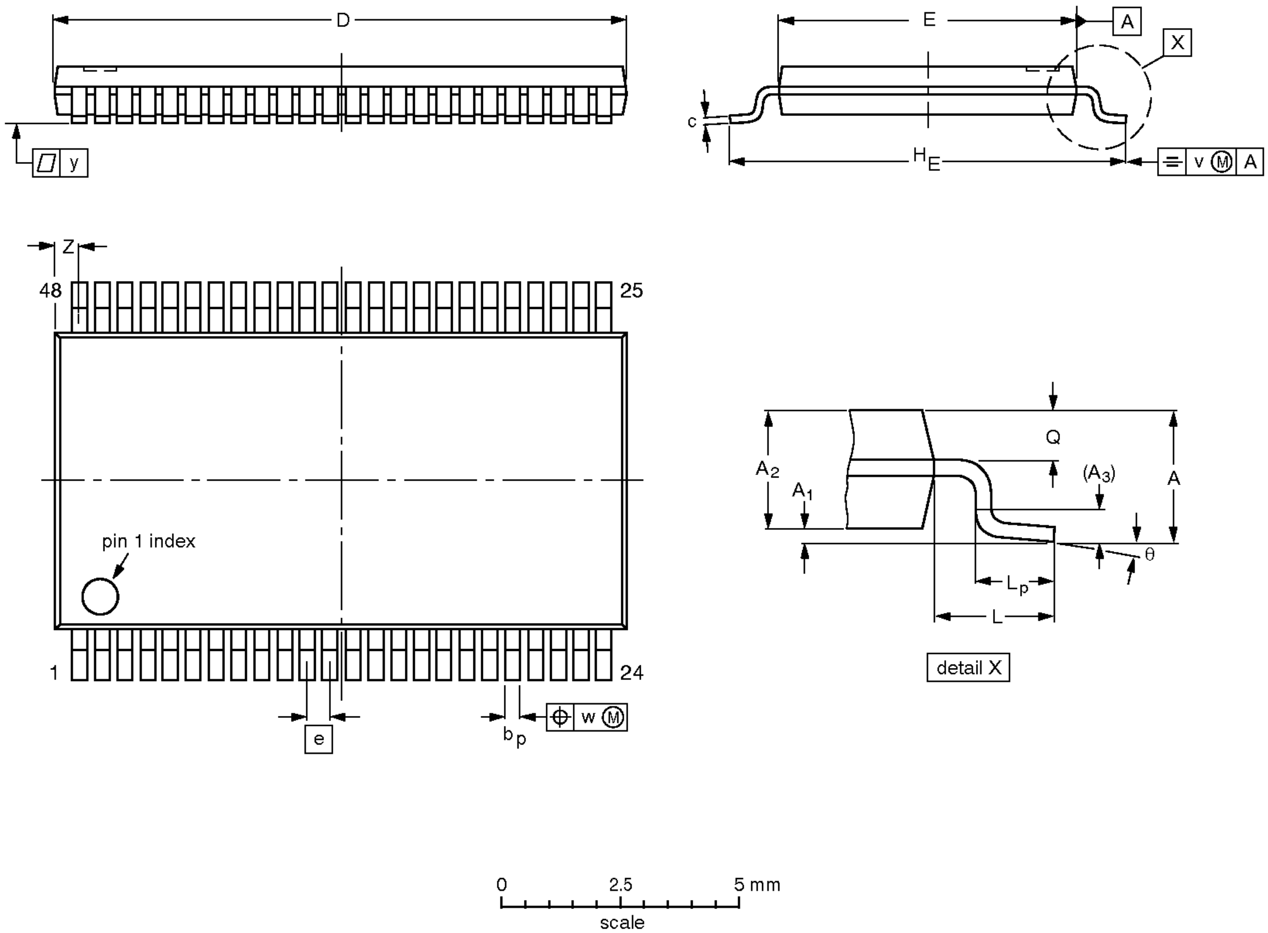


Figure 7. 3.3 V clock waveforms

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_2	20030731	**Product data (9397 750 11761); ECN 853-2257 30052 dated 18 June 2003. Supersedes data of 2002 June 12 (9397 750 08473).** Modifications: • Minor changes or corrections to existing product specifications.
_1	20020612	Product data (9397 750 08473); ECN 853-2257 26484 of 12 June 2002.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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