



# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies to 175 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

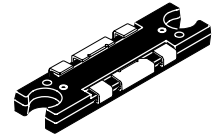
- Specified Performance @ 175 MHz, 12.5 Volts
  - Output Power — 50 Watts
  - Power Gain — 12 dB
  - Efficiency — 50%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 175 MHz, 2 dB Overdrive

### Features

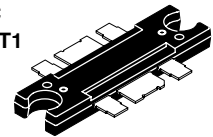
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135-175 MHz
- Broadband Demonstration Amplifier Information Available Upon Request
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

**MRF1550NT1**  
**MRF1550FNT1**

**175 MHz, 50 W, 12.5 V**  
**LATERAL N-CHANNEL**  
**BROADBAND**  
**RF POWER MOSFETs**



**CASE 1264-09, STYLE 1**  
**TO-272-6 WRAP**  
**PLASTIC**  
**MRF1550NT1**



**CASE 1264A-02, STYLE 1**  
**TO-272-6**  
**PLASTIC**  
**MRF1550FNT1**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-0.5, +40	Vdc
Gate-Source Voltage	V <sub>GS</sub>	±20	Vdc
Drain Current — Continuous	I <sub>D</sub>	12	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C (1) Derate above 25°C	P <sub>D</sub>	165 0.50	W W/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Junction Temperature	T <sub>J</sub>	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value(2)	Unit
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	0.75	°C/W

**Table 3. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

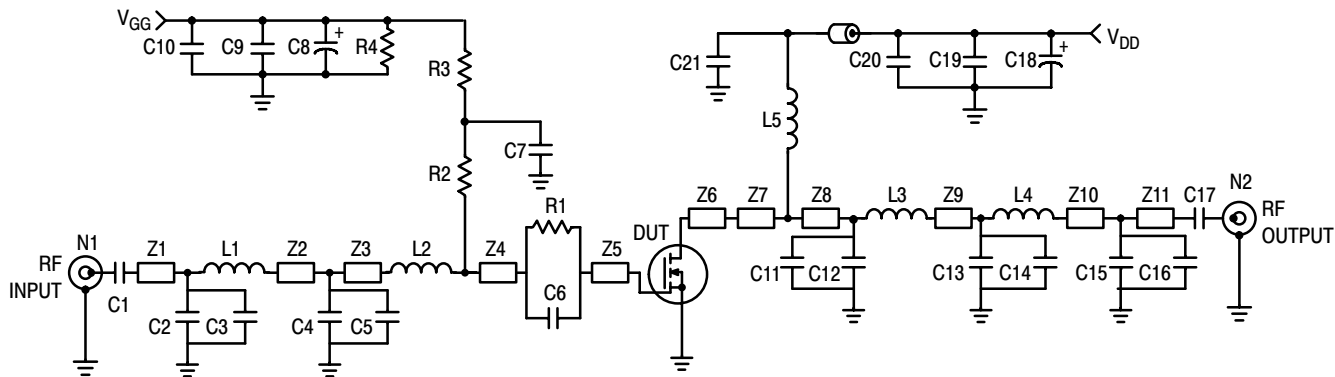
1. Calculated based on the formula  $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

2. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Zero Gate Voltage Drain Current ( $V_{DS} = 60\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}_{dc}$
Gate-Source Leakage Current ( $V_{GS} = 10\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	0.5	$\mu\text{A}_{dc}$
<b>On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 12.5\text{ Vdc}$ , $I_D = 800\ \mu\text{A}$ )	$V_{GS(th)}$	1	—	3	Vdc
Drain-Source On-Voltage ( $V_{GS} = 5\text{ Vdc}$ , $I_D = 1.2\text{ A}$ )	$R_{DS(on)}$	—	—	0.5	$\Omega$
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4.0\text{ A}_{dc}$ )	$V_{DS(on)}$	—	—	1	Vdc
<b>Dynamic Characteristics</b>					
Input Capacitance (Includes Input Matching Capacitance) ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ )	$C_{iss}$	—	—	500	pF
Output Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ )	$C_{oss}$	—	—	250	pF
Reverse Transfer Capacitance ( $V_{DS} = 12.5\text{ Vdc}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$ )	$C_{rss}$	—	—	35	pF
<b>RF Characteristics</b> (In Freescale Test Fixture)					
Common-Source Amplifier Power Gain ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 50\text{ Watts}$ , $I_{DQ} = 500\text{ mA}$ ) $f = 175\text{ MHz}$	$G_{ps}$	—	14.5	—	dB
Drain Efficiency ( $V_{DD} = 12.5\text{ Vdc}$ , $P_{out} = 50\text{ Watts}$ , $I_{DQ} = 500\text{ mA}$ ) $f = 175\text{ MHz}$	$\eta$	—	55	—	%



B1	Ferroxcube #VK200	L4	1 Turn, #26 AWG, 0.240" ID
C1	180 pF, 100 mil Chip Capacitor	L5	3 Turn, #24 AWG, 0.180" ID
C2	10 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C3	33 pF, 100 mil Chip Capacitor	R1	5.1 $\Omega$ , 1/4 W Chip Resistor
C4, C16	24 pF, 100 mil Chip Capacitors	R2	39 $\Omega$ Chip Resistor (0805)
C5	160 pF, 100 mil Chip Capacitor	R3	1 k $\Omega$ , 1/8 W Chip Resistor
C6	240 pF, 100 mil Chip Capacitor	R4	33 k $\Omega$ , 1/4 W Chip Resistor
C7, C17	300 pF, 100 mil Chip Capacitors	Z1	1.000" x 0.080" Microstrip
C8, C18	10 $\mu$ F, 50 V Electrolytic Capacitors	Z2	0.400" x 0.080" Microstrip
C9, C19	0.1 $\mu$ F, 100 mil Chip Capacitors	Z3	0.200" x 0.080" Microstrip
C10	470 pF, 100 mil Chip Capacitor	Z4	0.200" x 0.080" Microstrip
C11, C12	200 pF, 100 mil Chip Capacitors	Z5, Z6	0.100" x 0.223" Microstrip
C13	22 pF, 100 mil Chip Capacitor	Z7	0.160" x 0.080" Microstrip
C14	30 pF, 100 mil Chip Capacitor	Z8	0.260" x 0.080" Microstrip
C15	6.8 pF, 100 mil Chip Capacitor	Z9	0.280" x 0.080" Microstrip
C20	1,000 pF, 100 mil Chip Capacitor	Z10	0.270" x 0.080" Microstrip
L1	18.5 nH, Coilcraft #A05T	Z11	0.730" x 0.080" Microstrip
L2	5 nH, Coilcraft #A02T	Board	Glass Teflon <sup>®</sup> , 31 mils
L3	1 Turn, #24 AWG, 0.250" ID		

Figure 1. 135 - 175 MHz Broadband Test Circuit

### TYPICAL CHARACTERISTICS

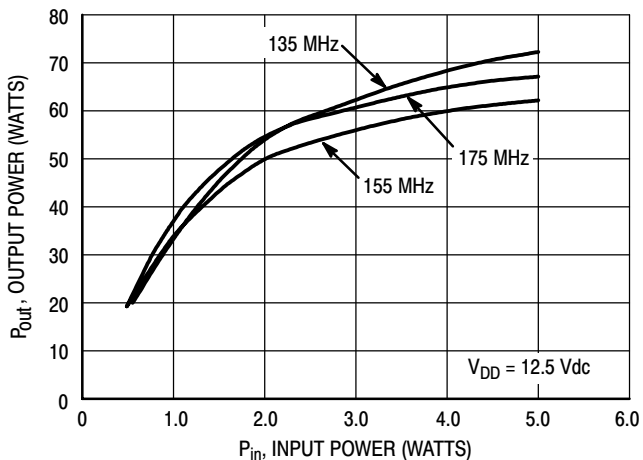


Figure 2. Output Power versus Input Power

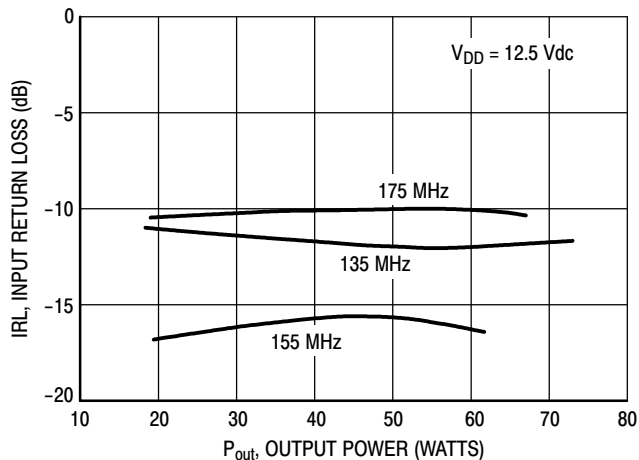


Figure 3. Input Return Loss versus Output Power

## TYPICAL CHARACTERISTICS

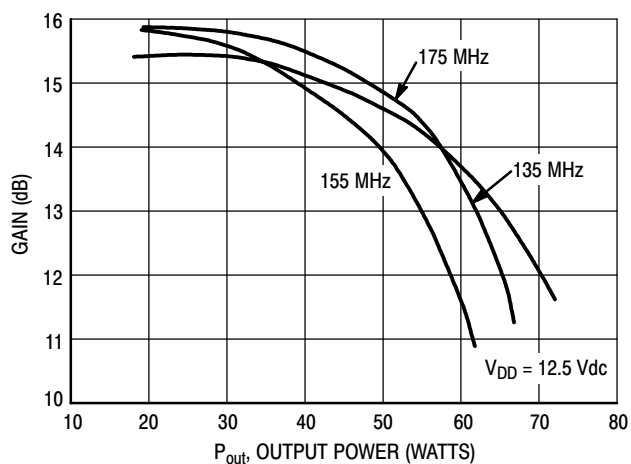


Figure 4. Gain versus Output Power

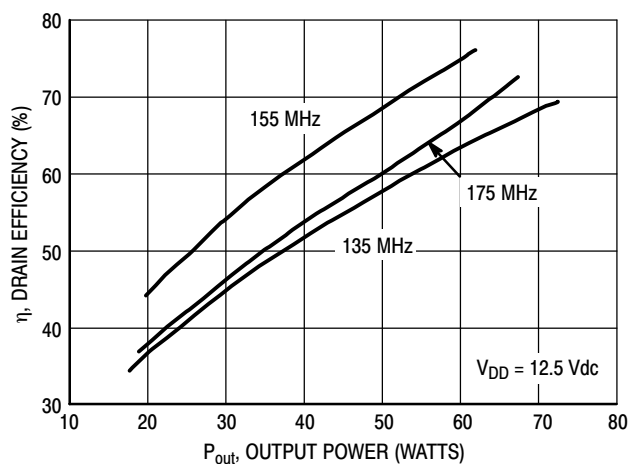


Figure 5. Drain Efficiency versus Output Power

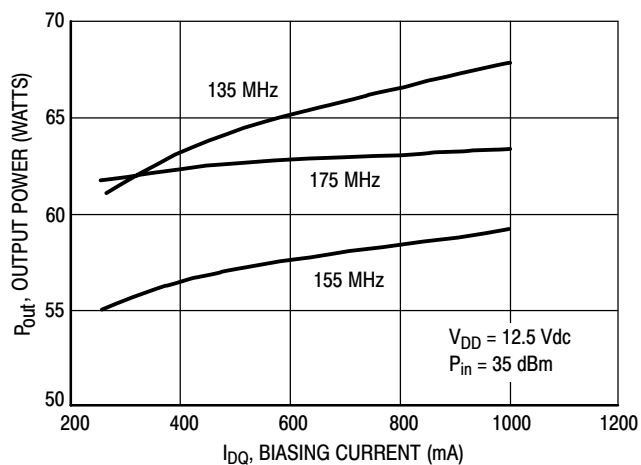


Figure 6. Output Power versus Biasing Current

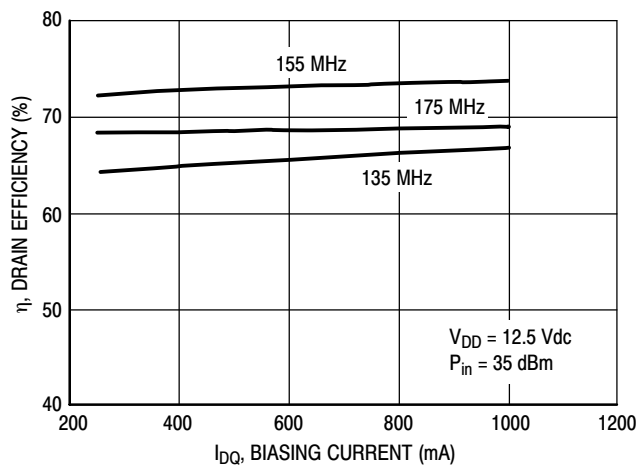


Figure 7. Drain Efficiency versus Biasing Current

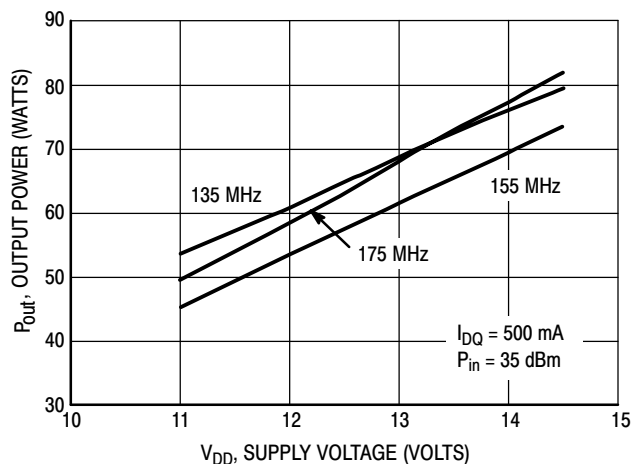


Figure 8. Output Power versus Supply Voltage

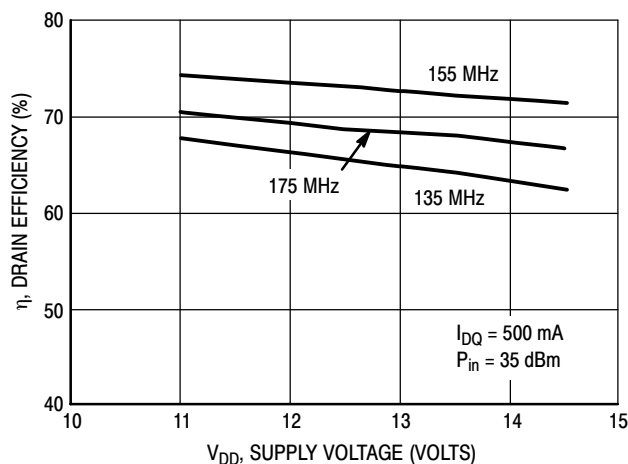
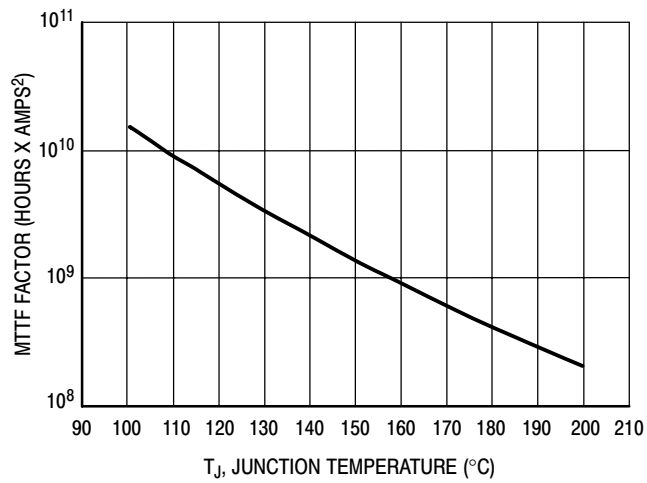


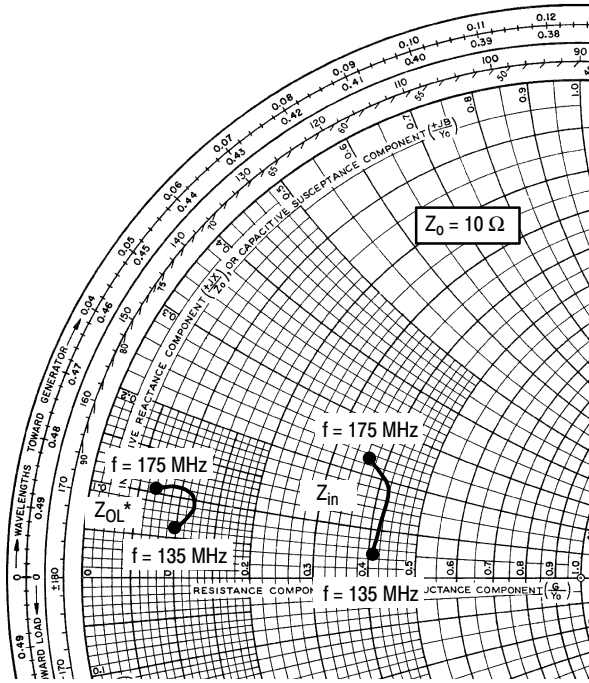
Figure 9. Drain Efficiency versus Supply Voltage

## TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I<sub>D</sub><sup>2</sup> for MTTF in a particular application.

**Figure 10. MTTF Factor versus Junction Temperature**



$V_{DD} = 12.5\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$ ,  $P_{out} = 50\text{ W}$

f MHz	$Z_{in}$ $\Omega$	$Z_{OL}^*$ $\Omega$
135	$4.1 + j0.5$	$1.0 + j0.6$
155	$4.2 + j1.7$	$1.2 + j.09$
175	$3.7 + j2.3$	$0.7 + j1.1$

$Z_{in}$  = Complex conjugate of source impedance.

$Z_{OL}^*$  = Complex conjugate of the load impedance at given output power, voltage, frequency, and  $\eta_D > 50\%$ .

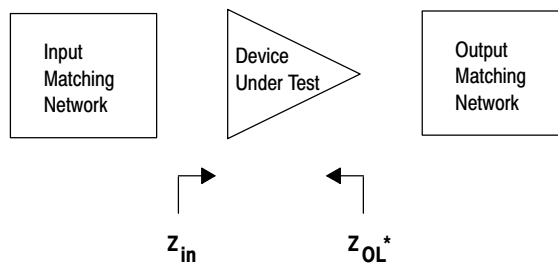


Figure 11. Series Equivalent Input and Output Impedance

**Table 5. Common Source Scattering Parameters ( $V_{DD} = 12.5$  Vdc)**

$I_{DQ} = 500$  mA

f MHz	$S_{11}$		$S_{21}$		$S_{12}$		$S_{22}$	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
50	0.93	-178	4.817	80	0.009	-39	0.86	-176
100	0.94	-178	2.212	69	0.009	-3	0.88	-175
150	0.95	-178	1.349	61	0.008	-8	0.90	-174
200	0.95	-178	0.892	54	0.006	-13	0.92	-174
250	0.96	-178	0.648	51	0.005	-7	0.93	-174
300	0.97	-178	0.481	47	0.004	-8	0.95	-174
350	0.97	-178	0.370	46	0.005	4	0.95	-174
400	0.98	-178	0.304	43	0.001	15	0.97	-174
450	0.98	-178	0.245	43	0.005	81	0.97	-174
500	0.98	-178	0.209	43	0.003	84	0.97	-174
550	0.99	-177	0.178	41	0.007	70	0.98	-175
600	0.98	-178	0.149	41	0.010	106	0.96	-175

$I_{DQ} = 2.0$  mA

f MHz	$S_{11}$		$S_{21}$		$S_{12}$		$S_{22}$	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
50	0.93	-177	4.81	80	0.003	-119	0.93	-178
100	0.94	-178	2.20	69	0.006	4	0.93	-178
150	0.95	-178	1.35	61	0.003	-1	0.93	-177
200	0.95	-178	0.89	54	0.004	18	0.93	-176
250	0.96	-178	0.65	51	0.001	28	0.94	-176
300	0.97	-178	0.48	47	0.004	77	0.94	-175
350	0.97	-178	0.37	46	0.006	85	0.95	-175
400	0.98	-178	0.30	43	0.007	53	0.96	-174
450	0.98	-178	0.25	43	0.006	74	0.97	-174
500	0.98	-177	0.21	44	0.006	84	0.97	-174
550	0.99	-177	0.18	41	0.002	106	0.97	-175
600	0.98	-178	0.15	41	0.004	116	0.96	-174

$I_{DQ} = 4.0$  mA

f MHz	$S_{11}$		$S_{21}$		$S_{12}$		$S_{22}$	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
50	0.97	-179	5.04	87	0.002	-116	0.94	-179
100	0.96	-179	2.43	82	0.006	42	0.94	-178
150	0.96	-179	1.60	77	0.004	13	0.94	-177
200	0.96	-179	1.14	74	0.003	43	0.95	-176
250	0.97	-179	0.89	71	0.004	65	0.95	-175
300	0.97	-179	0.71	68	0.006	68	0.95	-175
350	0.97	-179	0.57	67	0.006	74	0.97	-174

**Table 5. Common Source Scattering Parameters ( $V_{DD} = 12.5$  Vdc) (continued)**

$I_{DQ} = 4.0$  mA (continued)

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠ φ	S <sub>21</sub>	∠ φ	S <sub>12</sub>	∠ φ	S <sub>22</sub>	∠ φ
400	0.97	-179	0.49	63	0.005	58	0.97	-173
450	0.98	-178	0.41	63	0.005	73	0.98	-173
500	0.98	-178	0.36	62	0.003	128	0.98	-173
550	0.98	-178	0.32	58	0.004	57	0.99	-174
600	0.98	-178	0.27	58	0.009	83	0.98	-174



### DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Freescale Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

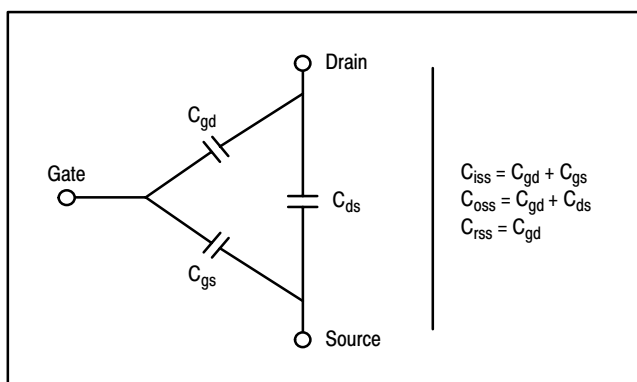
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ). These capacitances are characterized as input ( $C_{iss}$ ), output ( $C_{oss}$ ) and reverse transfer ( $C_{rss}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iss}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



### DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $R_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed  $V_{DS(on)}$ . For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

$BV_{DSS}$  values for this device are higher than normally required for typical applications. Measurement of  $BV_{DSS}$  is not recommended and may result in possible damage to the device.

### GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high - on the order of  $10^9 \Omega$  — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating. Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

### DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current ( $I_{DQ}$ ), whose value is application dependent. This device was characterized at  $I_{DQ} = 150 \text{ mA}$ , which is the suggested value of bias current for typical applications. For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

### GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

## AMPLIFIER DESIGN

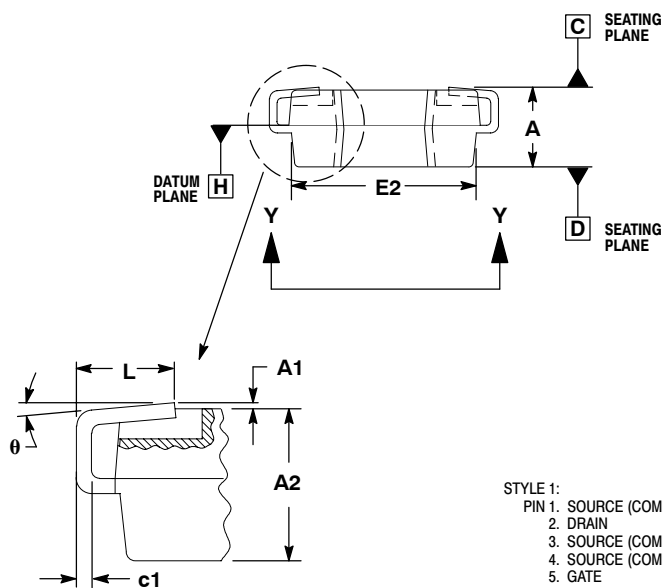
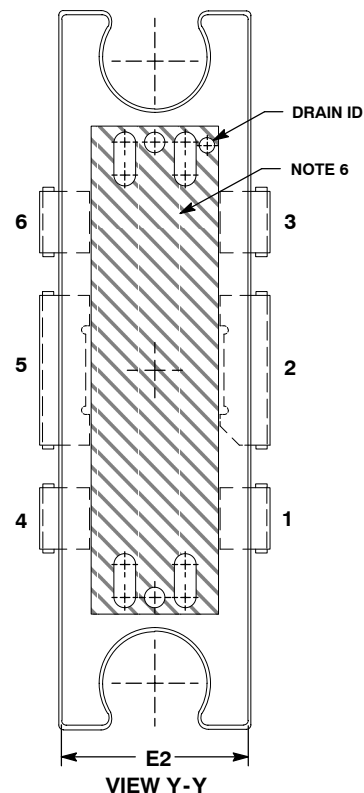
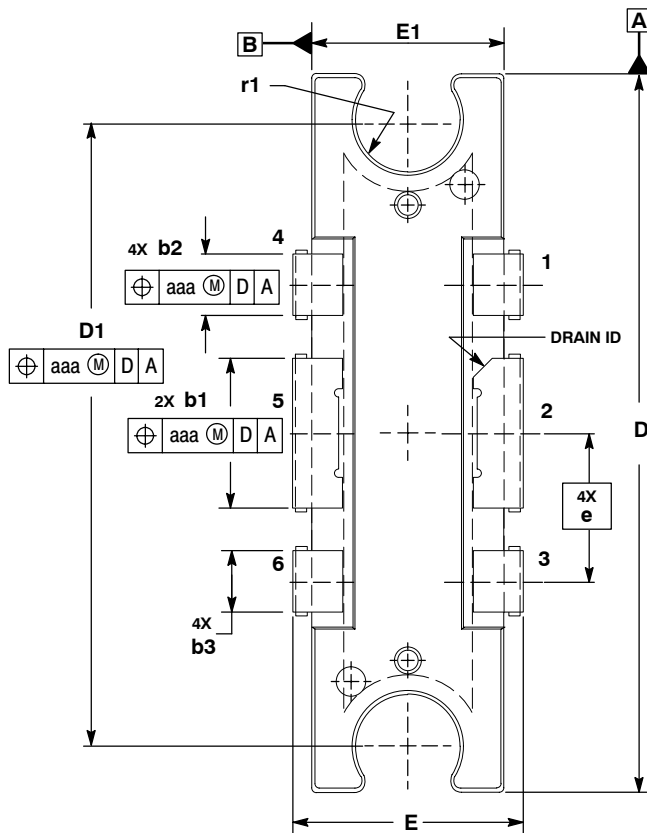
Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Freescale Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt

resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Freescale Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

# PACKAGE DIMENSIONS

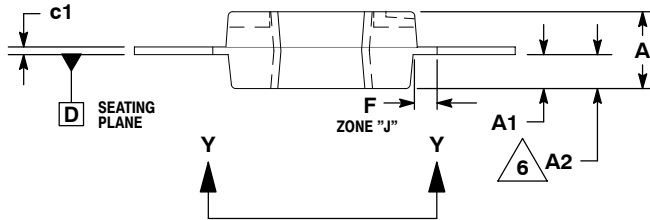
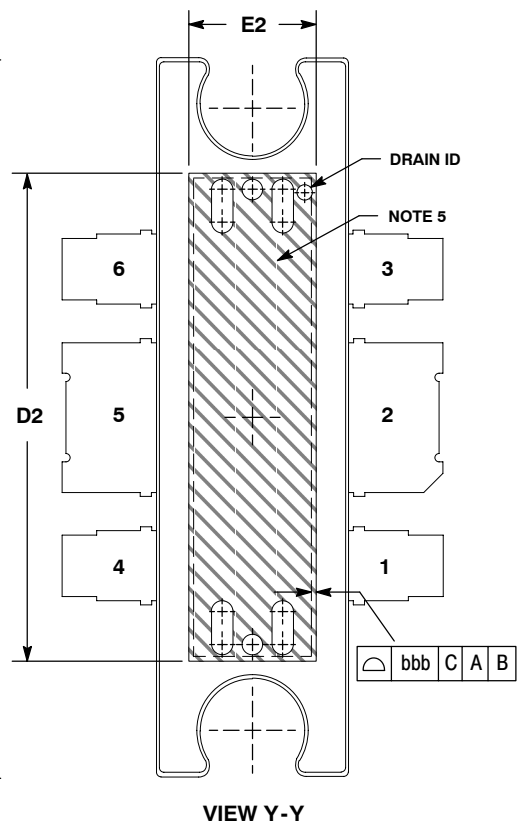
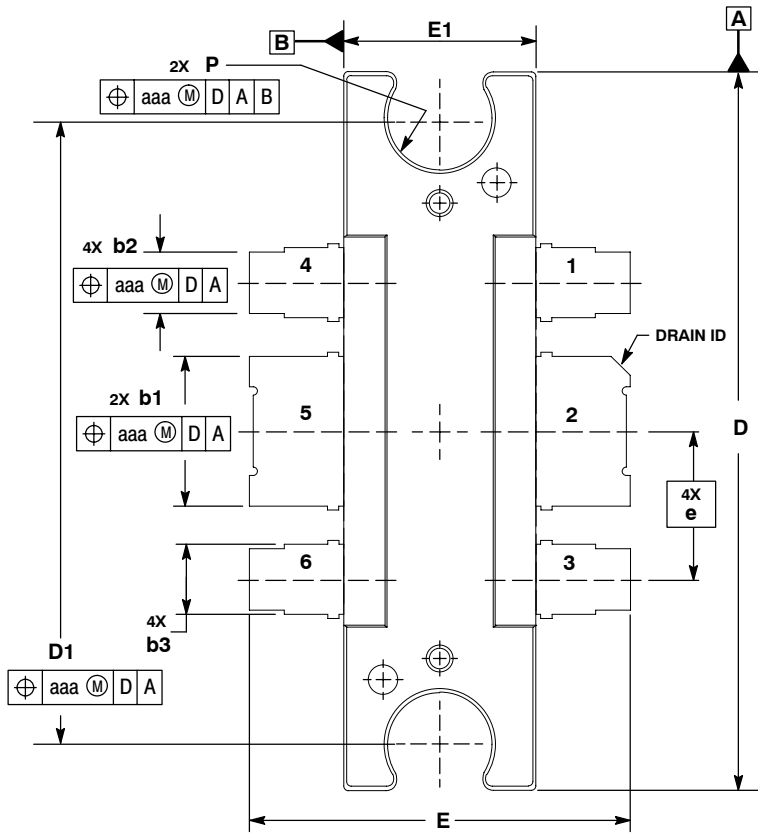


STYLE 1:  
 PIN 1. SOURCE (COMMON)  
 2. DRAIN  
 3. SOURCE (COMMON)  
 4. SOURCE (COMMON)  
 5. GATE  
 6. SOURCE (COMMON)

**CASE 1264-09**  
**ISSUE K**  
**TO-272-6 WRAP**  
**PLASTIC**  
**MRF1550NT1**

- NOTES:
1. CONTROLLING DIMENSION: INCH .
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
  4. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSION D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  5. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
  6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.108	2.49	2.74
A1	0.000	0.004	0.00	0.10
A2	0.100	0.104	2.54	2.64
D	0.928	0.932	23.57	23.67
D1	0.806	0.814	20.47	20.68
E	0.296	0.304	7.52	7.72
E1	0.248	0.252	6.30	6.40
E2	0.241	0.245	6.12	6.22
L	0.060	0.070	1.52	1.78
b1	0.193	0.199	4.90	5.05
b2	0.078	0.084	1.98	2.13
b3	0.088	0.094	2.24	2.39
c1	0.007	0.011	0.18	0.28
e	0.193 BSC		4.90 BSC	
r1	0.063	0.068	1.60	1.73
θ	0°	6°	0°	6°
aaa	0.004		0.10	



- NOTES:
1. CONTROLLING DIMENSION: INCH.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  4. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
  5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
  6. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.098	0.106	2.49	2.69
A1	0.038	0.044	0.96	1.12
A2	0.040	0.042	1.02	1.07
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.492	0.500	12.50	12.70
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
F	0.025 BSC		0.64 BSC	
P	0.126	0.134	3.20	3.40
b1	0.193	0.199	4.90	5.05
b2	0.078	0.084	1.98	2.13
b3	0.088	0.094	2.24	2.39
c1	0.007	0.011	0.178	0.279
e	0.193 BSC		4.90 BSC	
aaa	0.004		0.10	
bbb	0.008		0.20	

- STYLE 1:  
 PIN 1. SOURCE (COMMON)  
 2. DRAIN  
 3. SOURCE (COMMON)  
 4. SOURCE (COMMON)  
 5. GATE  
 6. SOURCE (COMMON)

**CASE 1264A-02  
 ISSUE C  
 TO-272-6  
 PLASTIC  
 MRF1550FNT1**

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **E-mail:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T., Hong Kong  
+800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.  
© Freescale Semiconductor, Inc. 2006. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

