

**ML7048-01****Preliminary****3-Channel Single Rail CODEC****GENERAL DESCRIPTION**

The ML7048 is a three-channel single rail CMOS CODEC LSI. This device contains filters for A-to-D and D-to-A conversions of voice signals ranging 300 to 3400 Hz.

The ML7048 is designed for a single power supply and low power applications and contains three-channel A-to-D and D-to-A converters on a single chip, and achieves a reduced footprint and external component parts.

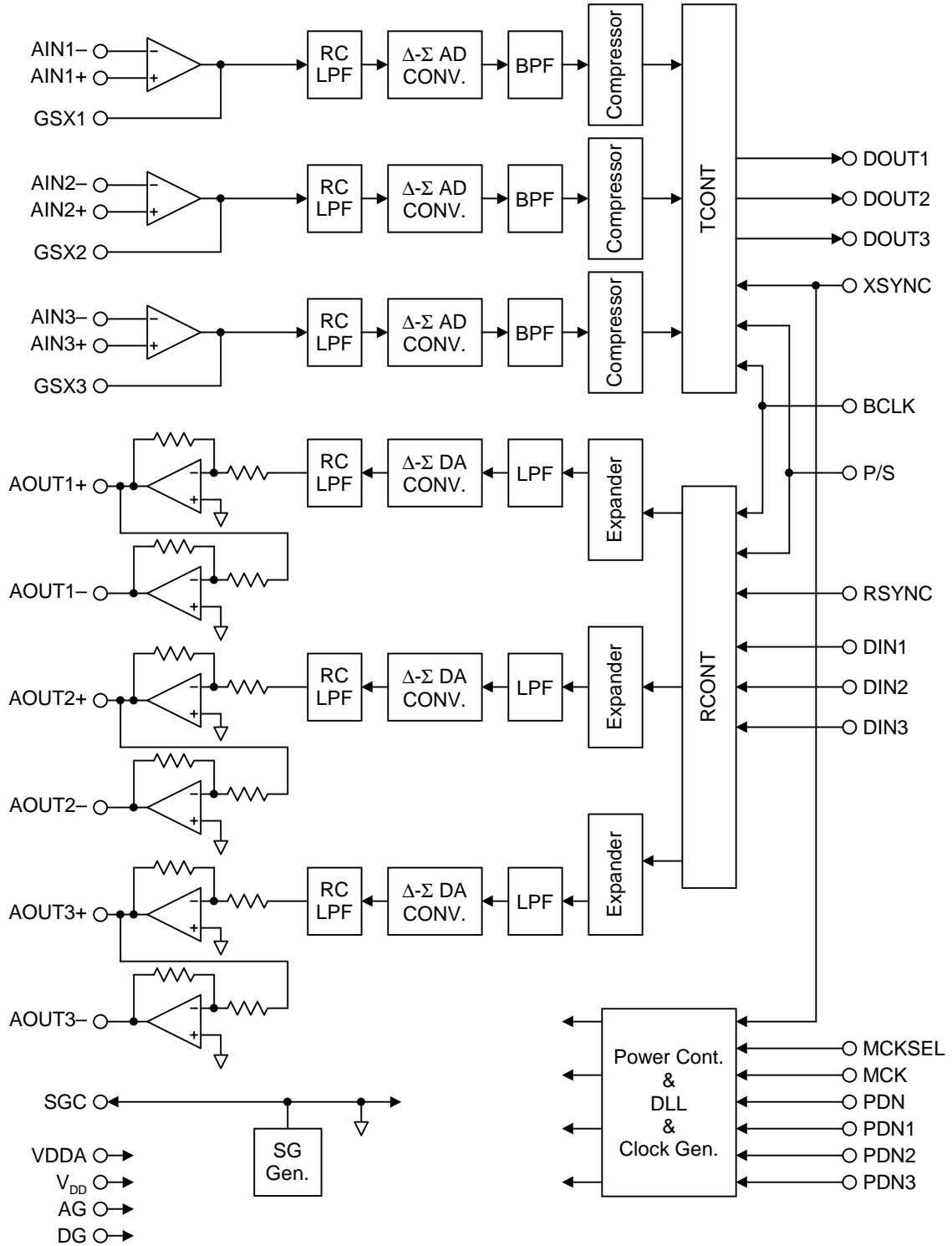
The ML7048 is best suited for ISDN terminal and digital telephone terminal applications.

**FEATURES**

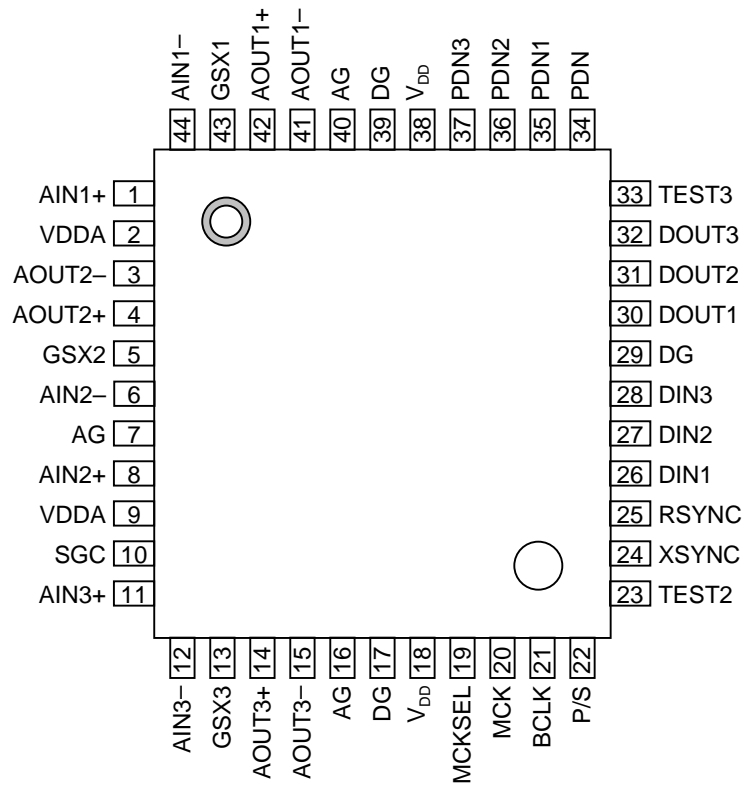
- Single 5 V Power Supply Operation
- Using  $\Delta$ - $\Sigma$  ADC and DAC Technique
- Low Power Consumption
 

3-Channel Operating Mode:	typical: 140 mW	max.:174 mW
Power Saving Mode: (PDN = "1", PDN1 to 3 = "0")	typical: 15 mW	max.: 26 mW
Power Down Mode: (PDN = "0")	typical: 0.05 mW	max.: 0.3 mW
- ITU-T Companding Law:  $\mu$ -law
- PCM Interface:
  - 3-Channel Independent or 3-Channel Continuous Serial Interface Pin Selectable
- Master Clock:
  - 12.288 MHz or 15.360 MHz Pin Selectable
- Transmission Clocks:
  - 64, 128, 256, 512, 1024, 2048 kHz
  - 96, 192, 384, 768, 1536 kHz
- Adjustable Transmit Gain for Each Channel
- Built-in Reference Voltage Supply
- Differential Analog Output can Directly Drive a 600 $\Omega$  Transformer.
- Package:
  - 44-pin Plastic QFP (QFP44-P-910-0.80-2K) (Product name: ML7048-01GA)

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



**44-Pin Plastic QFP**

## PIN DESCRIPTION

Pin	Symbol	Type	Description
1	AIN1+	I	Channel-1 Transmit Amp Non-inverting Input
2	VDDA	—	Analog Power Supply
3	AOUT2–	O	Channel-2 Receive Amp Inverting Output
4	AOUT2+	O	Channel-2 Receive Amp Non-inverting Output
5	GSX2	O	Channel-2 Transmit Amp Output
6	AIN2–	I	Channel-2 Transmit Amp Inverting Input
7	AG	—	Analog Ground
8	AIN2+	I	Channel-2 Transmit Amp Non-inverting Input
9	VDDA	—	Analog Power Supply
10	SGC	O	Analog Signal Ground
11	AIN3+	I	Channel-3 Transmit Amp Non-inverting Input
12	AIN3–	I	Channel-3 Transmit Amp Inverting Input
13	GSX3	O	Channel-3 Transmit Amp Output
14	AOUT3+	O	Channel-3 Receive Amp Non-inverting Output
15	AOUT3–	O	Channel-3 Receive Amp Inverting Output
16	AG	—	Analog Ground
17	DG	—	Digital Ground
18	V <sub>DD</sub>	—	Digital Power Supply
19	MCKSEL	I	Master Clock Frequency Select Signal
20	MCK	I	Master Clock
21	BCLK	I	PCM Signal Shift Clock
22	P/S	I	3-Channel Independent/3-Channel Continuous Serial Interface Select Signal
23	TEST2	I	Test Control Signal 2
24	XSYNC	I	Transmit Sync Signal
25	RSYNC	I	Receive Sync Signal
26	DIN1	I	Channel-1 PCM Signal Input
27	DIN2	I	Channel-2 PCM Signal Input
28	DIN3	I	Channel-3 PCM Signal Input
29	DG	—	Digital Ground
30	DOUT1	O	Channel-1 PCM Signal Output
31	DOUT2	O	Channel-2 PCM Signal Output
32	DOUT3	O	Channel-3 PCM Signal Output
33	TEST3	I	Test Control Signal 3
34	PDN	I	Power Down Control Signal
35	PDN1	I	Channel-1 Power Down Control Signal
36	PDN2	I	Channel-2 Power Down Control Signal
37	PDN3	I	Channel-3 Power Down Control Signal
38	V <sub>DD</sub>	—	Digital Power Supply
39	DG	—	Digital Ground
40	AG	—	Analog Ground
41	AOUT1–	O	Channel-1 Receive Amp Inverting Output
42	AOUT1+	O	Channel-1 Receive Amp Non-inverting Output
43	GSX1	O	Channel-1 Transmit Amp Output
44	AIN1–	I	Channel-1 Transmit Amp Inverting Input

## PIN FUNCTIONAL DESCRIPTION

### AIN1+, AIN2+, AIN3+, AIN1-, AIN2-, AIN3-, QSX1, GSX2, GSX3

AIN1+, AIN1- and GSX1 are the transmit inputs and transmit level adjustment pins for Channel 1, AIN2+, AIN2- and GSX2 are those for Channel 2. AIN3+, and AIN3- and GSX3 are those for Channel 3.

AIN1+, AIN2+ and AIN3+ are non-inverting inputs for the op-amp.

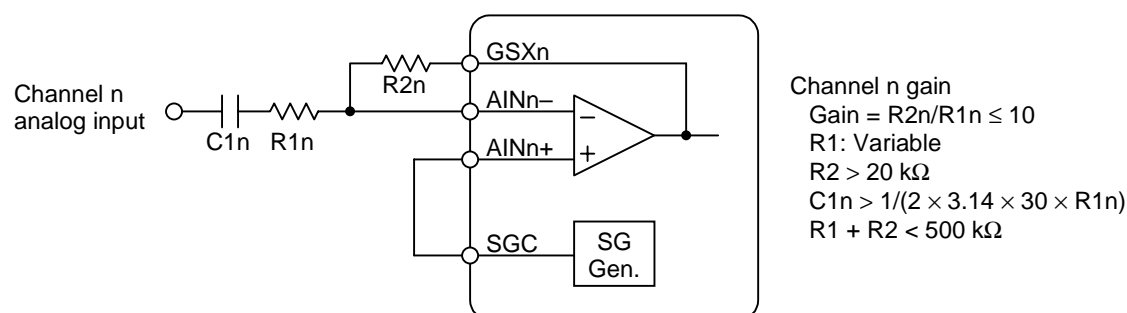
AIN1-, AIN2- and AIN3- are inverting inputs for the op-amp.

GSX1, GSX2 and GSX3 are the outputs for op-amp.

Do the level adjustment as described below.

If AINn- and AINn+ are not used, connect AINn- to GSXn and AINn+ to SGC.

During power saving and power down modes, GSX1, GSX2, and GSX3 outputs are at a high impedance. During power down mode in each channel, the GSX output of a channel in power down mode is at a high impedance.



### AOUT1+, AOUT1-, AOUT2+, AOUT2-, AOUT3+, AOUT3-

AOUT1+ and AOUT1- are the receive analog output pins for Channel 1, AOUT2+ and AOUT2- are those for Channel 2, and AOUT3+ and AOUT3- are those for Channel 3.

AOUT1- is the inverting output for AOUT1+, AOUT2- is for AOUT2+, and AOUT3- is for AOUT3+. A load of  $600\Omega$  or more can be driven between AOUT1+ and AOUT1-, AOUT2+ and AOUT2-, and AOUT3+ and AOUT3-. The output signal has an amplitude of 3.4 Vpp above and below the signal ground voltage (SG) when the digital signal of 3.17 dBm0 is input to DIN1, DIN2, and DIN3.

During power saving and power down modes, the AOUT1+, AOUT1-, AOUT2+, AOUT2-, AOUT3+, and AOUT3- outputs are at a high impedance.

During power down mode in each channel, the AOUTn+ and AOUTn- of a channel in power down are at a high impedance.

### SGC

Bypass capacitor pin used to generate the signal ground voltage level.

Connect a 1  $\mu\text{F}$  capacitor with excellent high frequency characteristics between the SGC pin and the AG pin.

### MCK

Master clock input pin. The frequency is 12.288 MHz or 15.360 MHz.

The frequency is switched by MCKSEL. This master clock may be asynchronous with BCLK, RSYNC, and XSYNC.

### MCKSEL

Master clock frequency select signal input pin. Input a 12.288 MHz clock to the MCK pin when MCKSEL is "0". Input a 15.360 MHz clock to the MCK pin when MCKSEL is "1".

### PDN

Power down control signal input pin. When PDN is "0", all circuits are in power down mode.

**PDN1, PDN2, PDN3**

PDN1 is the power down control signal input pin for Channel 1, PDN2 is for Channel 2, and PDN3 is for Channel 3.

When PDN is “1” and PDN1, PDN2, and PDN3 are “0s”, the corresponding channel goes in power saving mode (all analog circuits except the reference voltage generation circuit are being powered down).

**P/S**

Signal input pin for selecting either 3-channel independent serial interface or 3-channel continuous serial interface. When P/S is “0”, 3-channel independent serial interface, in which the input/output of each channel is made through DIN1 to 3 and DOUT1 to 3 independently, is selected.

When P/S is “1”, 3-channel continuous serial interface, in which the input/output of each channel is made from DIN1 and DOUT1 continuously.

When 3-channel continuous serial interface is selected, DOUT2 and DOUT3 pins are at a high impedance. Connect the DIN2 and DIN3 pins to the digital ground (DG).

**BCLK**

PCM signal shift clock input pin for DIN1, DIN2, DIN3, DOUT1, DOUT2, and DOUT3.

The frequency is equal to the data rate.

The clock frequencies available are 64, 96, 128, 192, 256, 384, 512, 1024, 1536, and 2048 kHz.

When P/S is “1” and 3-channel continuous serial interface is selected, the frequencies of 64, 96, and 128 kHz cannot be used.

**RSYNC**

Receive synchronizing signal input pin.

This signal selects necessary 8-bit PCM data from serial PCM signals for the DIN1, DIN2 and DIN3 pins. This synchronizing signal must be synchronized in phase with BCLK (generated from BCLK).

**XSYNC**

Transmit synchronizing signal input pin.

This synchronizing signal must be synchronized in phase with BCLK (generated from BCLK). The DPLL circuit is synchronized in phase with XSYNC.

**DIN1, DIN2, DIN3**

When P/S is “0” and 3-channel independent serial interface is selected, DIN1 is the PCM signal input pin for Channel 1, DIN2 is for Channel 2, and DIN3 is for Channel 3.

When P/S is “1” and 3-channel continuous serial interface is selected, DIN1 is the PCM signal input pin for each channel and data is input in the order of Channel 1, Channel 2 and Channel 3.

At that time, connect DIN2 and DIN3 to the digital ground (DG).

The PCM signal data rate is equal to the frequency of BCLK. The PCM signal is shifted at the falling edge of BCLK. The MSD of PCM data is identified at the rising edge of RSYNC.

**DOUT1, DOUT2, DOUT3**

When P/S is “0” and 3-channel independent serial interface is selected, DOUT1 is the PCM signal output pin for Channel 1, DOUT2 is for Channel 2, and DOUT3 is for Channel 3.

When P/S is “1” and 3-channel continuous serial interface is selected, DOUT1 is the PCM signal output pin for each channel and data is output in the order of Channel 1, Channel 2, and Channel 3. At that time, DOUT2 and DOUT3 are at a high impedance state.

The PCM signal is sequentially output starting from MSD in synchronization with the rise of BCLK. (MSD may be output at the rising edge of XSYNC depending on the timing of BCLK and XSYNC.) These pins are at a high impedance during the time other than PCM data output bits.

These pins also are at a high impedance during power down mode and power saving mode.

These pins must be internally connected to pull-up resistors because the output form is of open-drain. For coding law, the ITU-T Recommend  $\mu$ -law is employed.

Input/output level	PCMIN / PCMOUT							
	$\mu$ -law							
	M S D	D 2	D 3	D 4	D 5	D 6	D 7	D 8
+ full scale	1	0	0	0	0	0	0	0
+0	1	1	1	1	1	1	1	1
-0	0	1	1	1	1	1	1	1
- full scale	0	0	0	0	0	0	0	0

**Table 1 Coding law**

**VDDA**

+5V power supply for analog signal circuits.

Use an analog power supply system of equipment used.

Connect a bypass capacitor of 1  $\mu$ F with excellent high frequency characteristics and a capacitor of 10  $\mu$ F between this pin and the AG pin.

**AG**

Ground pin for analog signal circuits.

**V<sub>DD</sub>**

+5V power supply pin for digital signal circuits.

Although this pin and VDDA are not connected internally, these pins must be connected on the printed circuit board.

**DG**

Ground pin for digital signal circuits.

Although this pin and AG are not connected internally, these pins must be connected on the printed circuit board.

**TEST2, TEST3**

These pins are used for device test.

These device test pins must be connected to the DG pin.

PDN	PDNn	DOUTn
0	0/1	H
1	0	11111111
1	1	Converted output

**Table 2 Power Control vs. DOUT Output Status**

PDN	PDN1	PDN2	PDN3	GSX1, AOUT1±	GSX2, AOUT2±	GSX3, AOUT3±	SGC
0	0/1	0/1	0/1	High impedance	High impedance	High impedance	Connected to AG with a resistor of about 50 kΩ
1	0	0	0	High impedance	High impedance	High impedance	Operating
1	1	0/1	0/1	Operating	Depending on PDN2	Depending on PDN3	Operating
1	0/1	1	0/1	Depending on PDN1	Operating	Depending on PDN3	Operating
1	0/1	0/1	1	Depending on PDN1	Depending on PDN2	Operating	Operating

**Table 3 Power Control vs. Analog Output Status**



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	$V_{DD}$	—	-0.3 to +7.0	V
Analog Input Voltage	$V_{AIN}$	—	-0.3 to $V_{DD}+0.3$	V
Digital Input Voltage	$V_{DIN}$	—	-0.3 to $V_{DD}+0.3$	V
Storage Temperature	$T_{STG}$	—	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}$	Voltage must be fixed	4.75	5.0	5.25	V
Operating Temperature	$T_{OP}$	—	-30	—	+85	°C
Analog Input Voltage	$V_{AIN}$	Gain = 1	—	—	2.26	$V_{PP}$
High Level Input Voltage	$V_{IH}$	All Digital Input Pins	2.2	—	$V_{DD}$	V
Low Level Input Voltage	$V_{IL}$		0	—	0.8	V
MCK Frequency	$F_{MCK}$	MCKSEL = "0"	-100ppm	12.288	+100ppm	MHz
		MCKSEL = "1"	-100ppm	15.360	+100ppm	
BCLK Frequency	$F_{BCLK}$	BCLK	64k, 128k, 256k, 512k, 1.024M, 2.048M 96k, 192k, 284k, 768k, 1.536M			Hz
Sync Pulse Frequency	$F_{SYNC}$	XSYNC, RSYNC	—	8	—	kHz
Clock Duty Ratio	$D_{CLK}$	MCK, BCLK	40	50	60	%
Digital Input Rise Time	$T_{IR}$	All Digital Input Pins	—	—	50	ns
Digital Input Fall Time	$T_{IF}$		—	—	50	ns
Transmit Sync Pulse Setting Time	$T_{XS}$	BCLK to XSYNC	50	—	—	ns
	$T_{SX}$	XSYNC to BCLK	50	—	—	ns
Receive Sync Pulse Setting Time	$T_{RS}$	BCLK to RSYNC	50	—	—	ns
	$T_{SR}$	RSYNC to BCLK	50	—	—	ns
Sync Pulse Width	$T_{WS}$	XSYNC, RSYNC	1 BCLK	—	100	μs
DIN Set-up Time	$T_{DS}$	DIN1 to 3	50	—	—	ns
DIN Hold Time	$T_{DH}$	DIN1 to 3	50	—	—	ns
Digital Output Load	$R_{DL}$	Pull-up Resistor, DOUT1 to 3	0.5	—	—	kΩ
	$C_{DL}$	DOUT1 to 3	—	—	50	pF
Allowable Jitter Width	$T_{JT}$	XSYNC, RSYNC	—	—	500	ns
Bypass Capacitor for SGC	$C_{SG}$	Between SGC and AG	1	—	—	μF

## ELECTRICAL CHARACTERISTICS

### DC and Digital Interface Characteristics

(V<sub>DD</sub> = 4.75 to 5.25 V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I <sub>DD1</sub>	3CH Operating Mode, No Signal PDN = "1", PDN1 = PDN2 = PDN3 = "1"	—	28.0	33.0	mA
	I <sub>DD2</sub>	Power Saving Mode, PDN = "1", PDN1 = PDN2 = PDN3 = "0"	—	3.0	5.0	mA
	I <sub>DD3</sub>	Power Down Mode, PDN = "0" All inputs fixed	—	0.01	0.05	mA
High Level Input Leakage Current	I <sub>IH</sub>	All Digital Input Pins V <sub>I</sub> = V <sub>DD</sub>	—	—	10	μA
Low Level Input Leakage Current	I <sub>IL</sub>	All Digital Input Pins V <sub>I</sub> = 0 V	—	—	10	μA
Digital Output Low Voltage	V <sub>OL</sub>	DOUT1 to 3, Pull-up = 0.5 kΩ	0	0.2	0.4	V
Digital Output Leakage Current	I <sub>O</sub>	DOUT1 to 3, High Impedance State	—	—	10	μA
Input Capacitance	C <sub>IN</sub>	—	—	5	—	pF

### Analog Interface Characteristics

(V<sub>DD</sub> = 4.75 to 5.25 V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SGC Rise Time	T <sub>SGC</sub>	SGC to AG 0.1 μF Rise time to 90% of max. level	—	—	100	ms

### Transmit Analog Interface Characteristics

(V<sub>DD</sub> = 4.75 to 5.25 V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R <sub>INX</sub>	AIN1, AIN2	10	—	—	MΩ
Output Load Resistance	R <sub>LGX</sub>	GSX1, GSX2 with respect to SG voltage *1 Gain = 1	20	—	—	kΩ
Output Load Capacitance	C <sub>LGX</sub>		—	—	30	pF
Output Amplitude	V <sub>OGX</sub>		-1.13	—	+1.13	V
Offset Voltage	V <sub>OSGX</sub>		-50	—	+50	mV

\*1 -2.73 dBm (600Ω) = 3.17 dBm0 (μ-law) = 2.26 V<sub>PP</sub>

## Receive Analog Interface Characteristics

 $(V_{DD} = 4.75 \text{ to } 5.25 \text{ V}, T_a = -30 \text{ to } +85^\circ\text{C})$ 

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Load Resistance	$R_{LAO}$	AOUT1 $\pm$ , AOUT2 $\pm$ AOUT3 $\pm$ with respect to inverting output	0.6	—	—	k $\Omega$
Output Load Capacitance	$C_{LAO}$	AOUT1 $\pm$ , AOUT2 $\pm$ , AOUT3 $\pm$	—	—	50	pF
Output Amplitude	$V_{OAO}$	AOUT1 $\pm$ , AOUT2 $\pm$ , AOUT3 $\pm$ , $R_{LAO}=0.6 \text{ k}\Omega$ with respect to inverting output	-1.7	—	+1.7	V
Offset Voltage	$V_{OSAO}$	AOUT1 $\pm$ , AOUT2 $\pm$ , AOUT3 $\pm$ with respect to SG voltage	-100	—	+100	mV

## AC Characteristics

 $(V_{DD} = 4.75 \text{ to } 5.25 \text{ V}, T_a = -30 \text{ to } +85^\circ\text{C})$ 

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	
		Freq.	Level					
Transmit Frequency Response	Loss T1	60	0	(Attenuation)	25	45	—	dB
	Loss T2	300			-0.15	+0.15	+0.20	
	Loss T3	1020			Reference			
	Loss T4	3000			-0.15	+0.02	+0.20	
	Loss T5	3300			-0.15	+0.1	+0.80	
	Loss T6	3400			0	0.6	0.80	
Receive Frequency Response	Loss R1	100	0	(Attenuation)	-0.15	+0.04	+0.2	dB
	Loss R2	1020			Reference			
	Loss R3	3000			-0.15	+0.07	+0.20	
	Loss R4	3300			-0.15	+0.20	+0.80	
	Loss R5	3400			0	0.6	0.8	
Transmit Signal to Distortion Ratio	SDT1	1020	3	*2	36	43	—	dB
	SDT2		0		36	41	—	
	SDT3		-30		36	39	—	
	SDT4		-40		30	34	—	
	SDT5		-45		25	31	—	
Receive Signal to Distortion Ratio	SDR1	1020	3	*2	36	43	—	dB
	SDR2		0		36	41	—	
	SDR3		-30		36	39	—	
	SDR4		-40		30	34	—	
	SDR5		-45		25	31	—	
Transmit Gain Tracking	GTT1	1020	3		-0.2	+0.02	+0.2	dB
	GTT2		-10		Reference			
	GTT3		-40		-0.2	+0.06	+0.2	
	GTT4		-50		-0.6	+0.3	+0.6	
	GTT5		-55		-1.2	+0.5	+1.2	
Receive Gain Tracking	GTR1	1020	3	DIN to AOUTn	-0.2	0	+0.2	dB
	GTR2		-10		Reference			
	GTR3		-40		-0.2	-0.02	+0.2	
	GTR4		-50		-0.6	-0.1	+0.6	
	GTR5		-55		-1.2	-0.2	+1.2	
Idle Channel Noise	NIDLE $_T$	—	—	AInn = SG *2	—	-76	-72	dBn0p
	NIDLE $_P$	—	—	DIN = 0 code *2	—	-88	-82	

\*2 P-message Filter is used

## AC Characteristics (Continued)

(V<sub>DD</sub> = 4.75 to 5.25 V, Ta = -30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	
		Freq.	Level					
Absolute Level (Initial Difference)	AV <sub>T</sub>	1020	0	V <sub>DD</sub> = 5 V, Ta = 25°C	0.535	0.555	0.574	Vrms
	AV <sub>R</sub>			V <sub>DD</sub> = 5 V, Ta = 25°C	0.806	0.835	0.864	
Absolute level (Deviation of Temperature and power)	AV <sub>TT</sub>			V <sub>DD</sub> = 4.75 to 5.25 V Ta = -40 to 85°C	-0.3	—	0.3	dB
	AV <sub>RT</sub>				-0.3	—	0.3	
Absolute Delay	T <sub>D</sub>	1020	0	A to A Mode BCLK = 2048 kHz	—	0.54	0.6	ms
Transmit Group Delay	T <sub>GD</sub> T1	500	0	*3	—	0.26	0.75	ms
	T <sub>GD</sub> T2	600			—	0.16	0.35	
	T <sub>GD</sub> T3	1000			—	0.02	0.125	
	T <sub>GD</sub> T4	2600			—	0.05	0.125	
	T <sub>GD</sub> T5	2800			—	0.07	0.75	
Receive Group Delay	T <sub>GD</sub> R1	500	0	*3	—	0.00	0.75	ms
	T <sub>GD</sub> R2	600			—	0.00	0.35	
	T <sub>GD</sub> R3	1000			—	0.00	0.125	
	T <sub>GD</sub> R4	2600			—	0.06	0.125	
	T <sub>GD</sub> R5	2800			—	0.09	0.75	
Cross Talk Attenuation	CR <sub>T</sub>	1020	0	Trans to Receive	80	85	—	dB
	CR <sub>R</sub>			Receive to Trans	75	80	—	
	CR <sub>CH</sub>			Channel to Channel	80	85	—	
Discrimination	DIS	4.6 to 72k	0	0 to 4 kHz	30	32	—	dB
Out of Band Spurious	OBS	300 to 3.4k	0	4.6 kHz to 1000 kHz	—	-37.5	-35	dB
Signal Frequency Distortion	SFD <sub>T</sub>	1020	0	0 to 4 kHz	—	-50	-40	dBm0
	SFD <sub>R</sub>				—	-48	-40	
Intermodulation Distortion	IMD <sub>T</sub>	fa = 470	-4	2 fa - fb	—	-52	-40	dBm0
	IMD <sub>R</sub>	fb = 320			—	-52	-40	
Power Supply Noise Rejection Ratio	PSR <sub>T1</sub>	0 to 4k	100 mVrms	*4	40	44	—	dB
	PSR <sub>T2</sub>	4 to 50k			50	55	—	
	PSR <sub>R1</sub>	0 to 4k			40	45	—	
	PSR <sub>R2</sub>	4 to 50k			50	56	—	
Digital Output Delay Time	T <sub>SD</sub>	DOUTn			20	—	100	ns
	T <sub>XD1</sub>	Pull-up resistor = 0.5 kΩ			20	—	100	
	T <sub>XD2</sub>	C <sub>L</sub> = 50 pF and 1 LSTTL			20	—	100	
DOUT Signal Output Delay Time	T <sub>DDO</sub>	Signal rise time after power on by PDNn *5			—	4	—	ms
AOUT Signal Output	T <sub>DAO</sub>	Signal rise time after power on by PDNn *5			—	4	—	ms

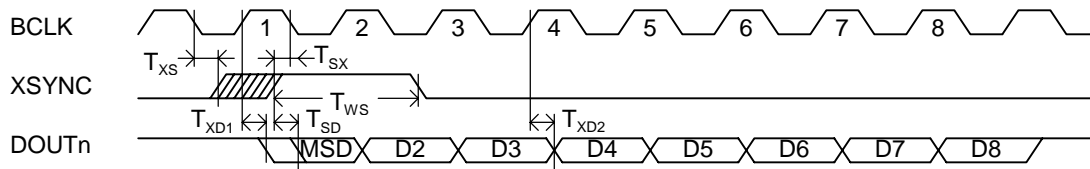
\*3 Minimum value of the group delay distortion

\*4 The measurement under idle channel noise

\*5 The rise time of SGC by PDN is not included.

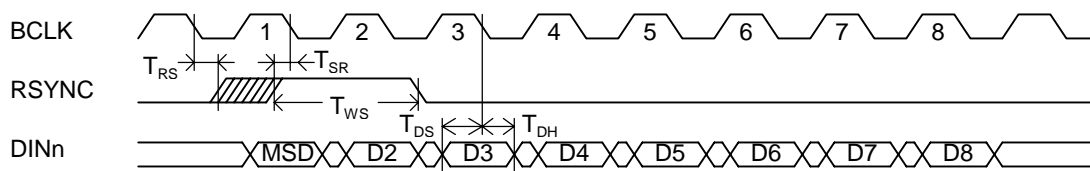
DOUT and AOUT will not rise before inputting XSYNC.

**TIMING DIAGRAM**



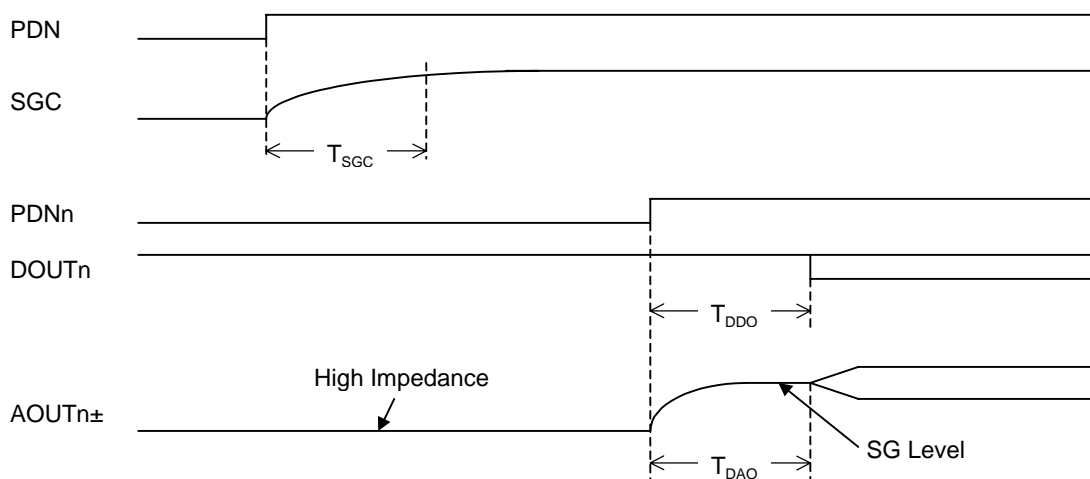
Note: In the above diagram, 3-channel independent serial interface is selected.  
 When 3-channel continuous serial interface is selected, 24-bit data is output from DOUT1 in the order of Channel 1, Channel 2, and Channel 3.

**Figure 1 Transmit side Timing Diagram**



Note: In the above diagram, 3-channel independent serial interface is selected.  
 When 3-channel continuous serial interface is selected, 24-bit data is input to DIN1 in the order of Channel 1, Channel 2, and Channel 3.

**Figure 2 Receive Side Timing Diagram**

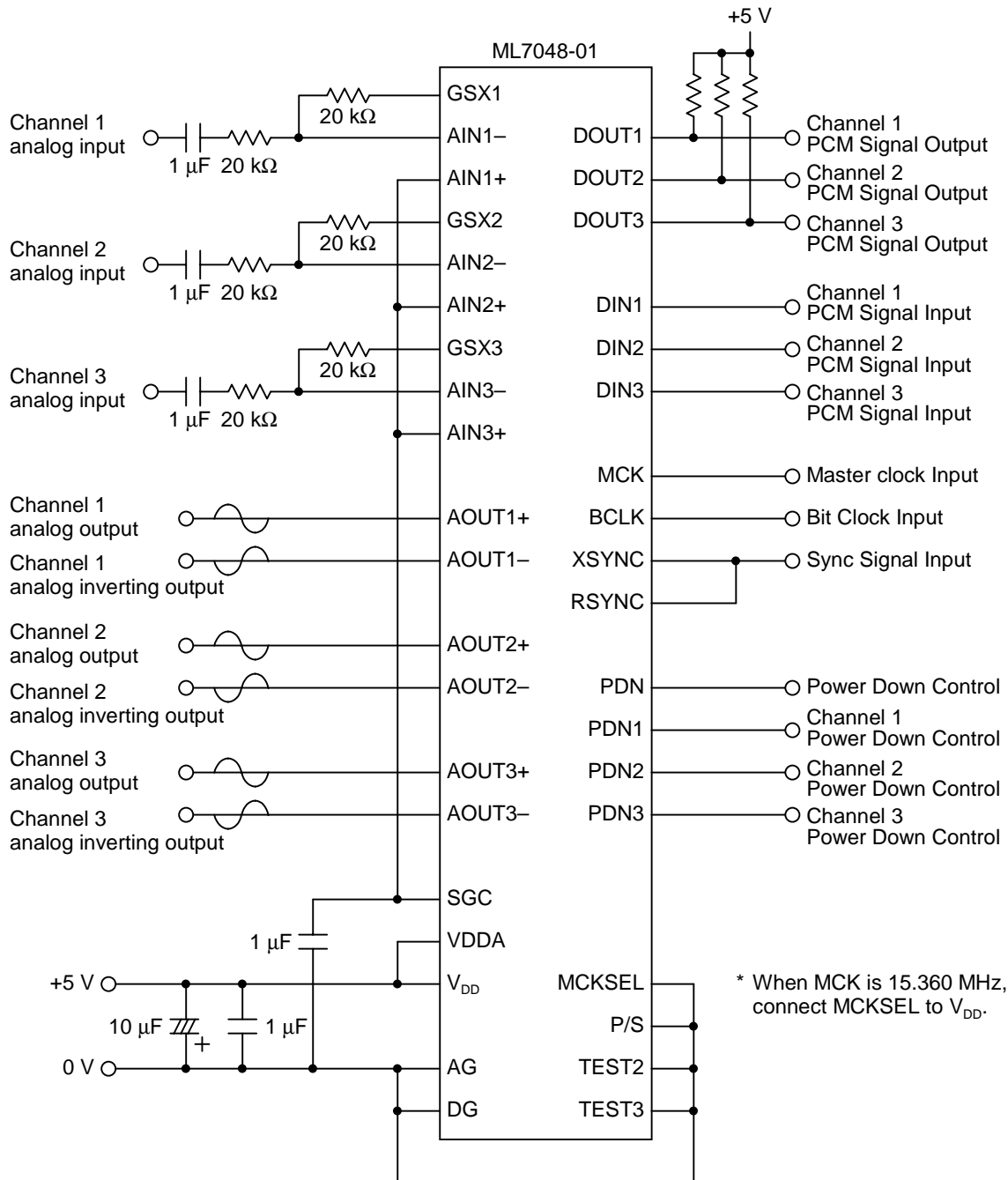


Note: DOUT and AOUT will not rise before inputting XSYNC.

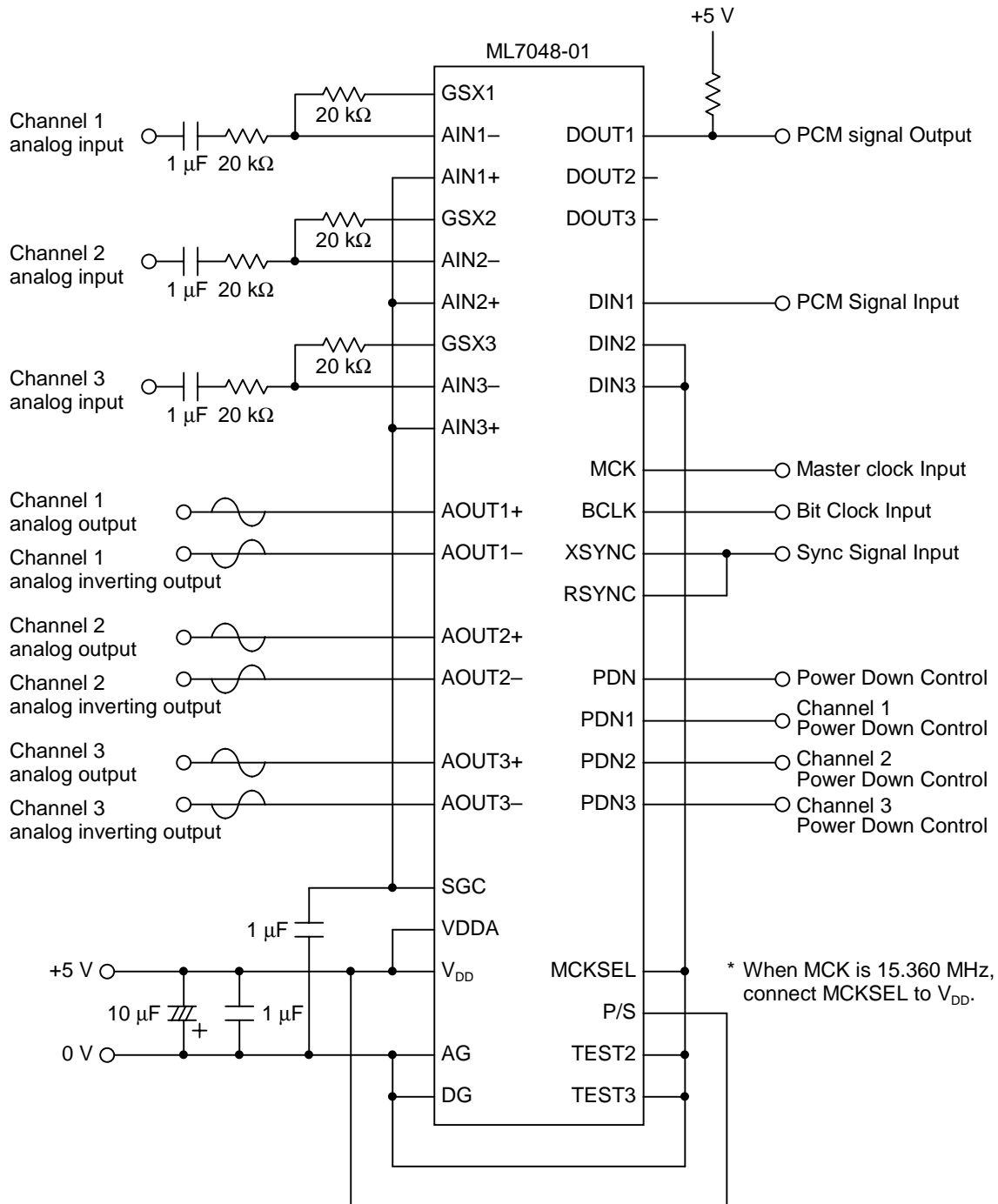
**Figure 3 SGC, DOUT, AOUT Outputs Timing**

APPLICATION CIRCUITS

When 3-channel independent serial interface is selected



When 3-channel continuous serial interface is selected



## APPLICATION NOTE

### Pull-up Resistor for the DOUT Pin

Use an optimal value of pull-up resistor for the DOUT pin considering the frequency and load capacitance of BCLK used. If a small value of pull-up resistor is used, the distortion characteristics may be degraded and current consumption also may be increased.

Select a pull-up resistance referencing the following calculation conditions.

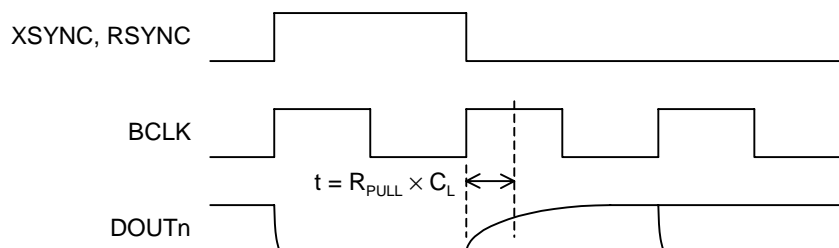
#### Calculation conditions:

If SYNC and BCLK have risen and data is looped between DOUT and DIN, data can be normally input and output.

$$R_{PULL} = \frac{1}{4 \times F_{BCLK}} - 20\text{ns} \quad (\Omega)$$

$$R_{PULL} = \frac{1}{4 \times F_{BCLK} \times C_L} - 20\text{ns} \quad (\Omega)$$

$F_{BCLK}$  : Frequency of BCLK  
 $C_L$  : Load capacitance of DOUTn  
 20ns : Internal delay



#### Calculation example:

BCLK (Hz)	$R_{PULL}$ (k $\Omega$ )			
	$C_L = 10$ pF	$C_L = 20$ pF	$C_L = 50$ pF	$C_L = 100$ pF
64k	388.6	194.3	77.7	38.9
128k	193.3	96.7	38.7	19.3
256k	95.7	47.8	19.1	9.7
512k	46.8	23.4	9.4	4.7
1.024M	22.4	11.2	4.5	2.2
2.048M	10.2	5.1	2.0	1.0

#### Selection of resistance value:

If the calculated resistance is more than 100 k $\Omega$ , use a 100 k $\Omega$  resistor.

Since the calculated resistance +10% is allowable, you can use a typical resistance a little higher than the calculated resistance.



### Cross-talk between Channels

This device contains a 3-channel CODEC.

The circuits and layout of this device have been designed so that the internal cross-talk between channels is to be as small as possible. The pins also are carefully placed.

It is required to design your printed circuit board considering the following descriptions.

#### Transmit Side:

AIN1+, AN1-, AIN2+, AIN2-, AIN3+, and AIN3- are the input pins for op-amps with a high resistance. Consequently, if the wiring patterns of these pins are close to the wiring patterns of other signals, cross-talk may be caused. And a longer wiring pattern generates noises.

The wiring pattern must be as short as possible and must not be close to the patterns of other signals. In addition, connect a ground pattern between these wiring patterns and the wiring patterns of other signals.

AIN1+, AIN2+, and AIN3+ are connected to SGC.

Connect a bypass capacitor to the SGC pin as closely as possible and place a wiring pattern for AIN+, AIN2+, and AIN3+ separately.

#### Receive Side:

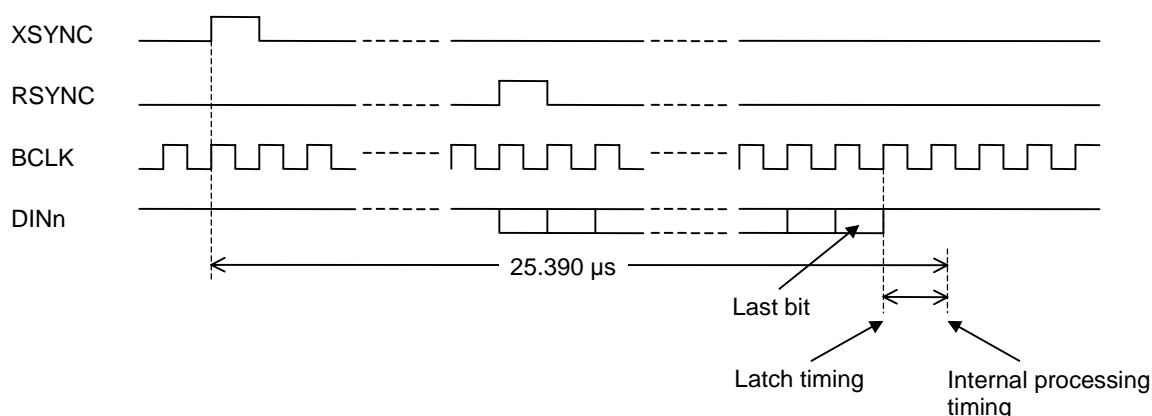
AOUT1+, AOUT1-, AOUT2+, AOUT2-, AOUT3+, and AOUT3- are the outputs for op-amps with a low resistance. Although the cross-talk caused by wiring patterns is small when compared with the transmit side, Avoid placing the wiring patterns of these pins closely to the wiring patterns of other signals.

### RSYNC Timing

Data that is input from DINn is latched at the rising edge of BCLK corresponding to the trailing edge of the last bit.

If the latch timing and the internal processing timing (25.390  $\mu$ s from the rise of XSYNC) are overlapped, data slip (data is deleted or the same data is output twice) data error may occur.

Set the timing so that the latch timing and internal processing timing are not within  $\pm 500$  ns considering the jitter of DPLL.



### Relationship between MCK and BCLK, XSYNC, RSYNC

Although MCK may be asynchronous with BCLK, XSYNC, and RSYNC, take note of the following.

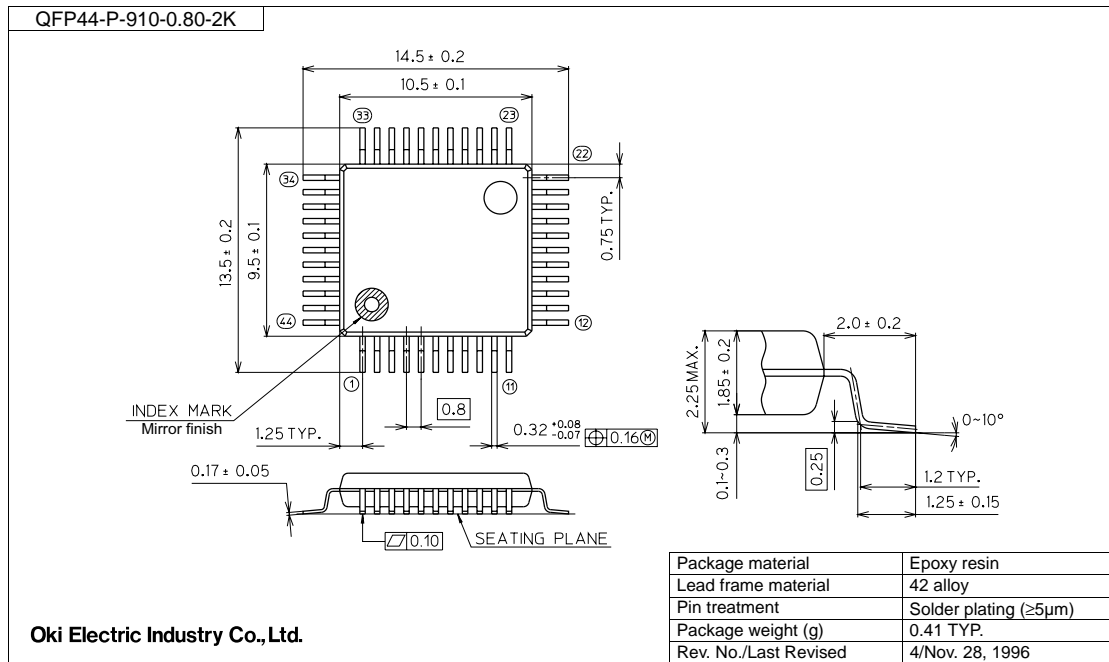
If MCK and BCLK, XSYNC, RSYNC are generated from the different oscillation sources (ex. two crystal oscillators are used) with the same frequency, the difference in frequency may cause a beat. If this beat frequency is within the band, the characteristics may be degraded.

**RECOMMENDATIONS FOR ACTUAL DESIGN**

- To assure specified electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and DG pin each other as closely as possible. Connect to the system ground with low impedance.
- Connect the VDDA pin to the V<sub>DD</sub> pin as closely as possible and connect them to the analog power supply at a low impedance.
- Directly mount this device onto the printed circuit board without using an IC socket. Unless unavoidable, use short lead type socket.
- When mounted on a frame, use electromagnetic shielding, if any electromagnetic emission sources such as power supply transformers surround the device.
- Keep the voltage on the V<sub>DD</sub> pin not lower than -0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise power supply (having low level high frequency spike noise or pulse noise) to avoid erroneous operation and the degradation of the characteristics of these device.

**PACKAGE DIMENSIONS**

(Unit: mm)



**Notes for Mounting the Surface Mount Type Package**

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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