MIC2159

SYNCHRONOUS-itty™ Step-Down Converter IC

General Description

The MIC2159 is a high efficiency, simple to use synchronous buck controller ICs housed in a 10-pin MSOP ePAD package. The MIC2159 switches at 400kHz, allowing the smallest possible external components and is designed to drive loads up to 30A. The devices feature high output driver capability, combined with an all n-channel synchronous architecture.

The MIC2159 operates from a 3V to 14.5V input and can be configured to generate output voltages as low as 0.8V. Efficiencies of over 95% can be achieved within the smallest possible printed circuit board space area.

The MIC2159 is available in a thermally capable 10-pin ePAD MSOP package, with an junction operating range from –40°C to +125°C.

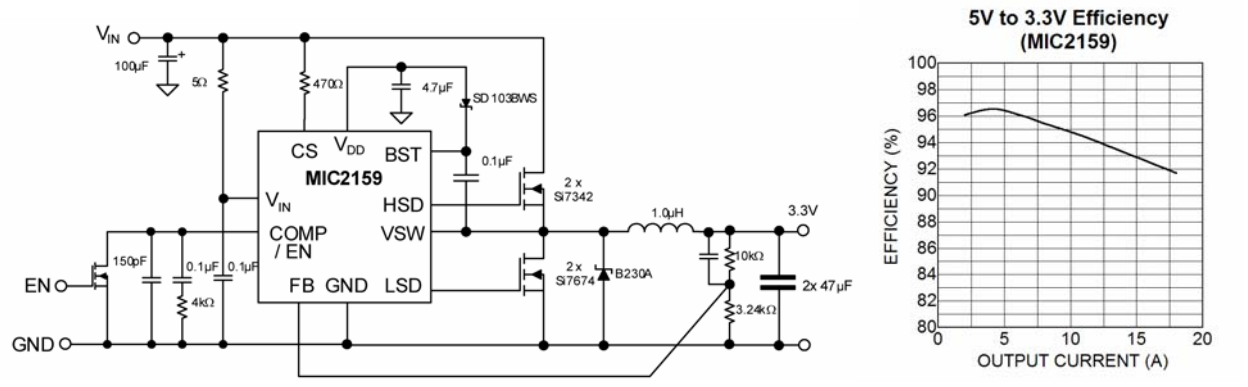
Features

- Small footprint 10-lead ePAD MSOP
- 3V to 14.5V input voltage range
- Adjustable output voltage down to 0.8V
- 400KHz operation
- Drives two n-channel MOSFETs
  - Built-in 3Ω drivers
- Simple control: voltage-mode PWM
- Fast transient response
  - Transient Hysteretic control
  - Externally compensated
- Over-current protection
- Hiccup mode short-circuit protection
- Dual function COMP & EN pin
  - I_{SD} = 50µA
- Short minimum ON time
  - 30ns
  - Very low duty cycle possible

Applications

- Point-of-Load DC/DC conversion
- High Current Power Supplies
- Telecom/datacom and Networking Power Supplies
- Servers and Workstations
- Graphics Cards and other PC Peripherals

Typical Application

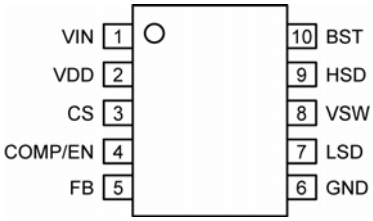


MIC2159 Adjustable Output 400kHz Converter

Ordering Information

Part Number	Output Voltage	Frequency	Juction Temperature Range	Package
MIC2159YMME	Adj	400KHz	-40°C to +125°C	10-lead ePAD MSOP

Pin Configuration



10-lead e-PAD MSOP (MME)

Pin Description

Pin Number (MSOP-10)	Pin Name	Pin Function
1	V_{IN}	Supply voltage (Input): 3V to 14.5V
2	V_{DD}	5V Internal Linear Regulator (Output): V_{DD} is the external MOSFET gate drive supply voltage and an internal supply bus for the IC. When Vin is ≤5V, V_{DD} should be connected to Vin.
3	CS	Current Sense. Current-limit comparator non-inverting input. The current limit is sensed across the FET during the ON time. The current can be set by the resistor in series with the CS pin.
4	COMP/EN	Compensation (Input): Dual function pin. Pin for external compensation. If this pin is pulled below 0.2V, with the reference fully up the device shuts down (50μA typical current draw)
5	FB	Feedback (Input): Input to error amplifier. Regulates error amplifier to 0.8V.
6	GND	Ground (Return)
7	LSD	Low-Side Drive (Output): High-current driver output for external synchronous MOSFET.
8	VSW	Switch (Return): High-side MOSFET driver return
9	HSD	High-Side Drive (Output): High current output-driver for the high-side MOSFET. When Vin is below 5v, 2.5v threshold FETs should be used. At Vin > 5V, 4.5V threshold FETs should be used.
10	BST	Boost (Input): Provides the drive voltage for the high-side MOSFET driver. The gate drive voltage is higher than the source voltage by V_{IN} minus a diode drop.

Absolute Maximum Rating[1]

Supply Voltage (V_{IN}) 15.5V
Booststrapped Voltage (V_{BST}) ..... V_{IN} +5V
Junction Temperature Range..... –40°C ≤ T_J ≤ +125°C
Ambient Storage Temp ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage..... +3V to +14.5V
Output Voltage Range .....0.8V to V_{IN}*D_{MAX}
Package Thermal Resistance
θ_{JA} 10-lead ePAD MSOP..... 63°C/W

Electrical Characteristics

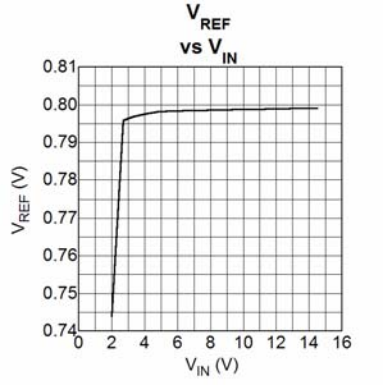
Tj = 25ºC, **bold** values indicate -40ºC<Tj<+125ºC; Vin = 5V; unless otherwise specified

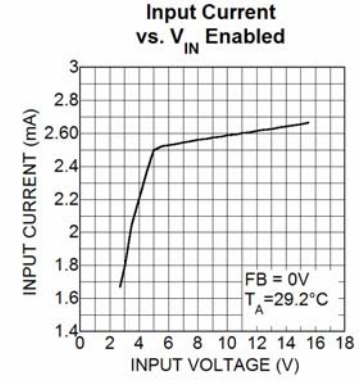
Parameter	Condition	Min	Typ	Max	Units
Regulation					
Feedback Voltage Reference	(+/- 1%)	0.792	0.8	0.808	V
Feedback Voltage Reference	(+/- 2% over temp)	**0.784**	0.8	**0.816**	V
Feedback Bias Current			150	350	nA
Output Voltage Line Regulation			0.03		% / V
Output Voltage Load Regulation			0.5		%
Output Voltage Total Regulation	3V ≤ VIN ≤ 14.5V; 1A ≤ IOUT ≤ 10A (VOUT = 2.5V) Note 3		0.6	**1.5**	%
Oscillator Section					
Oscillator Frequency		350	400	450	kHz
Maximum Duty Cycle		92			%
Minimum On-Time	Note 3		30	**60**	ns
Input and VDD Supply					
PWM mode supply current	$V_{CS/EN}$ =Vin- 0.25V; V_{FB} = 0.7V (output switching but excluding external MOSFET gate current.)		1.6	**3**	mA
Shutdown Quiescent Current (MSOP-10)	V_{COMP} = 0V		50	**150**	µA
V_{COMP} Shutdown Threshold (MSOP-10)		0.1	0.25	0.35	V
V_{COMP} Shutdown Blanking Period (MSOP-10)		1	4	**8**	ms
Digital Supply Voltage (V_{DD})	V_{IN} >6V	4.7	5	5.3	V
Error Amplifier					
DC Gain			70		dB
Transconductance			1.4		mS
Soft Start					
Soft Start Current	After time out of internal timer	-13	9	-4	µA
Current Sense					
Current Sense Over Current Trip Point		135	200	275	µA

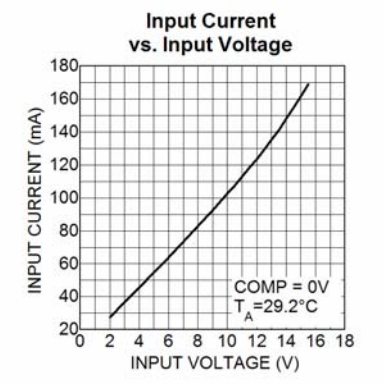
Temperature Coefficient			2300		ppm/°C
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Units**
Output Fault Correction Thresholds					
Upper Threshold, V_{FB_OVT}		2	3.5	5	%
Lower Threshold, V_{FB_UVT}		-2	-3.5	-5	%
Gate Drivers					
Rise/Fall Time	Into 3000pF at V_{IN} > 5V		15		ns
Output Driver Impedance	Source, V_{IN}= 4.5V		2.5	3	Ω
	Sink, V_{IN} = 4.5V		2.5	3	
	Source, V_{IN}= 3V		3	4	
	Sink, V_{IN} = 3V		3	4	
Driver Non-overlap Time	Note 3		50		ns

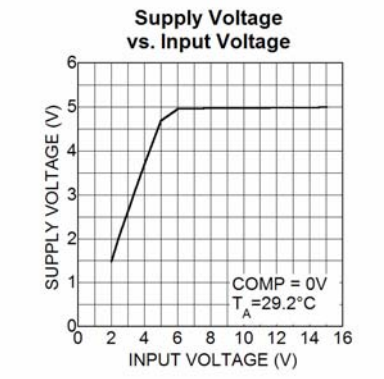
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Guaranteed by design
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.

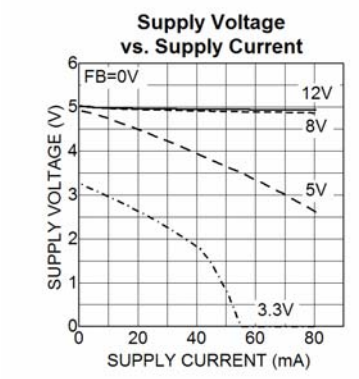
Typical Characteristics

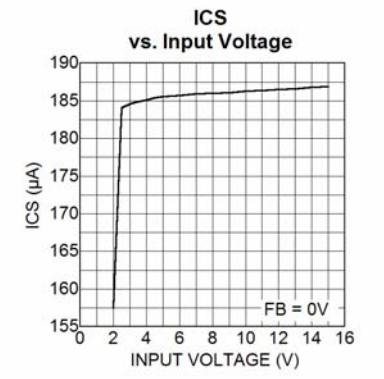


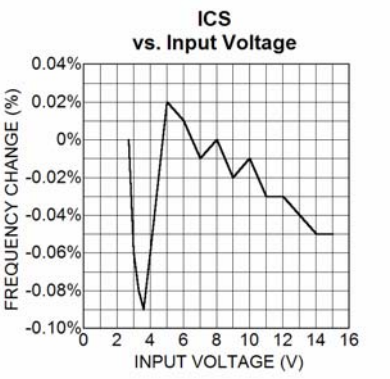




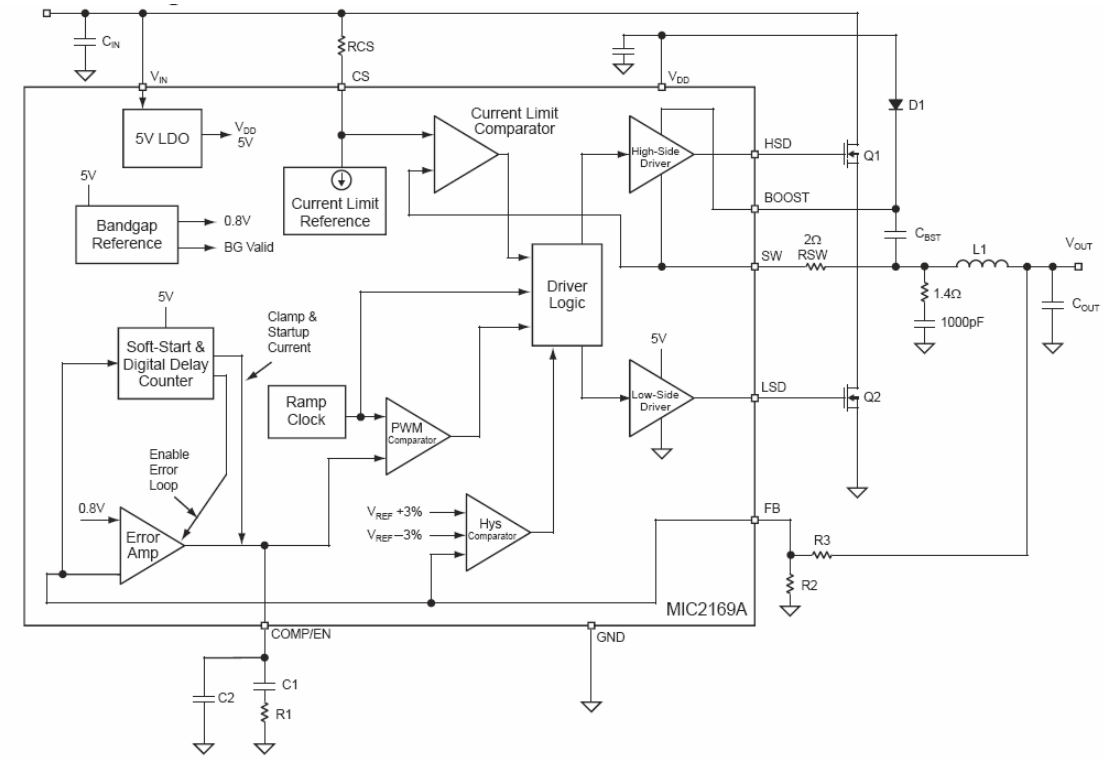








Block Diagram



MIC2159 Block Diagram

Functional Description

The MIC2159 is a voltage mode, synchronous step-down switching regulator controller designed for high power. Current limit is implemented without the use of an external sense resistor. It includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time, a PWM generator, a reference voltage, two MOSFET drivers, and short-circuit current limiting circuitry to form a complete 400kHz switching regulator.

Theory of Operation

The MIC2159 is a voltage mode step-down regulator. The figure above illustrates the block diagram for the voltage control loop. The output voltage variation due to load or line changes will be sensed by the inverting input of the transconductance error amplifier via the feedback resistors R3, and R2 and compared to a reference voltage at the non-inverting input. This will cause a small change in the DC voltage level at the output of the error amplifier which is the input to the PWM comparator. The other input to the comparator is a 1v triangular waveform. The comparator generates a rectangular waveform whose width tON is equal to the time from the start of the clock cycle t0 until t1, the time the triangle crosses the output waveform of the error amplifier. To illustrate the control loop, assume the output voltage drops due to sudden load turn-on, this would cause the inverting input of the error amplifier, which is the divided down version of VOUT, to be slightly less than the reference voltage, causing the output voltage of the error amplifier to go high. This will cause the PWM comparator to increase t_{ON} time of the top side MOSFET, causing the output voltage to go up and bringing VOUT back in regulation. If this sudden load transient was large enough to cause a 3% change in output voltage, then the output of the Hysteretic comparator will bypass the PWM comparator and drive the LSD and HSD outputs at full Duty cycle in order to recover the nominal output voltage in the fastest manner possible whilst fixed frequency PWM switching is maintained during normal loading.

Soft-Start

The COMP/EN pin on the MIC2159 is used for the following three functions:

1. Disables the part by grounding this pin.
2. External compensation to stabilize the voltage control loop.

3. Soft-start.

For better understanding of the soft-start feature, assume VIN = 12V and the MIC2159 is allowed to power-up by un-grounding the COMP/EN pin. The COMP pin has an internal 8.5µA current source that charges the external compensation capacitor. As soon as this voltage rises to 180mV (t = Cap_COMP × 0.18V/8.5µA), the MIC2159 allows the internal VDD linear regulator to power up and as soon as it crosses the under-voltage lockout of 2.6V, the chip's internal oscillator starts switching. At this point in time, the COMP pin current source increases to 40µA and an internal 12-bit counter starts counting, which takes approximately 2ms to complete. During counting, the COMP voltage is clamped at 0.65V. After this counting cycle the COMP current source is reduced to 8.5µA and the COMP pin voltage rises from 0.65V to 0.95V, the bottom edge of the saw-tooth oscillator. This is the beginning of 0% duty cycle and it increases slowly causing the output voltage to rise slowly. The MIC2159 has two hysteretic comparators that are enabled when VOUT is outside ±3% of steady state. When the output voltage reaches 97% of programmed output voltage then the gm error amplifier is enabled along with the hysteretic comparator. From this point onwards, the voltage control loop (gm error amplifier) is fully in control and will regulate the output voltage. Soft-start time can be calculated approximately by adding the following four time frames:

t1 = Cap_COMP × 0.18V/8.5µA

t2 = internal counter, approx 2ms

t3 = Cap_COMP × 0.3V/8.5µA

$$t4 = \frac{V_{OUT} \cdot 0.5 \cdot Cap\_COMP}{V_{IN} \cdot 8.5\mu.}$$

Soft-Start Time(Cap_COMP=100nF) = t1 + t2 + t3 + t4 = 2.1ms + 2ms + 3.5ms + 1.8ms = 10ms

Current Limit

The MIC2159 uses the RDS(ON) of the top power MOSFET to measure output current. Since it uses the drain to source resistance of the power MOSFET, it is not very accurate. This MOSFET scheme is adequate to protect the power supply and external components during a fault condition by cutting back the time the top MOSFET is on if the feedback voltage is greater than 0.67V. In case of a hard short when feedback voltage is less than 0.67V, the MIC2159 discharges the COMP capacitor to 0.65V, resets the digital counter and automatically shuts off the top gate drive, and the gm error amplifier and the +/- 3% hysteretic comparators are completely disabled and the soft-start cycles restarts. This mode of operation is called the "hiccup mode" and its purpose is to protect the down stream load in case of a hard short. The circuit in Figure 1 illustrates the MIC2159 current limiting circuit.

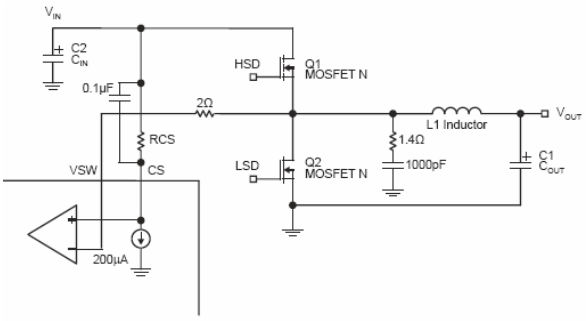


Figure 1. MIC2159 Current Limiting Circuit

The current limiting resistor RCS is calculated by the following equation:

$$R_{CS} = \frac{R_{DS(ON)} \cdot I_L}{200\mu A} \qquad \text{Equation (1)}$$

$$I_L = I_{LOAD} + \frac{1}{2} \cdot I_{RIPPLE}$$

Where:

$$I_{RIPPLE} = V_{OUT} \cdot \frac{V_{IN} - V_{OUT}}{V_{IN} \cdot F_{SWITCHING} \cdot L}$$

$F_{SWITCHING}$ = 400kHz

200µA is the internal sink current to program the MIC2159 current limit.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to the load current (I_{LOAD}) in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect RCS resistor directly to the drain of the top MOSFET Q1, and the RSW resistor to the source of Q1 to accurately sense the MOSFETs $R_{DS(ON)}$. To make the MIC2159 insensitive to board layout and noise generated by the switch node, a 1.4Ω resistor and a 1000pF capacitor is recommended between the switch node and GND. A 0.1µF capacitor in parallel with RCS should be connected to filter some of the switching noise.

Internal VDD Supply

The MIC2159 controller internally generates VDD for self biasing and to provide power to the gate drives. This VDD supply is generated through a low-dropout regulator and generates 5V from VIN supply greater than 5V. For supply voltage less than 5V, the VDD linear regulator is approximately 200mV in dropout. Therefore, it is recommended to short the VDD supply to the input supply through a 5Ω resistor for input supplies between

2.9V to 5V.

MOSFET Gate Drive

The MIC2159 high-side drive circuit is designed to switch an N-Channel MOSFET. The Functional Block Diagram shows a bootstrap circuit, consisting of D1 and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} circuit is charged while the low-side MOSFET is on and the voltage on the VSW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the MOSFET turns on, the voltage on the VSW pin increases to approximately VIN. Diode D1 is reversed biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. When the low-side switch is turned back on, C_{BST} is recharged through D1. The drive voltage is derived from the internal 5V V_{DD} bias supply. The nominal low-side gate drive voltage is 5V and the nominal high-side gate drive voltage is approximately 4.5V due the voltage drop across D1. An approximate 50ns delay between the low-side(off) to high-side(on) driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs (shoot-through). Adaptive gate drive is implemented on the high-side(off) to low-side(on) driver transition to reduce losses in the flywheel diode and to prevent shoot-through. This is operated by detecting the VSW pin; once this pin is detected to reach 1.5v, the high-side MOSFET can be assumed to be off and the low side driver is enabled.

Application information

MOSFET Selection

The MIC2159 controller works from input voltages of 3V to 14.5V and has an internal 5V regulator to provide power to turn the external N-Channel power MOSFETs for high- and low-side switches. For applications where V_{IN} < 5V, the internal V_{DD} regulator operates in dropout mode, and it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for V_{GS} of 2.5V. For applications when VIN > 5V; logic-level MOSFETs, whose operation is specified at VGS = 4.5V must be used. For the lower (<5v) applications, the V_{DD} supply can be connected directly to Vin to help increase the driver voltage to the MOSFET.

It is important to note the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current-sense (CS) resistor. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2159 gate-drive circuit. At 400kHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2159. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$I_{G[high\text{-}side]}(avg)=Q_G \times F_S$

Where:

$I_{G[high\text{-}side]}(avg)$=Average high-side MOSFET gate current

Q_G = total gate charge for the high-side MOSFET taken from manufacturer's data sheet for VGS = 5V.

F_S = Switching Frequency (400kHz)

The low-side MOSFET is turned on and off at VDS = 0 because the freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$I_{G[low\text{-}side]}(avg) = C_{ISS} \times V_{GS} \times F_S$

Since the current from the gate drive comes from the input voltage, the power dissipated in the MIC2159 due to gate drive is:

$$P_{GATEDRIVE} = V_{IN}.(I_{G[high\text{-}sde]}(avg) + I_{G[low\text{-}side]}(avg))$$

A convenient figure of merit for switching MOSFETs is the on resistance times the total gate charge $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2159.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the top and bottom MOSFET are essentially equal to the input voltage. A safety factor of 20% should be added to the V_{DS}(max) of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

Where:

$$P_{CONDUCTION} = I_{SW(RMS)}{}^2 \cdot R_{SW}$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)}$$

R_{SW} = on-resistance of the MOSFET switch

$$D = duty\_cyle = \frac{V_{OUT}}{V_{IN}}$$

Making the assumption the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \cdot V_{GS} \cdot C_{OSS} \cdot V_{IN}}{I_G}$$

where:

CISS and COSS are measured at VDS = 0

IG = gate-drive current (1.4A for the MIC2159)

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{IN} + V_D) \cdot I_{PK} \cdot t_T \cdot F_S$$

Where:

t_T = Switching transition time (~20ns)

V_D = Freewheeling diode drop (0.5v)

F_S = Switching Frequency (400kHz)

The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher

inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by the equation below.

$$L = \frac{V_{OUT} \cdot (V_{IN(\max)} - V_{OUT})}{V_{IN(\max)} \cdot F_S \cdot 0.2 \cdot I_{OUT(\max)}}$$

where:

F_S = switching frequency, 400 kHz

0.2 = ratio of AC ripple current to DC output current

V_{IN}(max) = maximum input voltage

The peak-to-peak inductor current (AC ripple current) is:

$$I_{PP} = \frac{V_{OUT} \cdot (V_{IN(\max)} - V_{OUT})}{V_{IN(\max)} \cdot F_S \cdot L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor ripple current.

$I_{PK} = I_{OUT(max)} + 0.5 \times I_{PP}$

The RMS inductor current is used to calculate the I2R losses in the inductor.

$$I_{INDUCTOR} = I_{OUT(\max)} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{I_{PK}}{I_{OUT(\max)}} \right)^2}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2159 requires the use of ferrite materials for all but the most cost sensitive applications.

Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTOR_{Cu}} = I_{INDUCTOR(rms)}^2 \cdot R_{WINDING}$$

The resistance of the copper wire, RWINDING, increases with temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING(hot)} = R_{WINDING(20^oC)} \cdot (1 + 0.0042 \cdot (T_{HOT} - T_{20^oC}))$$

Where:

T_{HOT} = temperature of wire under full load

T_{20^oC} = ambient temperature

$R_{WINDING(20^oC)}$ = room temperature winding resistance (usually specified by manufacturer)

Output Capacitor Selection

The output capacitor values are usually determined by the capacitors ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminium electrolytic, and POSCAPS. The output capacitor's ESR is usually the main cause of output ripple. The output capacitor ESR also affects the overall voltage feedback loop from a stability point of view. See "Feedback Loop Compensation" section for more information. The maximum value of ESR is calculated:

$$R_{ESR} \le \frac{\Delta V_{OUT}}{I_{PP}}$$

Where:

V_{OUT} = peak-to-peak output voltage ripple

I_{PP} = peak-to-peak inductor ripple current

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP} \cdot (1 - D)}{C_{OUT} \cdot F_S} \right)^2 + (I_{PP} \cdot R_{ESR})^2}$$

Where:

D = duty cycle

C_{OUT} = output capacitance value

f_S = switching frequency

The voltage rating of the capacitor should be twice the voltage for a tantalum and 20% greater for aluminium electrolytic. The output capacitor RMS current is calculated below:

$$I_{C_{OUT(rms)}} = \frac{I_{PP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{COUT(rms)}^2 \cdot R_{ESR(C_{OUT})}$$

Note that ∆Vout should be kept within the +/- 3% of nominal limits to prevent the loop switching between hysteretic and voltage mode control.

Input Capacitor Selection

The input capacitor should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least 2 times the maximum input voltage to maximize reliability. Aluminium electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{INDUCTOR(peak)} \cdot R_{ESR(C_{IN})}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor ripple current is low:

$$I_{C_{IN}(rms)} \approx I_{OUT(\max)} \cdot \sqrt{D \cdot (1-D)}$$

The power dissipated in the input capacitor is:

$$P_{DISS(C_{IN})} = I_{C_{IN}(rms)}^{2} . R_{ESR(C_{IN})}$$

Voltage Setting Components

The MIC2159 requires two resistors to set the output voltage as shown in Figure 2.

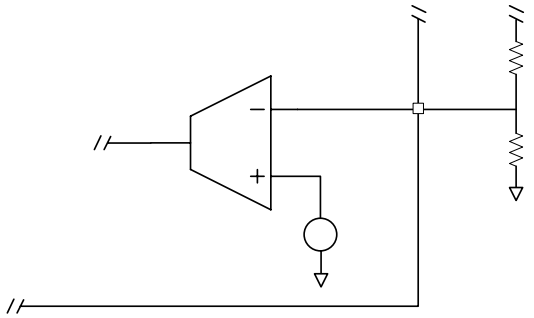


Figure 2. Voltage-Divider Configuration

The output voltage is determined by the equation:

$$V_O = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right)$$

A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \cdot R1}{V_O - V_{REF}}$$

External Schottky Diode

An external freewheeling diode is used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead time prevents current from flowing unimpeded through both MOSFETs and is typically ~50ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

$$I_{D(avg)} = I_{OUT} \cdot 2 \cdot 50ns \cdot F_S$$

The reverse voltage requirement of the diode is:

V_{DIODE}(rrm) = VIN

The power dissipated by the Schottky diode is:

$P_{DIODE} = I_D(avg) \times V_F$

Where:

V_F = forward voltage at the peak diode current

The external Schottky diode, D1, is not necessary for circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on. An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending on the circuit components and operating conditions, an external Schottky diode will give a 1/2% to 1% improvement in efficiency.

Feedback Loop Compensation

The MIC2159 controller comes with an internal transconductance error amplifier used for compensating the voltage feedback loop by placing a capacitor (C1) in series with a resistor (R1) and another capacitor C2 in parallel from the COMP pin to ground. See "MIC2159 Block Diagram."

Power Stage

The power stage of a voltage mode controller has an inductor, L1, with its winding resistance (DCR)

connected to the output capacitor, COUT, with its electrical series resistance (ESR) as shown in Figure 3. The transfer function G(s), for such a system is:

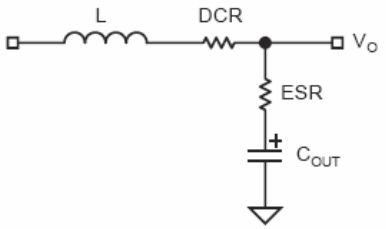


Figure 3. The Output LC Filter in a voltage Mode Buck Converter

$$G(s) = \frac{1 + ESR \cdot s \cdot C_{OUT}}{s(DCR \cdot C_{OUT} + ESR \cdot C_{OUT}) + s^2(L \cdot C_{OUT}) + 1}$$

Plotting this transfer function with the following assumed values (L=2 µH, DCR=0.009Ω, COUT=1000µF, ESR=0.050Ω) gives lot of insight as to why one needs to compensate the loop by adding resistor and capacitors on the COMP pin. Figures 4 and 5 show the gain curve and phase curve for the above transfer function.

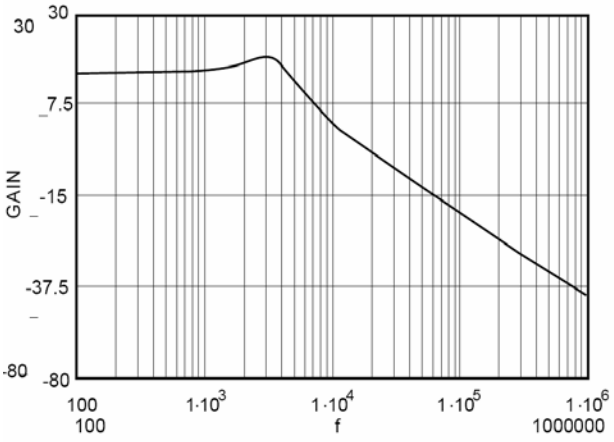


Figure 4. The Gain Curve for G(s)

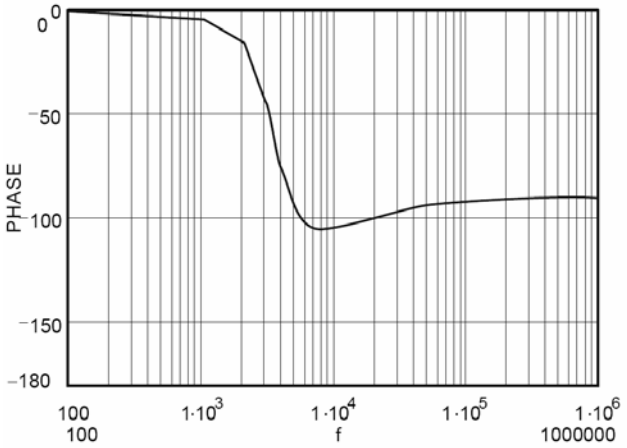


Figure 5. Phase Curve for G(s)

It can be seen from the transfer function G(s) and the gain curve that the output inductor and capacitor create a two pole system with a break frequency at:

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}}$$

Therefore, fLC = 3.6kHz

By looking at the phase curve, it can be seen that the output capacitor ESR (0.050Ω) cancels one of the two system poles (LCOUT) by introducing a zero at:

$$f_{ZERO} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

Therefore, FZERO = 6.36kHz.

From the point of view of compensating the voltage loop, it is recommended to use higher ESR output capacitors since they provide a 90° phase gain in the power path. For comparison purposes, Figure 6, shows the same phase curve with an ESR value of 0.002Ω.

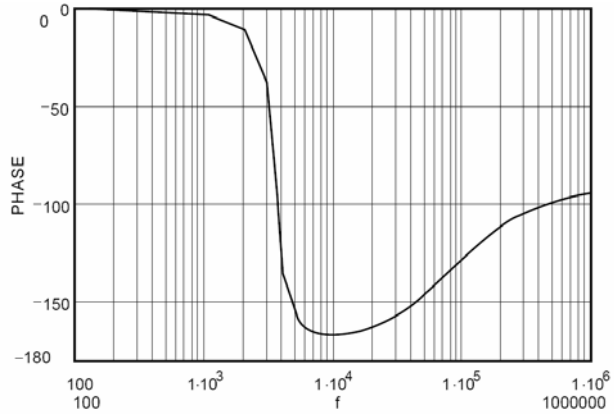


Figure 6. The Phase Curve with ESR = 0.002Ω

It can be seen from Figure 5 that at 50 kHz, the phase is approximately –90° versus Figure 6 where the number is –150°. This means that the transconductance error amplifier has to provide a phase boost of about 45° to achieve a closed loop phase margin of 45° at a crossover frequency of 50kHz for Figure 4, versus 105° for Figure 6. The simple R1,C1 and C2 compensation scheme allows a maximum error amplifier phase boost of about 90°. Therefore, it is easier to stabilize the MIC2169A voltage control loop by using high ESR value output capacitors.

g_m Error Amplifier

It is undesirable to have high error amplifier gain at high frequencies because high frequency noise spikes would be picked up and transmitted at large amplitude to the output, thus, gain should be permitted to fall off at high frequencies. At low frequency, it is desired to have high open-loop gain to attenuate the power line ripple. Thus, the error amplifier gain should be allowed to increase rapidly at low frequencies.

The transfer function with R1, C1, and C2 for the internal gm error amplifier can be approximated by the following equation:

$$Error\_Amplifier(z) = g_m \cdot \left[\frac{1+R1 \cdot S \cdot C1}{S \cdot (C1+C2) \cdot \left(1+R1 \cdot \frac{C1 \cdot C2 \cdot S}{C1+C2}\right)} \right]$$

The above equation can be simplified by assuming C2<<C1,

$$Error\_Amplifier\ (z) = g_m \cdot \left[\frac{1+R1 \cdot S \cdot C1}{S \cdot (C1) \cdot (1+R1 \cdot C2 \cdot S)} \right]$$

From the above transfer function, one can see that R1 and C1 introduce a zero and R1 and C2 a pole at the following frequencies:

F_{zero}= 1/2 π × R1 × C1

F_{pole} = 1/2 π × C2 × R1

$F_{pole@origin}$ = 1/2 π × C1

Figures 7 and 8 show the gain and phase curves for the above transfer function with R1 = 9.3k, C1 = 1000pF, C2 = 100pF, and gm = .005Ω–1. It can be seen that at 50 kHz, the error amplifier exhibits approximately 45° of phase margin.

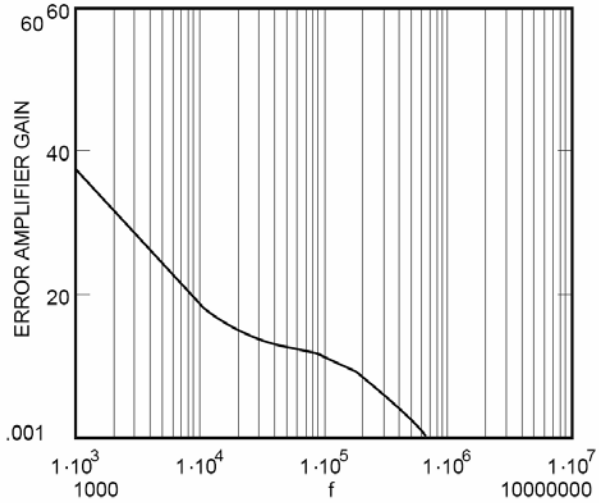


Figure 7. Error Amplifier Gain Curve

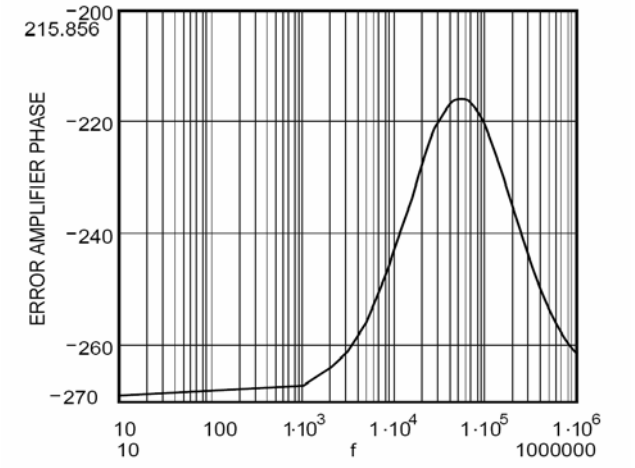


Figure 8. Error Amplifier Phase Curve

Total Open-Loop Response

The open-loop response for the MIC2159 controller is easily obtained by adding the power path and the error amplifier gains together, since they already are in Log scale. It is desirable to have the gain curve intersect zero dB at tens of kilohertz, this is commonly called crossover frequency; the phase margin at crossover frequency should be at least 45°. Phase margins of 30° or less cause the power supply to have substantial ringing when subjected to transients, and have little tolerance for component or environmental variations.

Figures 9 and 10 show the open-loop gain and phase margin and it can be seen from Figure 9 that the gain curve intersects the 0dB at approximately 50kHz, and from Figure 10 that at 50kHz, the phase shows approximately 50° of margin.

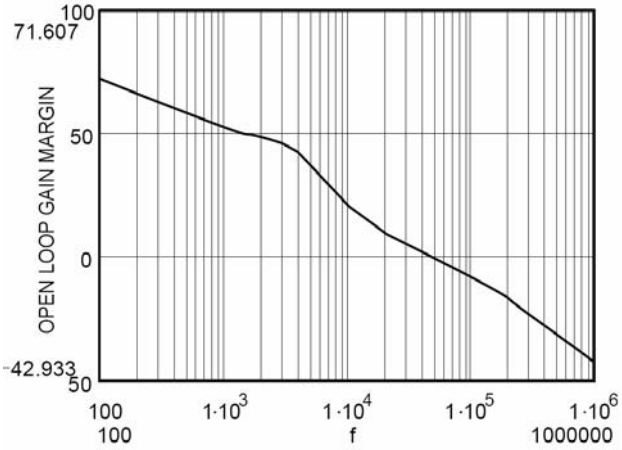


Figure 9. Open-Loop Gain Margin

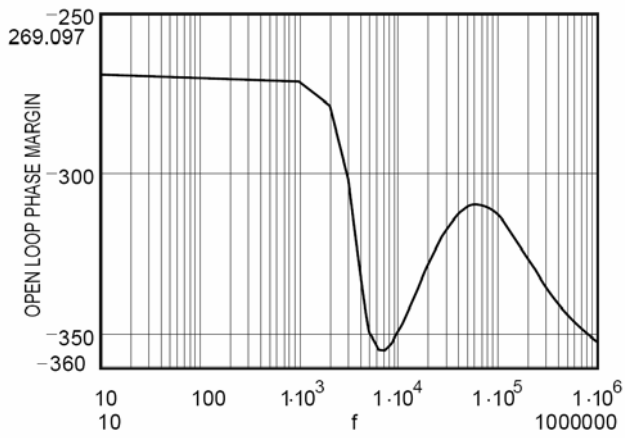


Figure 10. Open-Loop Phase Margin

Design Example

Layout and Checklist:

1. Connect the current limiting resistor directly to the drain of top MOSFET.

2. Use a resistor from the input supply to the VIN pin on the MIC2159. Also, place a 1µF ceramic

Capacitor from this pin to GND, preferably not thru a via.

3. The feedback resistors should be placed close to the FB pin. The top side of the resistor should connect directly to the output node. Run this trace away from the switch node. The bottom side of the lower resistor should connect to the GND pin on the MIC2159.

4. The compensation resistor and capacitors should be placed right next to the COMP pin and the other side should connect directly to the GND pin on the MIC2159 rather than going to the plane.

5. Add a 1.4Ω resistor and a 1000pF capacitor from the switch node to ground pin. See page 7, Current Limiting section for more detail.

6. Add place holders for gate resistors on the top and bottom MOSFET gate drives. If necessary, gate resistors of 5Ω or less should be used.

7. Low gate charge MOSFETs should be used to maximize efficiency.

8. Compensation component GND, feedback resistor ground, chip ground should all run together and connect to the output capacitor ground. See demo board layout, bottom layer.

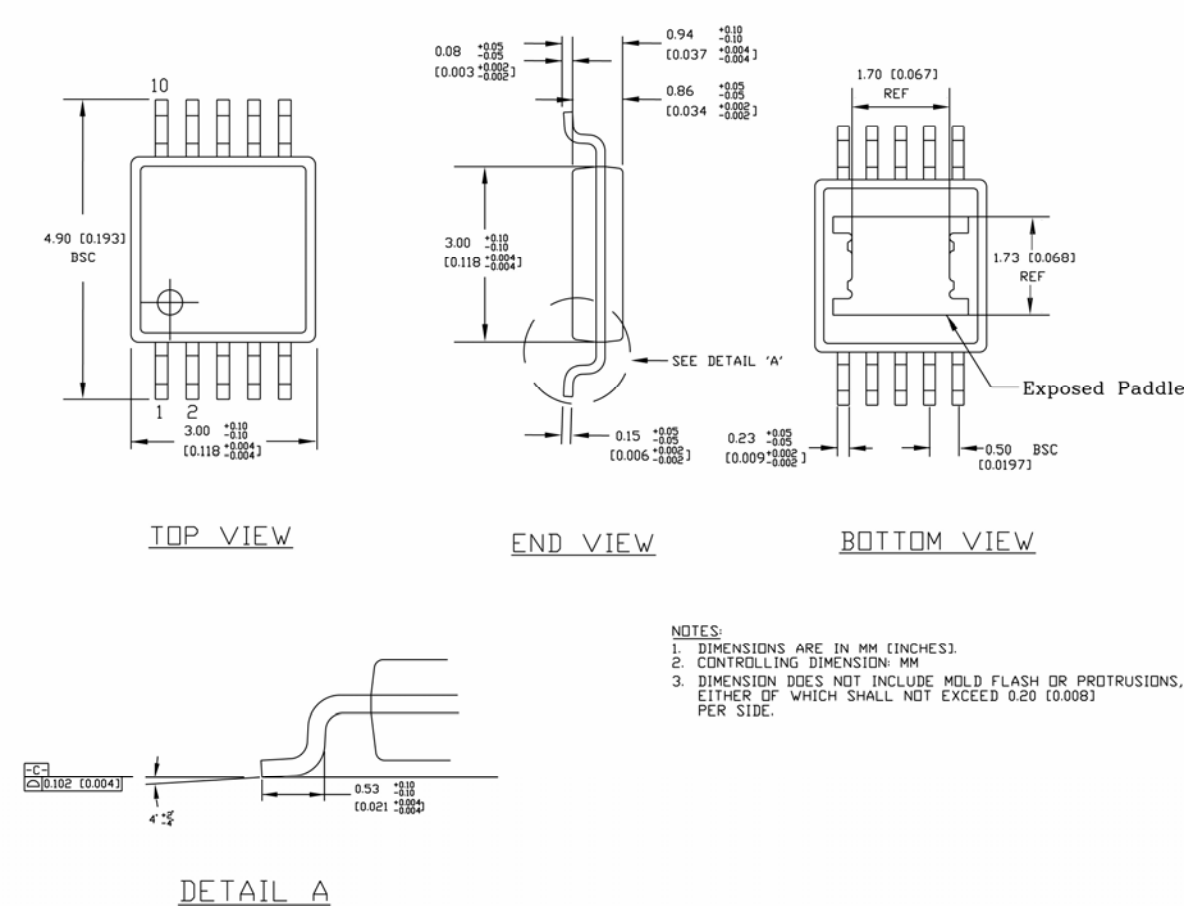
9. The 10µF ceramic capacitor should be placed between the drain of the top MOSFET and the source of the bottom MOSFET.

10. The 10µF ceramic capacitor should be placed right on the VDD pin without any vias.

11. The source of the bottom MOSFET should connect directly to the input capacitor GND with a thick trace. The output capacitor and the input capacitor should connect directly to the GND plane.

12. Place a 0.01µF to 0.1µF Ceramic capacitor in parallel with the CS resistor to filter any switching noise.

Package Drawing



10-Lead e-PAD MSOP (MME)

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Revision History

Date	Revision	Edits by:	Description of Change
	1.0		Initial Spec
6/15/06	1.1	M. Mclean	Coversion to Micrel Format