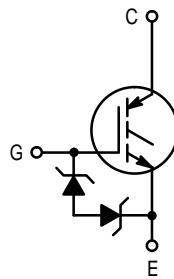


Product Preview

Insulated Gate Bipolar Transistor
N-Channel Enhancement-Mode Silicon Gate

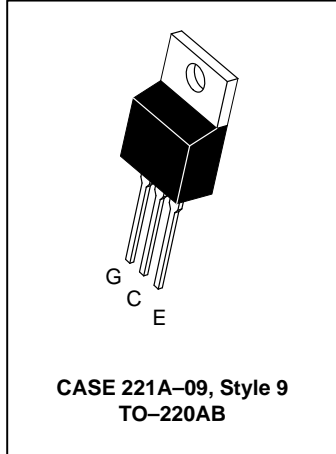
This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. It also provides fast switching characteristics and results in efficient operation at high frequencies.

- Industry Standard TO-220 Package
- High Speed E_{off} : 67 μ J/A typical at 125°C
- Low On-Voltage – 1.7 V typical at 8.0 A, 125°C
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes



MGP15N60U

IGBT IN TO-220
15 A @ 90°C
26 A @ 25°C
600 VOLTS
VERY LOW
ON-VOLTAGE



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	600	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0\text{ M}\Omega$)	V_{CGR}	600	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$ — Continuous @ $T_C = 90^\circ\text{C}$ — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	26 15 30	Adc Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	200	°C
Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage (V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positive)	V _{(BR)CES}	600 —	— 870	— —	Vdc mV/°C
Emitter-to-Collector Breakdown Voltage (V _{GE} = 0 Vdc, I _{EC} = 100 mAdc)	V _{(BR)ECS}	15	—	—	Vdc
Zero Gate Voltage Collector Current (V _{CE} = 600 Vdc, V _{GE} = 0 Vdc) (V _{CE} = 600 Vdc, V _{GE} = 0 Vdc, T _J = 125°C)	I _{CES}	— —	— —	10 200	μAdc
Gate-Body Leakage Current (V _{GE} = ± 20 Vdc, V _{CE} = 0 Vdc)	I _{GES}	—	—	50	μAdc

ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage (V _{GE} = 15 Vdc, I _C = 4.0 Adc) (V _{GE} = 15 Vdc, I _C = 4.0 Adc, T _J = 125°C) (V _{GE} = 15 Vdc, I _C = 8.0 Adc)	V _{CE(on)}	— — —	1.4 1.3 1.7	1.7 — 2.0	Vdc
Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	3.0 —	5.5 10	7.0 —	Vdc mV/°C
Forward Transconductance (V _{CE} = 10 Vdc, I _C = 8.0 Adc)	g _{fe}	—	7.0	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	806	—	pF
Output Capacitance		C _{oes}	—	78	—	
Transfer Capacitance		C _{res}	—	13	—	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{CC} = 360 Vdc, I _C = 8.0 Adc, V _{GE} = 15 Vdc, L = 300 μH, R _G = 20 Ω, T _J = 25°C) Energy losses include "tail"	t _{d(on)}	—	35	—	ns
Rise Time		t _r	—	34	—	
Turn-Off Delay Time		t _{d(off)}	—	105	—	
Fall Time		t _f	—	200	—	
Turn-Off Switching Loss		E _{off}	—	250	—	
Turn-On Delay Time	(V _{CC} = 360 Vdc, I _C = 8.0 Adc, V _{GE} = 15 Vdc, L = 300 μH, R _G = 20 Ω, T _J = 125°C) Energy losses include "tail"	t _{d(on)}	—	36	—	ns
Rise Time		t _r	—	39	—	
Turn-Off Delay Time		t _{d(off)}	—	206	—	
Fall Time		t _f	—	255	—	
Turn-Off Switching Loss		E _{off}	—	510	—	
Gate Charge	(V _{CC} = 360 Vdc, I _C = 8.0 Adc, V _{GE} = 15 Vdc)	Q _T	—	39.2	—	nC
		Q ₁	—	8.7	—	
		Q ₂	—	17.4	—	

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L _E	—	7.5	—	nH
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(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

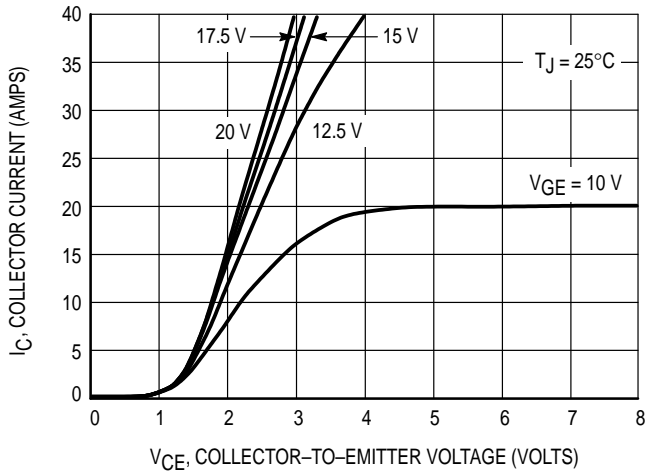


Figure 1. Output Characteristics

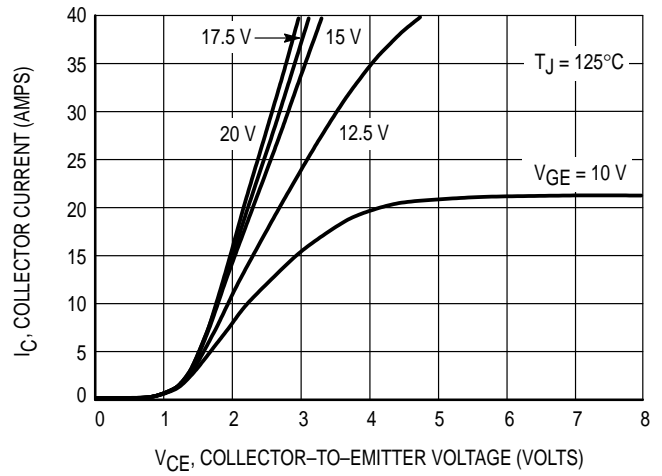


Figure 2. Output Characteristics

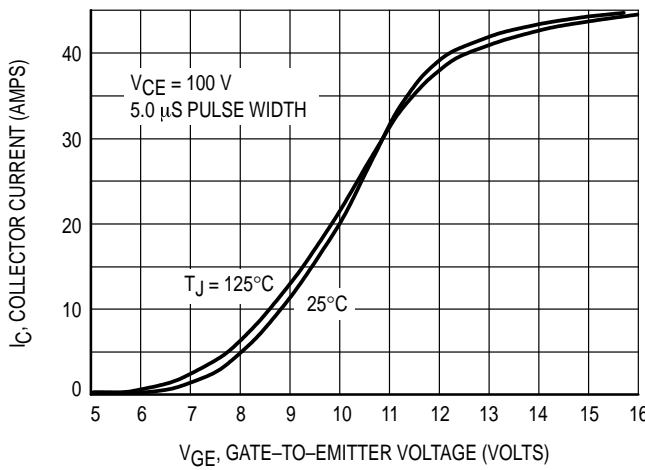


Figure 3. Transfer Characteristics

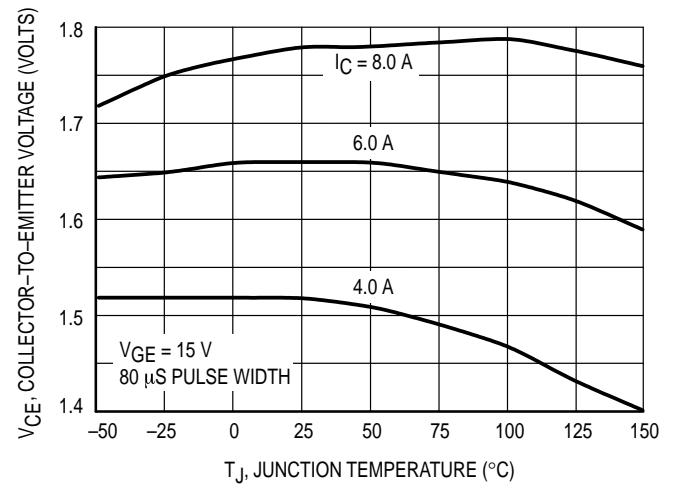


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

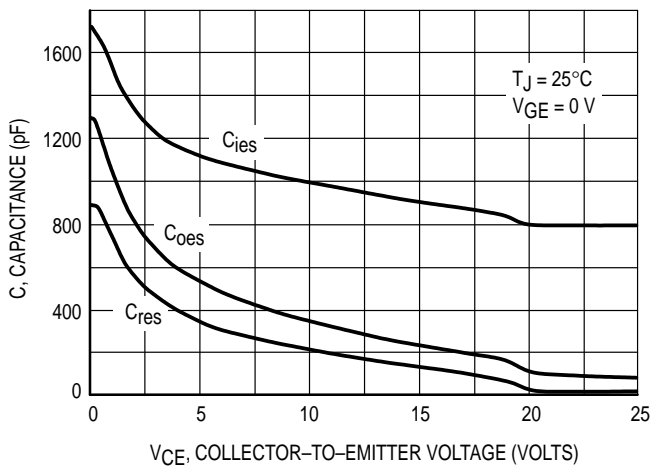


Figure 5. Capacitance Variation

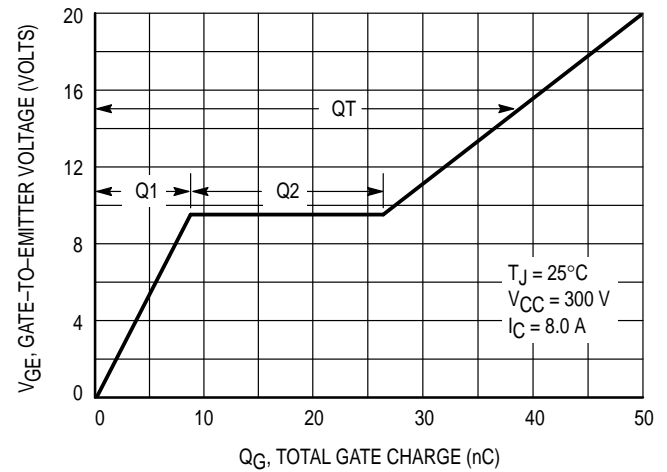


Figure 6. Gate-to-Emitter Voltage versus Total Charge

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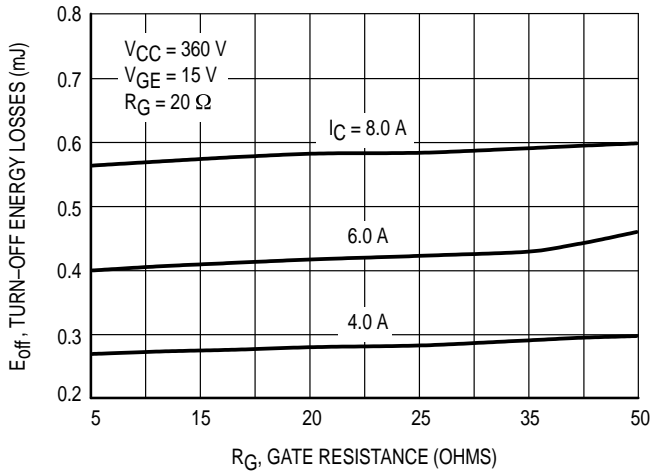


Figure 7. Turn-Off Losses versus Gate Resistance

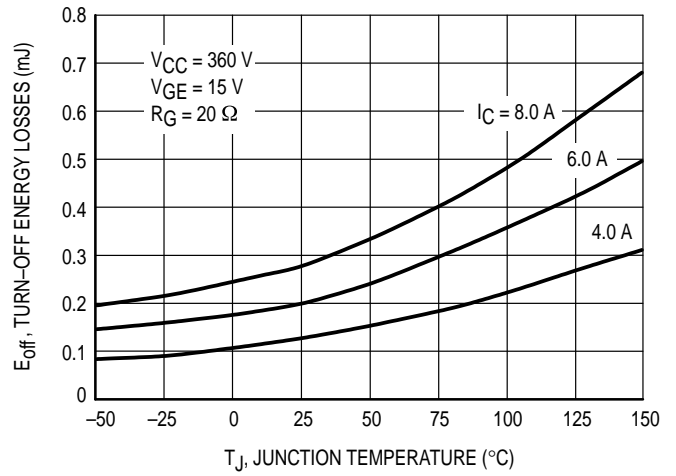


Figure 8. Turn-Off Losses versus Junction Temperature

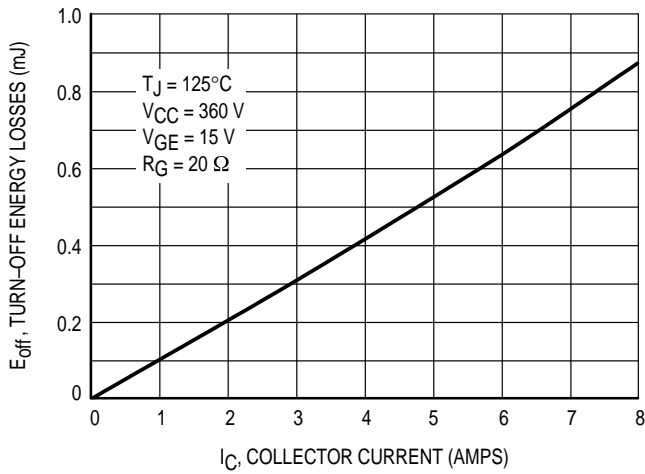


Figure 9. Turn-Off Losses versus Collector Current

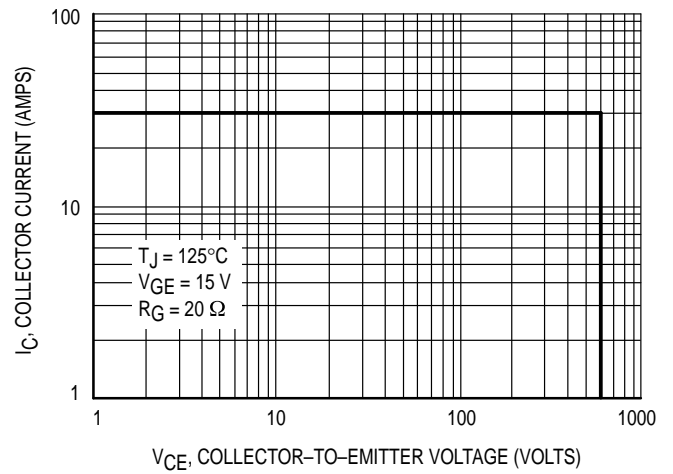
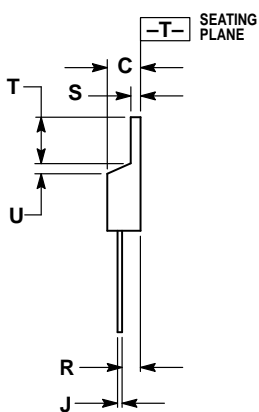
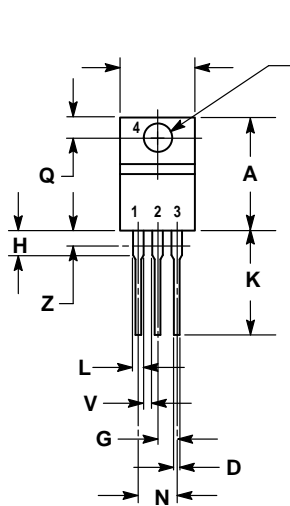


Figure 10. Reverse Biased Safe Operating Area

PACKAGE DIMENSIONS




STYLE 9:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-09
 ISSUE Z

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