MCM36F6
MCM36F7

Advance Information

256KB and 512KB Synchronous Fast Static RAM Module

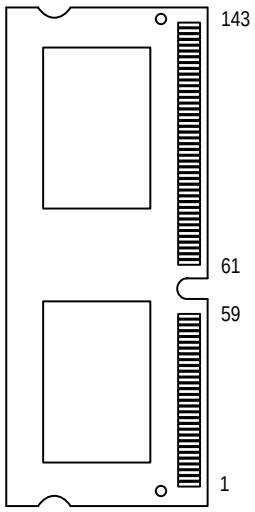
The MCM36F6 (256KB) is configured as 64K x 36 bits and the MCM36F7 (512KB) is configured as 128K x 36 bits. Both are packaged in a 144–pin dual–in–line memory module (DIMM). Each module uses Motorola's 3.3 V 64K x 18 bit flow–through BurstRAMs.

Address (A), data inputs (DQ, DP), and all control signals except output enable (G) are clock (K) controlled through positive–edge–triggered noninverting registers.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature provides increased timing flexibility for incoming signals. Synchronous byte write (BWx) and global byte write (WE) allows writes to either individual bytes or to both bytes.

- Single 3.3 V + 10%, – 5% Power Supply
- Plug and Pin Compatibility with 1MB and 2MB
- Multiple Clock Pins for Reduced Loading
- All Inputs and Outputs are LVTTL Compatible
- Byte Write and Global Write Capability
- Fast SRAM Access Times: 10 ns
- Berg Connector, Part Number: 61178–31844
- 144–Pin DIMM Module

144–LEAD DIMM
CASE 1154–01
TOP VIEW

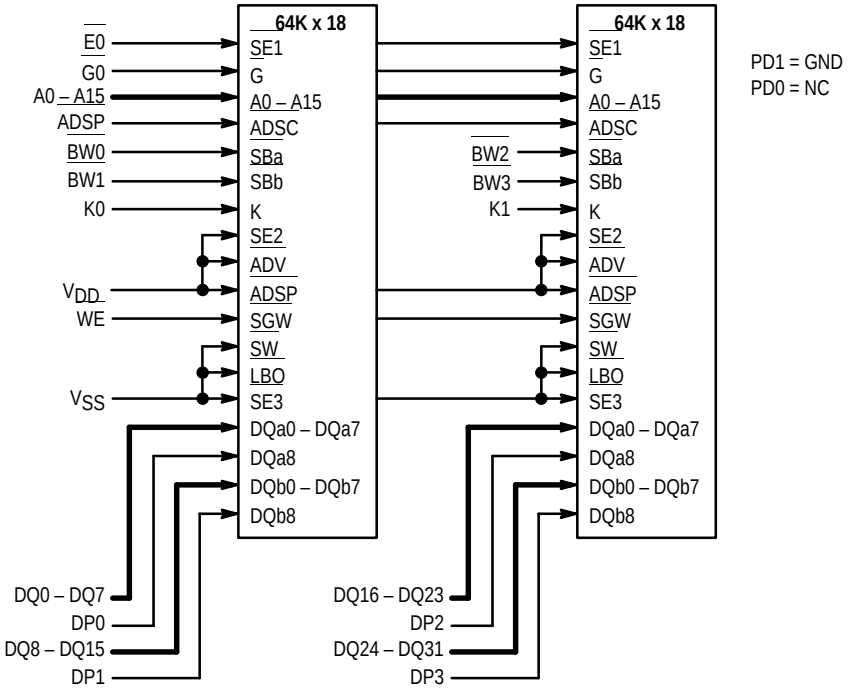


This document contains information on a new product. Specifications and information herein are subject to change without notice.

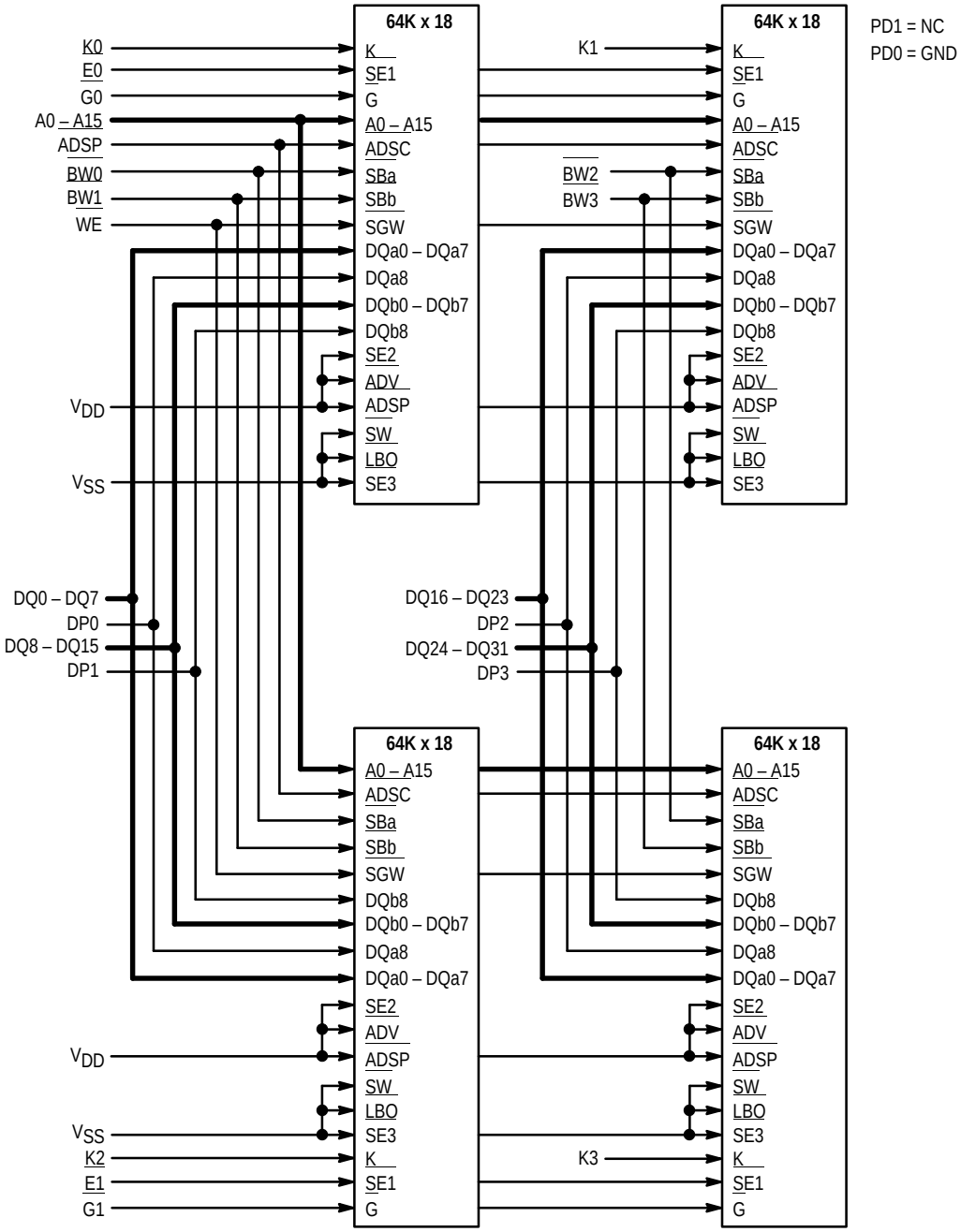
2/10/98

MOTOROLA

MCM36F6 BLOCK DIAGRAM



MCM36F7 BLOCK DIAGRAM



PIN ASSIGNMENT
144–LEAD DIMM
TOP VIEW

V_{SS}	1	2	V_{SS}
A0	3	4	A1
A2	5	6	A3
A4	7	8	A5
V_{DD}	9	10	V_{DD}
NC	11	12	NC
NC	13	14	NC
V_{SS}	15	16	V_{SS}
A6	17	18	A7
A8	19	20	A9
A10	21	22	A11
NC	23	24	NC
V_{DD}	25	26	V_{DD}
A12	27	28	A13
A14	29	30	A15
NC	31	32	NC
V_{SS}	33	34	V_{SS}
PD0	35	36	PD1
$\overline{V_{SS}}$	37	38	$\overline{V_{SS}}$
$\overline{BW0}$	39	40	$\overline{BW1}$
E0	41	42	G0
V_{SS}	43	44	V_{SS}
K1	45	46	K0
V_{SS}	47	48	V_{SS}
DQ0	49	50	DQ1
V_{DD}	51	52	V_{DD}
DQ2	53	54	DQ3
DQ4	55	56	DQ5
DQ6	57	58	DQ7
V_{SS}	59	60	V_{SS}
V_{DD}	61	62	V_{DD}
DQ8	63	64	DQ9
DQ10	65	66	DQ11
V_{SS}	67	68	V_{SS}
DQ12	69	70	DQ13
DQ14	71	72	DQ15
DP0	73	74	DP1
NC	75	76	NC
NC	77	78	NC
$\overline{V_{SS}}$	79	80	$\overline{V_{SS}}$
WE	81	82	ADSP
NC	83	84	NC
V_{DD}	85	86	V_{DD}
NC	87	88	NC
NC	89	90	NC
NC	91	92	NC
V_{DD}	93	94	V_{DD}
NC	95	96	NC
NC	97	98	NC
NC	99	100	NC
$\overline{V_{SS}}$	101	102	$\overline{V_{SS}}$
$\overline{BW2}$	103	104	$\overline{BW3}$
E1	105	106	G1
V_{DD}	107	108	V_{DD}
DQ16	109	110	DQ17
DQ18	111	112	DQ19
NC	113	114	NC
NC	115	116	NC
NC	117	118	NC
V_{SS}	119	120	V_{SS}
K3	121	122	K2
V_{SS}	123	124	V_{SS}
DQ20	125	126	DQ21
V_{SS}	127	128	V_{SS}
DQ22	129	130	DQ23
DQ24	131	132	DQ25
DQ26	133	134	DQ27
DQ28	135	136	DQ29
V_{DD}	137	138	V_{DD}
DQ30	139	140	DQ31
DP2	141	142	DP3
V_{SS}	143	144	V_{SS}

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
3, 4, 5, 6, 7, 8, 17, 18, 19, 20, 21, 22, 27, 28, 29, 30,	A0 – A15	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
82	$\overline{ADSP}$	Input	Synchronous Addresss Status Controller: Initiates read, write, or chip deselect cycle.
39, 40, 103, 104	BW0 – BW3	Input	Synchronous Byte Write Inputs: x refers to the byte being written (byte a, b, c, d). WE overrides BWx.
73, 74, 141, 142	DP0 – DP3		Synchronous Parity Data Inputs/Outputs.
(a) 49, 50, 53, 54, 55, 56, 57, 58, (b) 63, 64, 65, 66, 69, 70, 71, 72 (c) 109, 110, 111, 112, 125, 126, 129, 130 (d) 131, 132, 133, 134, 135, 136, 139, 140	DQ0 – DQ31	I/O	Synchronous Data Inputs/Outputs.
41, 105	$\overline{E0}$, $\overline{E1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — deselects chip when ADSP is asserted.
42, 106	$\overline{G0}$, $\overline{G1}$	Input	Asynchronous Output Enable Input.
46, 45, 122, 121	K0 – K3	Input	Clock: This signal registers the address, data in, and all control signals except G.
35, 36	PD0, PD1	Output	Presence Detect Bits.
81	$\overline{WE}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the BWx signals. If only byte write signals SBx are being used, tie this pin high.
9, 10, 25, 26, 51, 52, 61, 62, 85, 86, 93, 94, 107, 108, 137, 138	V_{DD}	Supply	Power Supply: 3.3 V + 10%, – 5%.
1, 2, 15, 16, 33, 34, 37, 38, 43, 44, 47, 48, 59, 60, 67, 68, 79, 80, 101, 102, 119, 120, 123, 124, 127, 128, 143, 144	V_{SS}	Supply	Ground.
11, 12, 13, 14, 23, 24, 31, 32, 75, 76, 77, 78, 83, 84, 87, 88, 89, 90, 91, 92, 95, 96, 97, 98, 99, 100, 113, 114, 115, 116, 117, 118	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{E}x$	$\overline{ADSP}$	$\overline{G}x$	DQx	$\overline{WRITE}$[2, 4]
Deselect	None	1	0	X	High–Z	X
Begin Read	External	0	0	0	DQ	Read
Read	Current	X	1	1	High–Z	Read
Read	Current	X	1	0	DQ	Read
Begin Write	External	0	0	X	High–Z	Write
Write	Current	X	1	X	High–Z	Write

NOTES:
1. X = don't care, 1 = logic high, 0 = logic low.
2. Write is defined as either any $\overline{BW}x$ or $\overline{WE}$ low.
3. Gx is an asynchronous signal and is not sampled by the clock K. Gx drives the bus immediately (t_{GLQX}) following $\overline{G}x$ going low.
4. On write cycles that follow read cycles, Gx must be negated prior to the start of the write cycle to ensure proper write data setup times. Gx must also remain negated at the completion of the write cycle to ensure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Ambient Temperature	T_A	0 to 70	°C
Die Temperature	T_J	110	°C
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* $V_{IL} \geq$ – 2.0 V for t ≤ t_{KHKH}/2.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit	Notes
AC Supply Current (Device Selected, All Outputs Open, Cycle Time ≥ t_{KHKH} min)	MCM36F6DG10 MCM36F7DG10	I_{DDA}	—	430 630	mA	1, 2, 3
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM36F6DG10 MCM36F7DG10	I_{SB1}	—	200 400	mA	
Clock Running Supply Current (Deselected, Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{DD} – 0.2 V)	MCM36F6DG10 MCM36F7DG10	I_{SB2}	—	70 140	mA	4

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (HSB).
3. Data states are all zero.
4. Device in deselected mode as defined by the Truth Table.

MCM36F6 CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{BW}$x, K Other Inputs	C_{in}	— —	11 17	pF
I/O Capacitance		$C_{I/O}$	—	14	pF

MCM36F7 CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70 °C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	$\overline{\text{\_\_\_\_}}$ $\overline{\text{K}}$ Addr, ADSP, WE Other Inputs	C_{in}	— — —	11 29 17	pF
I/O Capacitance		$C_{I/O}$	—	23	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, – 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

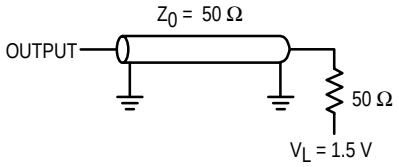
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 1 V/ns (20 to 80%)

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1 Unless Otherwise Noted

DATA RAM READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM36F6 – 10 MCM36F7 – 10		Unit	Notes
		Min	Max		
Cycle Time	t_{KHKH}	15	—	ns	
Clock Access Time	t_{KHQV}	—	10	ns	
Output Enable to Output Valid	t_{GLQV}	—	5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	ns	5
Clock High to Output Change	t_{KHQX2}	3	—	ns	5
Output Enable to Output Active	t_{GLQX}	0	—	ns	5
Output Disable to Q High–Z	t_{GHQZ}	—	5	ns	5, 6
Clock High to Q High–Z	t_{KHQZ}	3	5	ns	5, 6
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Setup Times: Address ADSP Data In Write Chip Enable	t_{AVKH} t_{ADKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	ns	
Hold Times: Address ADSP, ADSC, ADV Data In Write Chip Enable	t_{KHAX} t_{KHADX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	ns	

NOTES:
1. Write is defined as either any BWx and SW low or WE is low.
2. Chip Enable is defined as E0 low, SE2 high, and SE3 low whenever ADSP or ADSC is asserted.
3. All read and write cycle timings are referenced from K0 or G0.
4. G0 is a don't care after write cycle begins. To prevent bus contention, G0 should be negated prior to start of write cycle.
5. This parameter is sampled and not 100% tested.
6. Measured at ± 200 mV from steady state.

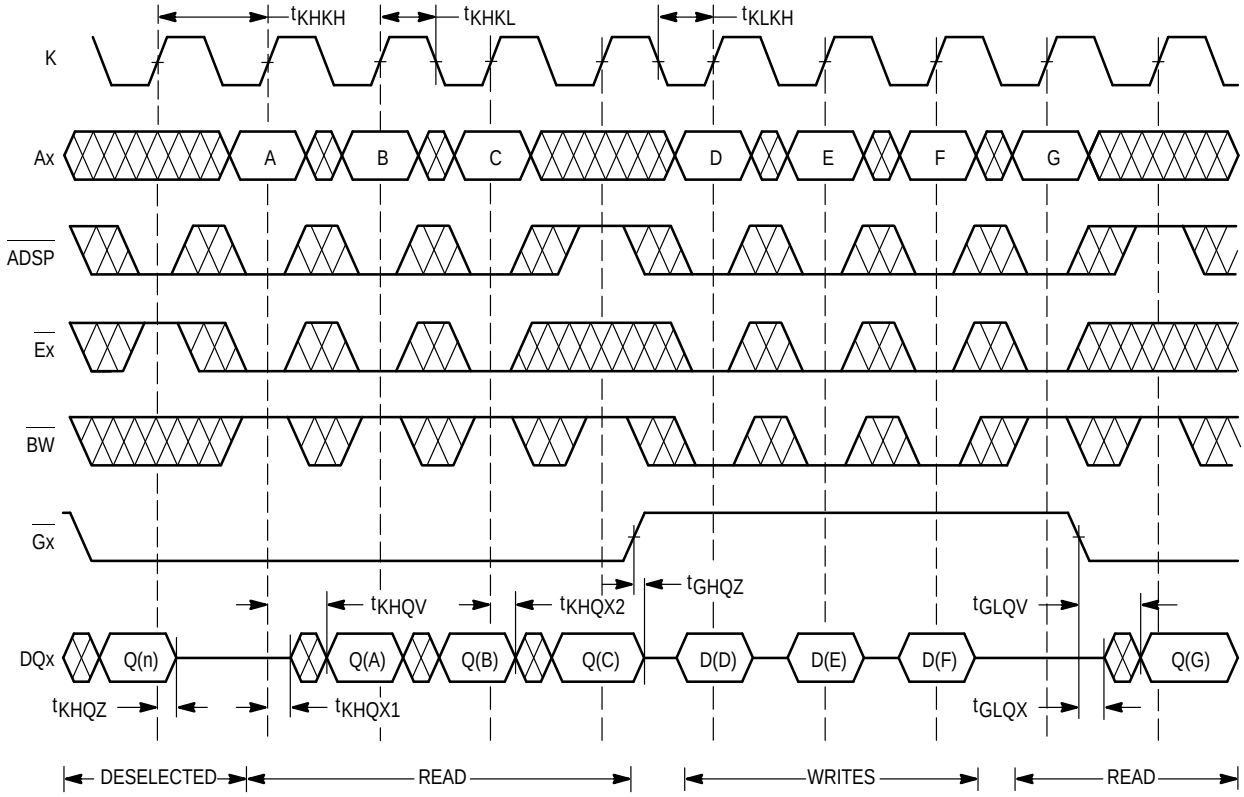


TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ/WRITE CYCLES



ORDERING INFORMATION

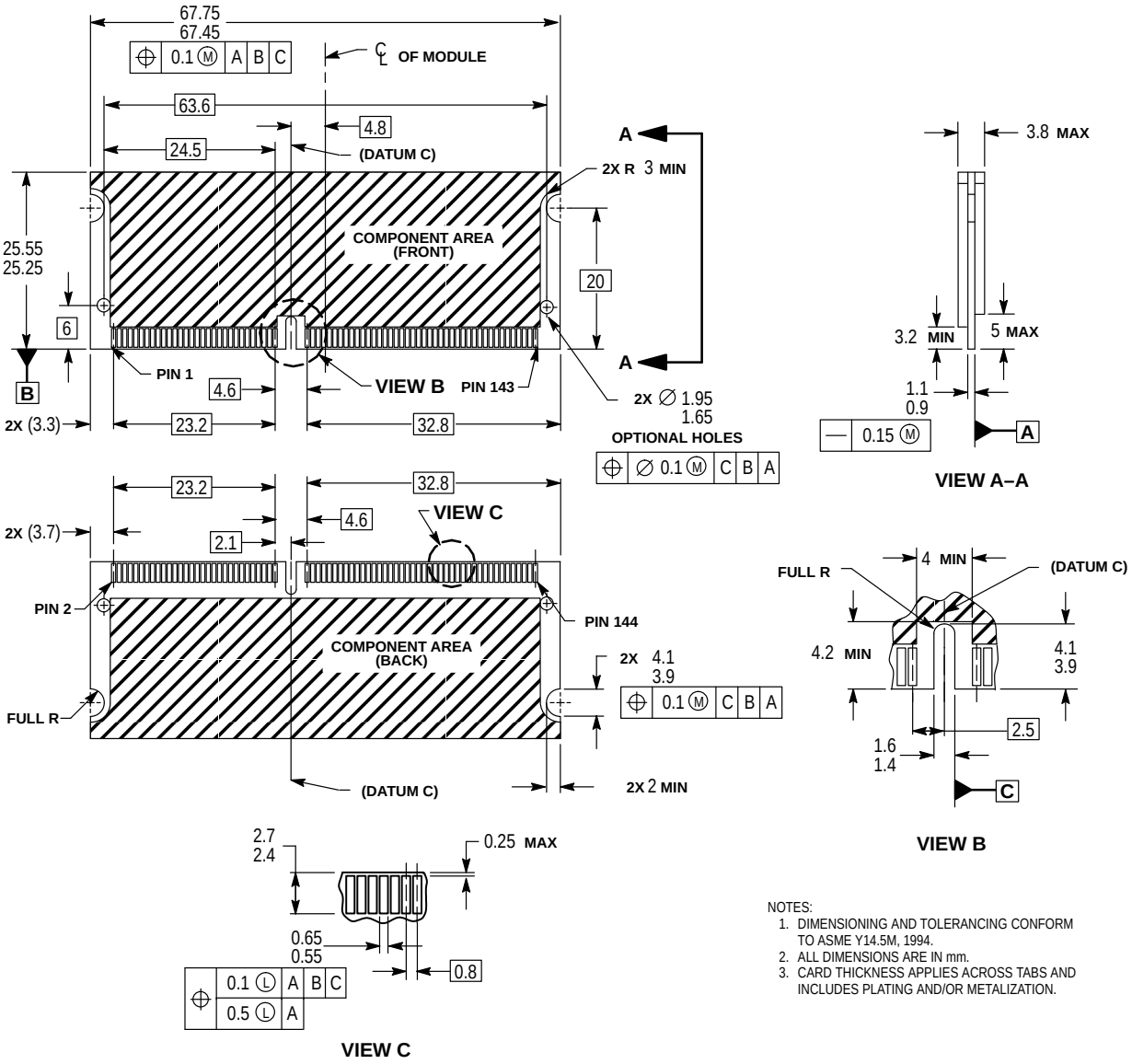
(Order by Full Part Number)

MCM	36F	X	XX	XX
Motorola Memory Prefix				
	Part Number			
		Memory Size (6 = 256KB, 7 = 512KB)		
			Package (DG = Gold Pad DIMM)	
				Speed (10 = 10 ns)

Full Part Numbers — MCM36F6DG10 MCM36F7DG10

PACKAGE DIMENSIONS

144–LEAD DIMM
CASE 1154–01



NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M, 1994.
2. ALL DIMENSIONS ARE IN mm.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

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