

# **MC9S12A256**

## **Device Guide**

### **V01.01**

**Original Release Date: 8 March 2002**  
**Revised: 12 April 2002**



# Revision History

| Version Number | Revision Date | Effective Date | Author | Description of Changes  |
|----------------|---------------|----------------|--------|---|
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For additional information, refer to the MC9S12A256 8-Bit Microcontroller Unit Mask Set Errata (Motorola document order number, 9S12A256MSE1). The errata can be found on the World Wide Web at:

<http://www.motorola.com/semiconductors/>

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## Preface

The Device User Guide provides information about the MC9S12A256 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the *CPU12 Reference Manual* (Motorola order number, CPU12RM/AD) and all the individual Block User Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-1** for names and versions of the referenced documents throughout the Device User Guide.

**Table 0-1 Document References**

| User Guide            | Version | Document Order Number |
|-----------------------|---------|-----------------------|
| HCS12 Core User Guide | V01     | HCS12COREUG/D         |
| CRG Block Guide       | V02     | S12CRGV3/D            |
| ECT_16B8C Block Guide | V01     | S12ECT16B8CV1/D       |
| ATD_10B8C Block Guide | V02     | S12ATD10B8CV2/D       |
| IIC Block Guide       | V02     | S12IICV2/D            |
| SCI Block Guide       | V02     | S12SCIV2/D            |
| SPI Block Guide       | V02     | S12SPIV2/D            |
| PWM_8B8C Block Guide  | V01     | S12PWM8B8CV1/D        |
| FTS256K Block Guide   | V02     | S12FTS256KV2/D        |
| EETS4K Block Guide    | V02     | S12EETS4KV2/D         |
| VREG Block Guide      | V01     | S12VREGV1/D           |
| PIM_9A256 Block Guide | V01     | S12A256PIMV1/D        |



# Section 1 Introduction

## 1.1 Overview

The MC9S12A256 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 256K bytes of Flash EEPROM, 12K bytes of RAM, 4K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), three serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability and an Inter-IC Bus. System resource mapping, clock generation, interrupt control and bus interfacing are managed by the System Integration Module (SIM). The MC9S12A256 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

## 1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    - i. Upward compatible with M68HC11 instruction set
    - ii. Interrupt stacking and programmer's model identical to M68HC11
    - iii. Instruction queue
    - iv. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Mode)
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- 8-bit and 4-bit ports with interrupt functionality
  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 256K Flash EEPROM
  - 4K byte EEPROM
  - 12K byte RAM

- Two 8-channel Analog-to-Digital Converters
  - 10-bit resolution
  - External conversion trigger capability
- Enhanced Capture Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 8 PWM channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
  - Usable as interrupt inputs
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Three Synchronous Serial Peripheral Interface (SPI)
- Inter-IC Bus (IIC)
  - Compatible with I2C Bus standard
  - Multi-master operation
  - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP and 80-pin QFP packages
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs
  - Operation at 50MHz equivalent to 25MHz Bus Speed
  - Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints



## 1.3 Modes of Operation

### User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Motorola use only**)
  - Special Peripheral Mode (**Motorola use only**)

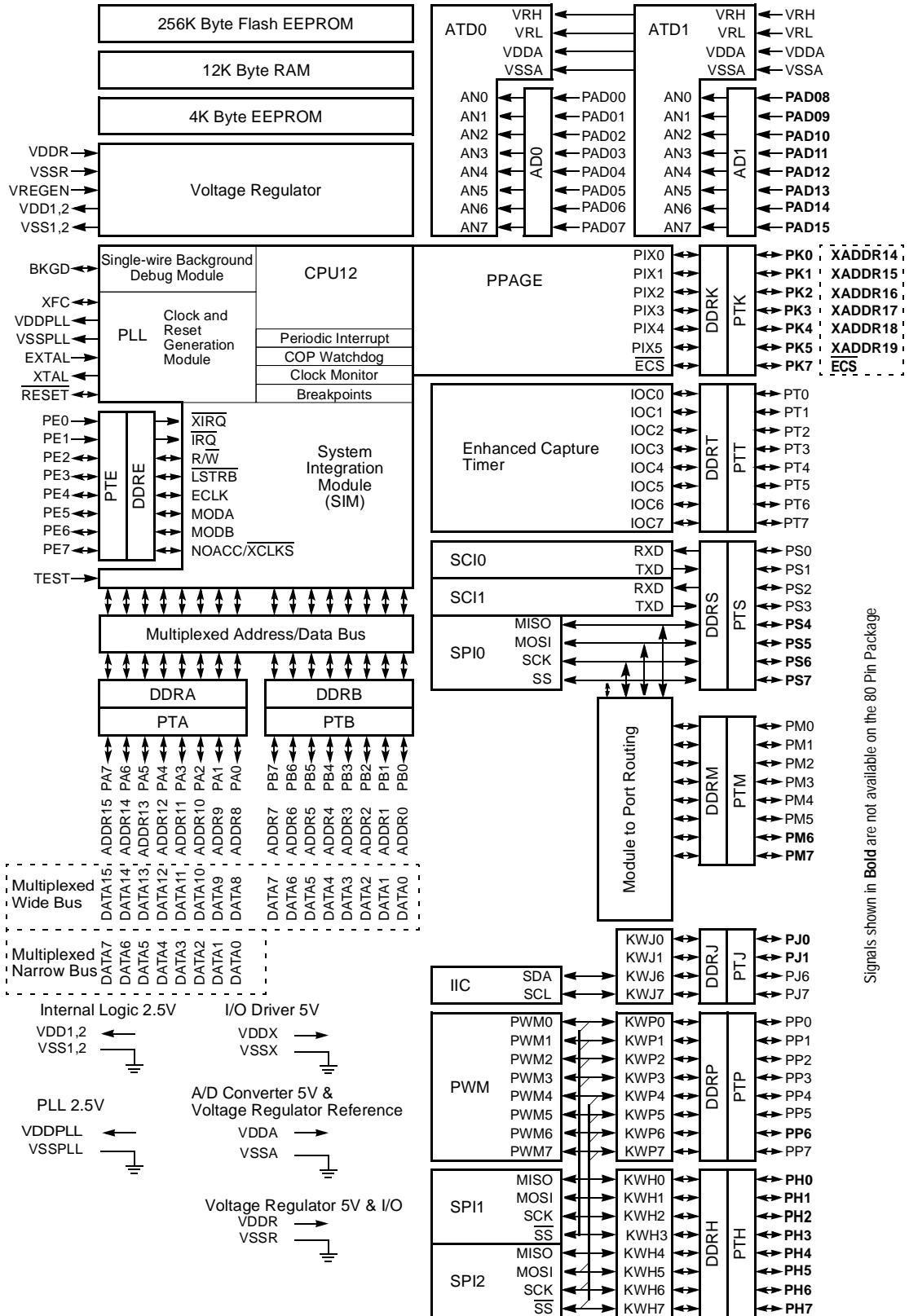
### Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

## 1.4 Block Diagram

**Figure 1-1** shows a block diagram of the MC9S12A256 device.

Figure 1-1 MC9S12A256 Block Diagram



Signals shown in **Bold** are not available on the 80 Pin Package

Freescale Semiconductor, Inc.

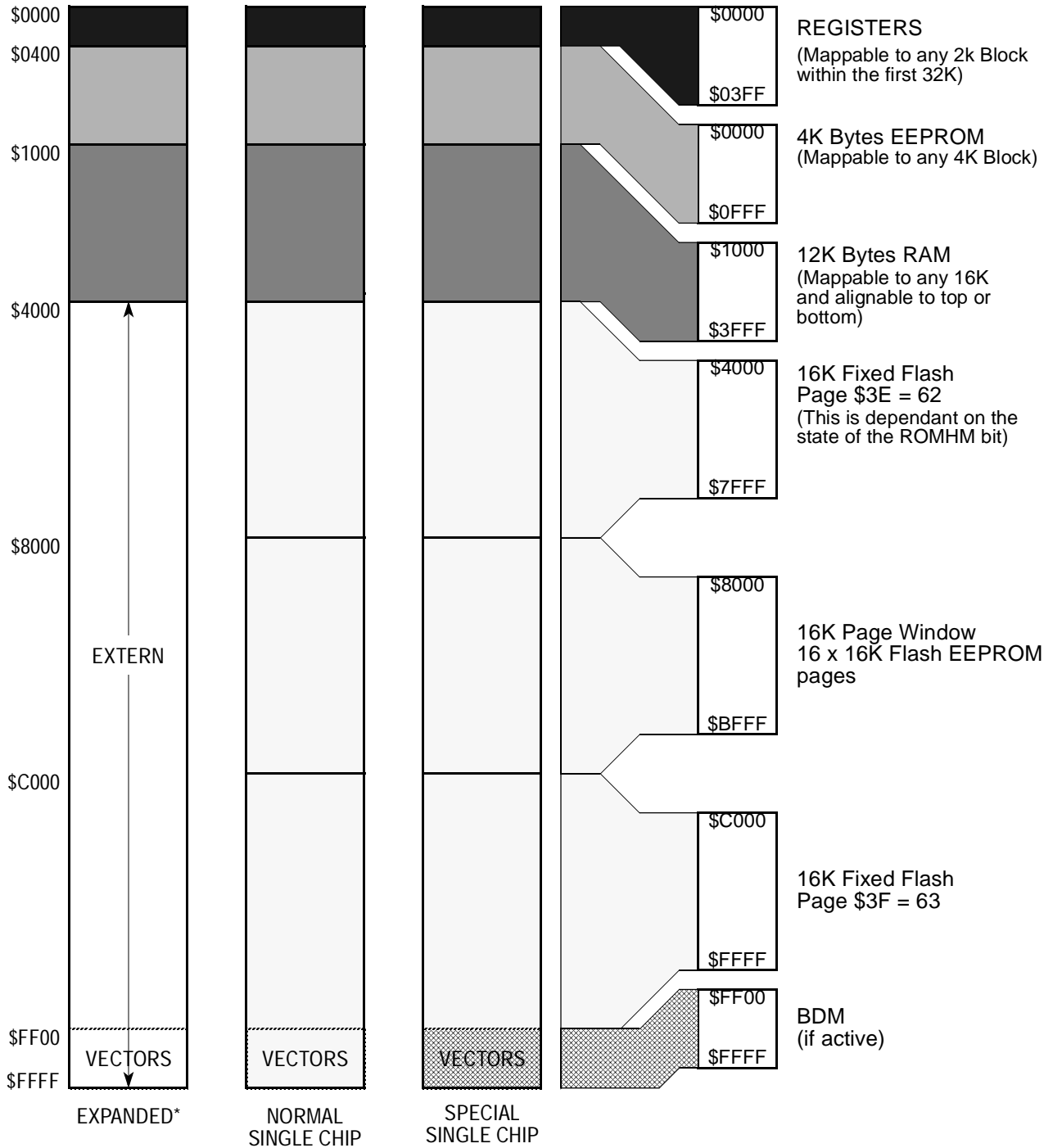
## 1.5 Device Memory Map

**Table 1-1** and **Figure 1-2** show the device memory map of the MC9S12A256 after reset. Note that after reset the bottom 1K of the EEPROM (\$0000 - \$03FF) are hidden by the register space.

**Table 1-1 Device Memory Map**

| Address         | Module   | Size (Bytes) |
|-----------------|--|--------------|
| \$0000 - \$0017 | CORE (Ports A, B, E, Modes, Inits, Test)   | 24           |
| \$0018 - \$0019 | Reserved   | 2            |
| \$001A - \$001B | Device ID register (PARTID)  | 2            |
| \$001C - \$001F | CORE (MEMSIZ, IRQ, HPRIO)  | 4            |
| \$0020 - \$0027 | Reserved   | 8            |
| \$0028 - \$002F | CORE (Background Debug Mode)   | 8            |
| \$0030 - \$0033 | CORE (PPAGE, Port K)   | 4            |
| \$0034 - \$003F | Clock and Reset Generator (PLL, RTI, COP)  | 12           |
| \$0040 - \$007F | Enhanced Capture Timer 16-bit 8 channels   | 64           |
| \$0080 - \$009F | Analog to Digital Converter 10-bit 8 channels (ATD0)   | 32           |
| \$00A0 - \$00C7 | Pulse Width Modulator 8-bit 8 channels (PWM)   | 40           |
| \$00C8 - \$00CF | Serial Communications Interface 0 (SCI0)   | 8            |
| \$00D0 - \$00D7 | Serial Communications Interface 0 (SCI1)   | 8            |
| \$00D8 - \$00DF | Serial Peripheral Interface (SPI0)   | 8            |
| \$00E0 - \$00E7 | Inter IC Bus   | 8            |
| \$00E8 - \$00EF | Reserved   | 8            |
| \$00F0 - \$00F7 | Serial Peripheral Interface (SPI1)   | 8            |
| \$00F8 - \$00FF | Serial Peripheral Interface (SPI2)   | 8            |
| \$0100 - \$010F | Flash Control Register   | 16           |
| \$0110 - \$011B | EEPROM Control Register  | 12           |
| \$011C - \$011F | Reserved   | 4            |
| \$0120 - \$013F | Analog to Digital Converter 10-bit 8 channels (ATD1)   | 32           |
| \$0140 - \$023F | Reserved   | 256          |
| \$0240 - \$027F | Port Integration Module (PIM)  | 64           |
| \$0280 - \$03FF | Reserved   | 384          |
| \$0000 - \$0FFF | EEPROM array   | 4096         |
| \$1000 - \$3FFF | RAM array  | 12288        |
| \$4000 - \$7FFF | Fixed Flash EEPROM array<br>incl. 0.5K, 1K, 2K or 4K Protected Sector at start   | 16384        |
| \$8000 - \$BFFF | Flash EEPROM Page Window   | 16384        |
| \$C000 - \$FFFF | Fixed Flash EEPROM array<br>incl. 0.5K, 1K, 2K or 4K Protected Sector at end<br>and 256 bytes of Vector Space at \$FF80 - \$FFFF | 16384        |

Figure 1-2 MC9S12A256 Memory Map



\* Assuming that a '0' was driven onto port K bit 7 during MCU reset is reset into normal expanded wide or narrow mode.

## 1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses \$001A and \$001B after reset). The read-only value is a unique part ID for each revision of the chip. **Table 1-2** shows the assigned part ID number.

**Table 1-2 Assigned Part ID Numbers**

| Device     | Mask Set Number | Part ID <sup>1</sup> |
|------------|-----------------|----------------------|
| MC9S12A256 |                 | \$0010               |
| MC9S12A256 |                 | \$0011               |

NOTES:

- The coding is as follows:  
 Bit 15-12: Major family identifier  
 Bit 11-8: Minor family identifier  
 Bit 7-4: Major mask set revision number including FAB transfers  
 Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses \$001C and \$001D after reset). **Table 1-3** shows the read-only values of these registers. Refer to the *HCS12 Core User Guide* (Motorola order number, HCS12COREUG/D) for further details.

**Table 1-3 Memory Size Registers**

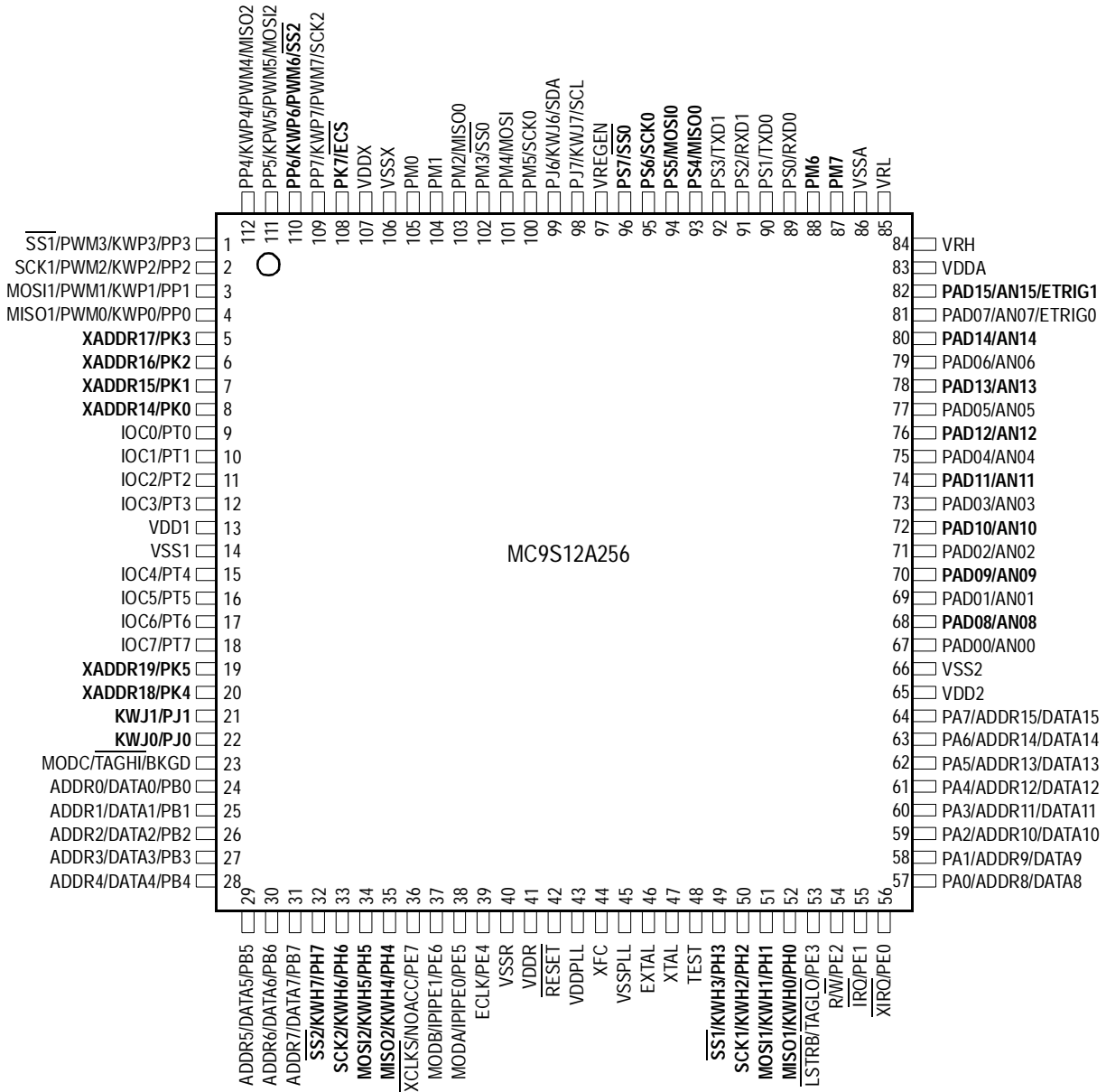
| Register name | Value |
|---------------|-------|
| MEMSIZ0       | \$25  |
| MEMSIZ1       | \$81  |

## Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

### 2.1 Device Pinout

The MC9S12A256 is available in a 112-pin low profile quad flat pack (LQFP) and is also available in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. [Figure 2-1](#) and [Figure 2-2](#) show the pin assignments.



Signals shown in **Bold** are not available on the 80 Pin Package

**Figure 2-1 Pin Assignments in 112-Pin LQFP**



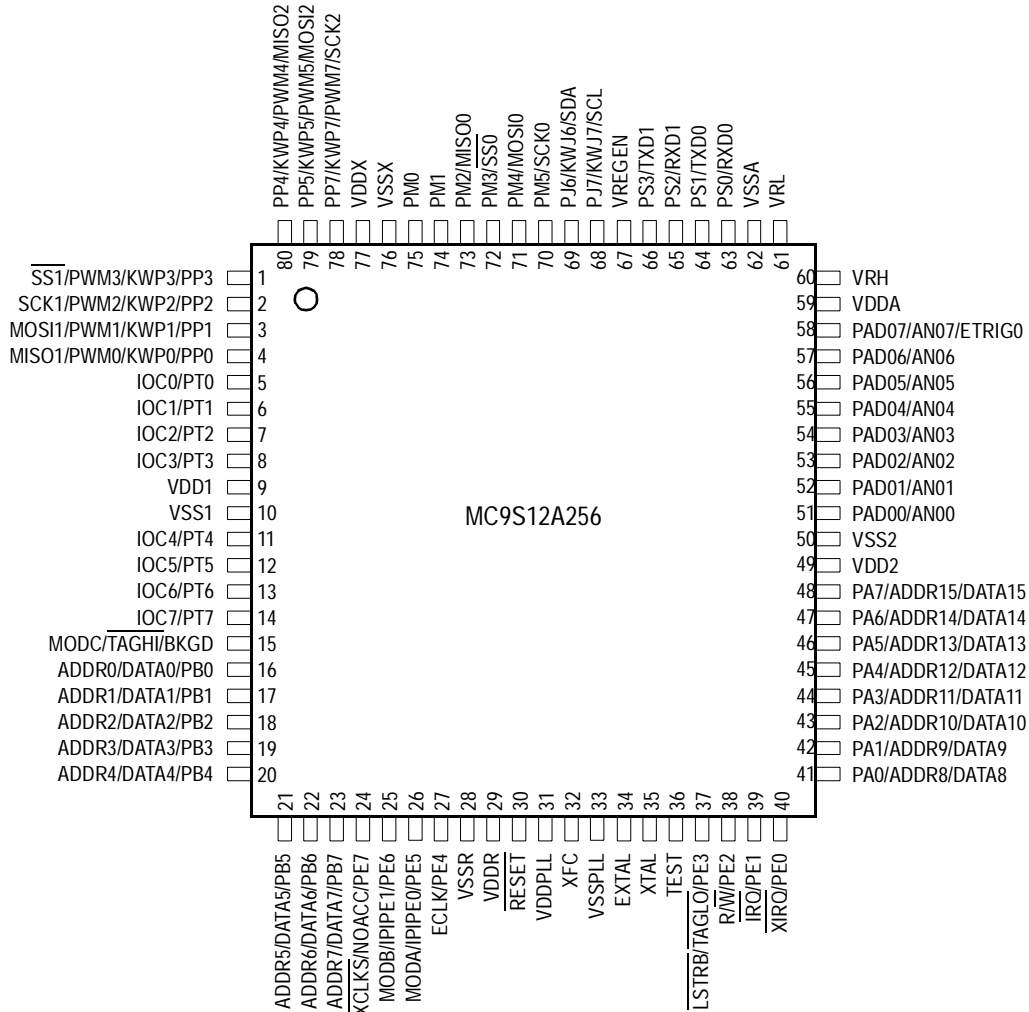


Figure 2-2 Pin Assignments in 80-Pin QFP for MC9S12A256

## 2.2 Signal Properties Summary

**Table 2-1** summarizes the pin functionality. Signals shown in **bold** are not available in the 80 pin package.

**Table 2-1 Signal Properties**

| Pin Name Function 1       | Pin Name Function 2       | Pin Name Function 3 | Pin Name Function 4 | Powered by         | Description  |
|---------------------------|---------------------------|---------------------|---------------------|--------------------|--|
| EXTAL                     | —                         | —                   | —                   | V <sub>DDPLL</sub> | Oscillator Pins  |
| XTAL                      | —                         | —                   | —                   |                    |  |
| $\overline{\text{RESET}}$ | —                         | —                   | —                   |                    |  |
| TEST                      | —                         | —                   | —                   | N.A.               | Test Input   |
| V <sub>REGEN</sub>        | —                         | —                   | —                   | V <sub>DDX</sub>   | Voltage Regulator Enable Input   |
| XFC                       | —                         | —                   | —                   | V <sub>DDPLL</sub> | PLL Loop Filter  |
| BKGD                      | $\overline{\text{TAGHI}}$ | MODC                | —                   | V <sub>DDR</sub>   | Background Debug, Tag High, Mode Input   |
| <b>PAD15</b>              | <b>AN15</b>               | <b>ETRIG1</b>       | —                   | V <sub>DDA</sub>   | <b>Port AD Input, Analog Input AN7 of ATD1, External Trigger Input of ATD1</b> |
| <b>PAD[14:8]</b>          | <b>AN[14:08]</b>          | —                   | —                   |                    | <b>Port AD Inputs, Analog Inputs AN[6:0] of ATD1</b>                           |
| PAD07                     | AN07                      | ETRIG0              | —                   |                    | Port AD Input, Analog Input AN7 of ATD0, External Trigger Input of ATD0        |
| PAD[06:00]                | AN[06:00]                 | —                   | —                   |                    | Port AD Inputs, Analog Inputs AN[6:0] of ATD0                                  |
| PA[7:0]                   | ADDR[15:8]/<br>DATA[15:8] | —                   | —                   | V <sub>DDR</sub>   | Port A I/O, Multiplexed Address/Data   |
| PB[7:0]                   | ADDR[7:0]/<br>DATA[7:0]   | —                   | —                   |                    | Port B I/O, Multiplexed Address/Data   |
| PE7                       | NOACC                     | XCLKS               | —                   |                    | Port E I/O, Access, Clock Select   |
| PE6                       | IPIPE1                    | MODB                | —                   |                    | Port E I/O, Pipe Status, Mode Input  |
| PE5                       | IPIPE0                    | MODA                | —                   |                    | Port E I/O, Pipe Status, Mode Input  |
| PE4                       | ECLK                      | —                   | —                   |                    | Port E I/O, Bus Clock Output   |
| PE3                       | LSTRB                     | TAGLO               | —                   |                    | Port E I/O, Byte Strobe, Tag Low   |
| PE2                       | R/W                       | —                   | —                   |                    | Port E I/O, R/W in expanded modes  |
| PE1                       | IRQ                       | —                   | —                   |                    | Port E Input, Maskable Interrupt   |
| PE0                       | XIRQ                      | —                   | —                   |                    | Port E Input, Non Maskable Interrupt   |
| <b>PH7</b>                | <b>KWH7</b>               | <b>SS2</b>          | —                   |                    | <b>Port H I/O, Interrupt, SS of SPI2</b>                                       |
| <b>PH6</b>                | <b>KWH6</b>               | <b>SCK2</b>         | —                   |                    | <b>Port H I/O, Interrupt, SCK of SPI2</b>                                      |
| <b>PH5</b>                | <b>KWH5</b>               | <b>MOSI2</b>        | —                   |                    | <b>Port H I/O, Interrupt, MOSI of SPI2</b>                                     |
| <b>PH4</b>                | <b>KWH4</b>               | <b>MISO2</b>        | —                   |                    | <b>Port H I/O, Interrupt, MISO of SPI2</b>                                     |
| <b>PH3</b>                | <b>KWH3</b>               | <b>SS1</b>          | —                   |                    | <b>Port H I/O, Interrupt, SS of SPI1</b>                                       |
| <b>PH2</b>                | <b>KWH2</b>               | <b>SCK1</b>         | —                   |                    | <b>Port H I/O, Interrupt, SCK of SPI1</b>                                      |
| <b>PH1</b>                | <b>KWH1</b>               | <b>MOSI1</b>        | —                   |                    | <b>Port H I/O, Interrupt, MOSI of SPI1</b>                                     |
| <b>PH0</b>                | <b>KWH0</b>               | <b>MISO1</b>        | —                   |                    | <b>Port H I/O, Interrupt, MISO of SPI1</b>                                     |

| Pin Name Function 1 | Pin Name Function 2                       | Pin Name Function 3 | Pin Name Function 4                       | Powered by | Description  |
|---------------------|---|---------------------|---|------------|--|
| PJ7                 | KWJ7                                      | SCL                 |   | VDDX       | Port J I/O, Interrupt, SCL of IIC                          |
| PJ6                 | KWJ6                                      | SDA                 |   |            | Port J I/O, Interrupt, SDA of IIC                          |
| <b>PJ[1:0]</b>      | <b>KWJ[1:0]</b>                           | —                   | —   |            | <b>Port J I/O, Interrupts</b>                              |
| <b>PK7</b>          | <b><math>\overline{\text{ECS}}</math></b> | <b>ROMONE</b>       | —   |            | <b>Port K I/O, Emulation Chip Select, ROM On Enable</b>    |
| <b>PK[5:0]</b>      | <b>XADDR[19:14]</b>                       |                     | —   |            | <b>Port K I/O, Extended Addresses</b>                      |
| <b>PM7</b>          | —   | —                   | —   |            | <b>Port M I/O</b>  |
| <b>PM6</b>          | —   | —                   | —   |            | <b>Port M I/O</b>  |
| PM5                 | SCK0                                      | —                   | —   |            | Port M I/O, SCK of SPI0                                    |
| PM4                 | MOSI0                                     | —                   | —   |            | Port M I/O, MOSI of SPI0                                   |
| PM3                 | SS0                                       | —                   | —   |            | Port M I/O, SS of SPI0                                     |
| PM2                 | MISO0                                     | —                   | —   |            | Port M I/O, MISO of SPI0                                   |
| PM1                 | —   | —                   | —   |            | Port M I/O   |
| PM0                 | —   | —                   | —   |            | Port M I/O   |
| PP7                 | KWP7                                      | PWM7                | SCK2                                      |            | Port P I/O, Interrupt, Channel 7 of PWM, SCK of SPI2       |
| <b>PP6</b>          | <b>KWP6</b>                               | <b>PWM6</b>         | <b><math>\overline{\text{SS2}}</math></b> |            | <b>Port P I/O, Interrupt, Channel 6 of PWM, SS of SPI2</b> |
| PP5                 | KWP5                                      | PWM5                | MOSI2                                     |            | Port P I/O, Interrupt, Channel 5 of PWM, MOSI of SPI2      |
| PP4                 | KWP4                                      | PWM4                | MISO2                                     |            | Port P I/O, Interrupt, Channel 4 of PWM, MISO2 of SPI2     |
| PP3                 | KWP3                                      | PWM3                | $\overline{\text{SS1}}$                   |            | Port P I/O, Interrupt, Channel 3 of PWM, SS of SPI1        |
| PP2                 | KWP2                                      | PWM2                | SCK1                                      |            | Port P I/O, Interrupt, Channel 2 of PWM, SCK of SPI1       |
| PP1                 | KWP1                                      | PWM1                | MOSI1                                     |            | Port P I/O, Interrupt, Channel 1 of PWM, MOSI of SPI1      |
| PP0                 | KWP0                                      | PWM0                | MISO1                                     |            | Port P I/O, Interrupt, Channel 0 of PWM, MISO2 of SPI1     |
| <b>PS7</b>          | <b><math>\overline{\text{SS0}}</math></b> | —                   | —   |            | <b>Port S I/O, SS of SPI0</b>                              |
| <b>PS6</b>          | <b>SCK0</b>                               | —                   | —   |            | <b>Port S I/O, SCK of SPI0</b>                             |
| <b>PS5</b>          | <b>MOSI0</b>                              | —                   | —   |            | <b>Port S I/O, MOSI of SPI0</b>                            |
| <b>PS4</b>          | <b>MISO0</b>                              | —                   | —   |            | <b>Port S I/O, MISO of SPI0</b>                            |
| PS3                 | TXD1                                      | —                   | —   |            | Port S I/O, TXD of SCI1                                    |
| PS2                 | RXD1                                      | —                   | —   |            | Port S I/O, RXD of SCI1                                    |
| PS1                 | TXD0                                      | —                   | —   |            | Port S I/O, TXD of SCI0                                    |
| PS0                 | RXD0                                      | —                   | —   |            | Port S I/O, RXD of SCI0                                    |
| PT[7:0]             | IOC[7:0]                                  | —                   | —   |            | Port T I/O, Timer channels                                 |

## 2.3 Detailed Signal Descriptions

### 2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

### 2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

### 2.3.3 TEST — Test Pin

This input only pin is reserved for test.

**NOTE:** The TEST pin must be tied to VSS in all applications.

### 2.3.4 $V_{\text{REGEN}}$ — Voltage Regulator Enable Pin

This input only pin enables or disables the on-chip voltage regulator.

### 2.3.5 XFC — PLL Loop Filter Pin

PLL loop filter, see [A.5.3 Phase Locked Loop](#). If needed, contact your Motorola representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

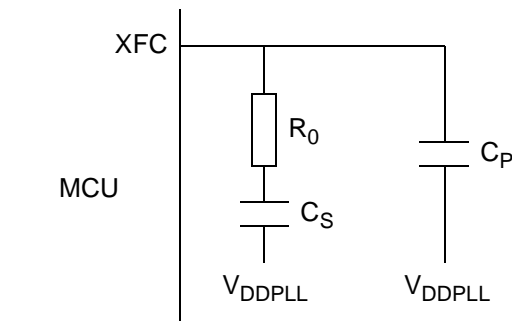


Figure 2-3 PLL Loop Filter Connections

### 2.3.6 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/ $\overline{\text{TAGHI}}$ /MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of  $\overline{\text{RESET}}$ .

### 2.3.7 PAD15 / AN15 / ETRIG1 — Port AD Input Pin of ATD1

PAD15 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD1. It can act as an external trigger input for the ATD1.

### 2.3.8 PAD[14:08] / AN[14:08] — Port AD Input Pins of ATD1

PAD14 - PAD08 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD1.

### 2.3.9 PAD7 / AN07 / ETRIG0 — Port AD Input Pin of ATD0

PAD7 is a general purpose input pin and analog input AN7 of the analog to digital converter ATD0. It can act as an external trigger input for the ATD0.

### 2.3.10 PAD[06:00] / AN[06:00] — Port AD Input Pins of ATD0

PAD06 - PAD00 are general purpose input pins and analog inputs AN[6:0] of the analog to digital converter ATD0.

### 2.3.11 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

### 2.3.12 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

### 2.3.13 PE7 / NOACC / $\overline{\text{XCLKS}}$ — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.

The  $\overline{\text{XCLKS}}$  input selects between an external clock or oscillator configuration. The state of this pin is latched at the rising edge of  $\overline{\text{RESET}}$ . If the input is a logic low the EXTAL pin is configured for an external

clock drive. If input is a logic high an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-up device, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL.

### 2.3.14 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of  $\overline{\text{RESET}}$ . This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when  $\overline{\text{RESET}}$  is low.

### 2.3.15 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of  $\overline{\text{RESET}}$ . This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when  $\overline{\text{RESET}}$  is low.

### 2.3.16 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

### 2.3.17 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. In MCU expanded modes of operation,  $\overline{\text{LSTRB}}$  can be used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on,  $\overline{\text{TAGLO}}$  is used to tag the low half of the instruction word being read into the instruction queue.

### 2.3.18 PE2 / $\overline{\text{R/W}}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. In MCU expanded modes of operations, this pin drives the read/write output signal for the external bus. It indicates the direction of data on the external bus.

### 2.3.19 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general purpose input pin and the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

### 2.3.20 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general purpose input pin and the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

### 2.3.21 PH7 / KWH7 / $\overline{SS2}$ — Port H I/O Pin 7

PH7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 2 (SPI2).

### 2.3.22 PH6 / KWH6 / SCK2 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

### 2.3.23 PH5 / KWH5 / MOSI2 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

### 2.3.24 PH4 / KWH4 / MISO2 — Port H I/O Pin 4

PH4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

### 2.3.25 PH3 / KWH3 / $\overline{SS1}$ — Port H I/O Pin 3

PH3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 1 (SPI1).

### 2.3.26 PH2 / KWH2 / SCK1 — Port H I/O Pin 2

PH2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

### 2.3.27 PH1 / KWH1 / MOSI1 — Port H I/O Pin 1

PH1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

### 2.3.28 PH0 / KWH0 / MISO1 — Port H I/O Pin 0

PH0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

### 2.3.29 PJ7 / KWJ7 / SCL — PORT J I/O Pin 7

PJ7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial clock pin SCL of the IIC module.

### 2.3.30 PJ6 / KWJ6 / SDA — PORT J I/O Pin 6

PJ6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as the serial data pin SDA of the IIC module.

### 2.3.31 PJ[1:0] / KWJ[1:0] — Port J I/O Pins [1:0]

PJ1 and PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

### 2.3.32 PK7 / $\overline{\text{ECS}}$ / ROMONE — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, this pin is used as the emulation chip select output ( $\overline{\text{ECS}}$ ). During MCU normal expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMONE). At the rising edge of  $\overline{\text{RESET}}$ , the state of this pin is latched to the ROMON bit.

### 2.3.33 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK5-PK0 are general purpose input or output pins. In MCU expanded modes of operation, these pins provide the expanded address XADDR[19:14] for the external bus.

### 2.3.34 PM7 — Port M I/O Pin 7

PM7 is a general purpose input or output pin.

### 2.3.35 PM6 — Port M I/O Pin 6

PM6 is a general purpose input or output pin.

### 2.3.36 PM5 / SCK0 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).



### 2.3.37 PM4 / MOSI0 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the master output (during master mode) or slave input pin (during slave mode) MOSI for the Serial Peripheral Interface 0 (SPI0).

### 2.3.38 PM3 / $\overline{SS0}$ — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 0 (SPI0).

### 2.3.39 PM2 / MISO0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the master input (during master mode) or slave output pin (during slave mode) MISO for the Serial Peripheral Interface 0 (SPI0).

### 2.3.40 PM1 — Port M I/O Pin 1

PM1 is a general purpose input or output pin.

### 2.3.41 PM0 — Port M I/O Pin 0

PM0 is a general purpose input or output pin.

### 2.3.42 PP7 / KWP7 / PWM7 / SCK2 — Port P I/O Pin 7

PP7 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 7 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 2 (SPI2).

### 2.3.43 PP6 / KWP6 / PWM6 / $\overline{SS2}$ — Port P I/O Pin 6

PP6 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 6 output. It can be configured as slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 2 (SPI2).

### 2.3.44 PP5 / KWP5 / PWM5 / MOSI2 — Port P I/O Pin 5

PP5 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 5 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 2 (SPI2).

### 2.3.45 PP4 / KWP4 / PWM4 / MISO2 — Port P I/O Pin 4

PP4 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 4 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 2 (SPI2).

### 2.3.46 PP3 / KWP3 / PWM3 / $\overline{SS1}$ — Port P I/O Pin 3

PP3 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 3 output. It can be configured as slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 1 (SPI1).

### 2.3.47 PP2 / KWP2 / PWM2 / SCK1 — Port P I/O Pin 2

PP2 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 2 output. It can be configured as serial clock pin SCK of the Serial Peripheral Interface 1 (SPI1).

### 2.3.48 PP1 / KWP1 / PWM1 / MOSI1 — Port P I/O Pin 1

PP1 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 1 output. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 1 (SPI1).

### 2.3.49 PP0 / KWP0 / PWM0 / MISO1 — Port P I/O Pin 0

PP0 is a general purpose input or output pin. It can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode. It can be configured as Pulse Width Modulator (PWM) channel 0 output. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO of the Serial Peripheral Interface 1 (SPI1).

### 2.3.50 PS7 / $\overline{SS0}$ — Port S I/O Pin 7

PS6 is a general purpose input or output pin. It can be configured as the slave select pin  $\overline{SS}$  of the Serial Peripheral Interface 0 (SPI0).

### 2.3.51 PS6 / SCK0 — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as the serial clock pin SCK of the Serial Peripheral Interface 0 (SPI0).

### 2.3.52 PS5 / MOSI0 — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as master output (during master mode) or slave input pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

### 2.3.53 PS4 / MISO0 — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output pin (during slave mode) MOSI of the Serial Peripheral Interface 0 (SPI0).

### 2.3.54 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 1 (SCI1).

### 2.3.55 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 1 (SCI1).

### 2.3.56 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as the transmit pin TXD of Serial Communication Interface 0 (SCI0).

### 2.3.57 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as the receive pin RXD of Serial Communication Interface 0 (SCI0).

### 2.3.58 PT[7:0] / IOC[7:0] — Port T I/O Pins [7:0]

PT7-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC0 of the Enhanced Capture Timer (ECT).

## 2.4 Power Supply Pins

MC9S12A256 power and ground pins are described below.

**NOTE:** All  $V_{SS}$  pins must be connected together in the application.

### 2.4.1 $V_{DDX}$ , $V_{SSX}$ — Power & Ground Pins for I/O Drivers

External power and ground for I/O drivers. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

### 2.4.2 $V_{DDR}$ , $V_{SSR}$ — Power & Ground Pins for I/O Drivers & for Internal Voltage Regulator

External power and ground for I/O drivers and input to the internal voltage regulator. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

### 2.4.3 $V_{DD1}$ , $V_{DD2}$ , $V_{SS1}$ , $V_{SS2}$ — Core Power Pins

Power is supplied to the MCU through  $V_{DD}$  and  $V_{SS}$ . Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if  $V_{REGEN}$  is tied to ground.

**NOTE:** *No load allowed except for bypass capacitors.*

### 2.4.4 $V_{DDA}$ , $V_{SSA}$ — Power Supply Pins for ATD and $V_{REG}$

$V_{DDA}$ ,  $V_{SSA}$  are the power supply and ground input pins for the voltage regulator and the analog to digital converter. It also provides the reference for the internal voltage regulator. This allows the supply voltage to the ATD and the reference voltage to be bypassed independently.

### 2.4.5 $V_{RH}$ , $V_{RL}$ — ATD Reference Voltage Input Pins

$V_{RH}$  and  $V_{RL}$  are the reference voltage input pins for the analog to digital converter.

### 2.4.6 $V_{DDPLL}$ , $V_{SSPLL}$ — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently. This 2.5V voltage is generated by the internal voltage regulator.

**NOTE:** *No load allowed except for bypass capacitors.*

## 2.4.7 V<sub>REGEN</sub> — On Chip Voltage Regulator Enable

Enables the internal 5V to 2.5V voltage regulator. If this pin is tied low, V<sub>DD1,2</sub> and V<sub>DDPLL</sub> must be supplied externally.

**Table 2-2 MC9S12A256 Power and Ground Connection Summary**

| Mnemonic           | Pin Number  | Nominal Voltage | Description  |
|--------------------|-------------|-----------------|--|
|                    | 112-pin QFP |                 |  |
| V <sub>DD1,2</sub> | 13, 65      | 2.5 V           | Internal power and ground generated by internal regulator  |
| V <sub>SS1,2</sub> | 14, 66      | 0V              |  |
| V <sub>DDR</sub>   | 41          | 5.0 V           | External power and ground, supply to pin drivers and internal voltage regulator.   |
| V <sub>SSR</sub>   | 40          | 0 V             |  |
| V <sub>DDX</sub>   | 107         | 5.0 V           | External power and ground, supply to pin drivers.  |
| V <sub>SSX</sub>   | 106         | 0 V             |  |
| V <sub>DDA</sub>   | 83          | 5.0 V           | Operating voltage and ground for the analog-to-digital converters and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.           |
| V <sub>SSA</sub>   | 86          | 0 V             |  |
| V <sub>RL</sub>    | 85          | 0 V             | Reference voltages for the analog-to-digital converter.  |
| V <sub>RH</sub>    | 84          | 5.0 V           |  |
| V <sub>DDPLL</sub> | 43          | 2.5 V           | Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator. |
| V <sub>SSPLL</sub> | 45          | 0 V             |  |
| V <sub>REGEN</sub> | 97          | 5V              | Internal Voltage Regulator enable/disable  |



## Section 3 System Clock Description

### 3.1 Overview

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the *HCS12 Clock and Reset Generator (CRG) Block Guide* (Motorola document order number, S12CRGV3/D) for details on clock generation.

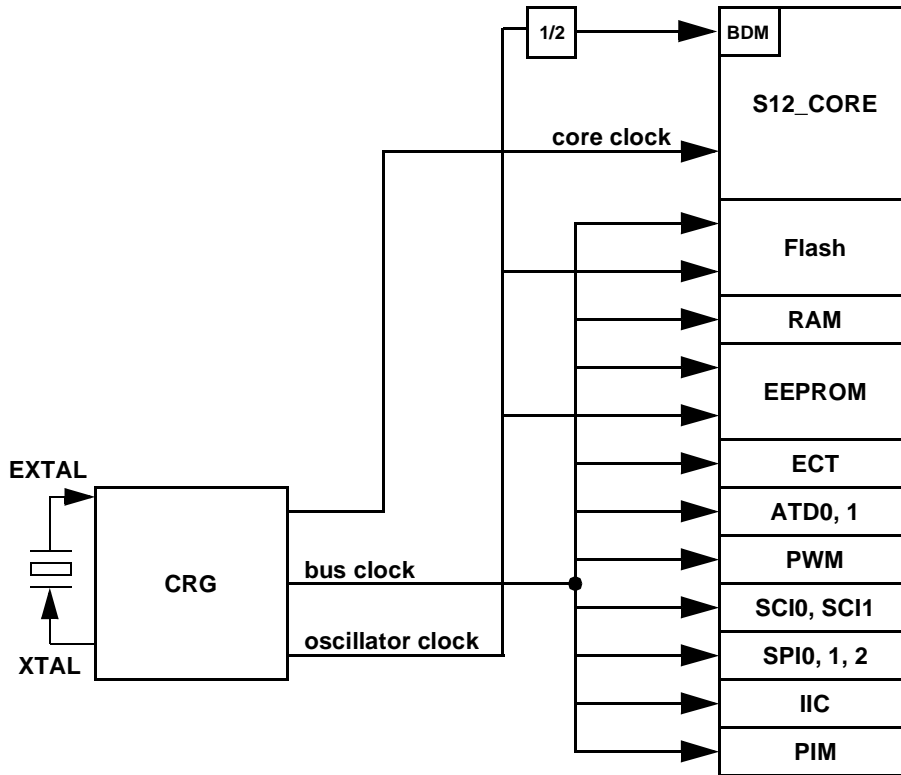


Figure 3-1 Clock Connections





## Section 4 Modes of Operation

### 4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12A256. Each mode has an associated default memory map and external bus configuration.

Three low power modes exist for the device.

### 4.2 Modes of Operation

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (Table 4-1). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 4-1 Mode Selection

| MODC | MODB | MODA | Mode Description  |
|------|------|------|---|
| 0    | 0    | 0    | Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active. |
| 0    | 0    | 1    | Emulation Expanded Narrow, BDM allowed  |
| 0    | 1    | 0    | Special Test (Expanded Wide), BDM allowed   |
| 0    | 1    | 1    | Emulation Expanded Wide, BDM allowed  |
| 1    | 0    | 0    | Normal Single Chip, BDM allowed   |
| 1    | 0    | 1    | Normal Expanded Narrow, BDM allowed   |
| 1    | 1    | 0    | Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)   |
| 1    | 1    | 1    | Normal Expanded Wide, BDM allowed   |

There are two basic types of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

A system development and debug feature, background debug mode (BDM), is available in all modes. In special single-chip mode, BDM is active immediately after reset.

Some aspects of Port E are not mode dependent. Bit 1 of Port E is a general purpose input or the  $\overline{\text{IRQ}}$  interrupt input.  $\overline{\text{IRQ}}$  can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. Bit 0 of Port E is a general purpose input or the  $\overline{\text{XIRQ}}$  interrupt input.  $\overline{\text{XIRQ}}$  can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. The ESTR bit in the EBICTL register is set to one by reset in any user mode. This assures that the reset vector can be fetched

even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as high-impedance mode select inputs during reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

## 4.2.1 Normal Operating Modes

These modes provide three operating configurations. Background debug is available in all three modes, but must first be enabled for some operations by means of a BDM background command, then activated.

### 4.2.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. All pins of Ports A, B and E are configured as general purpose I/O pins. Port E bits 1 and 0 are available as general purpose input only pins with internal pull-ups enabled. All other pins of Port E are bidirectional I/O pins that are initially configured as high-impedance inputs with internal pull-ups enabled. Ports A and B are configured as high-impedance inputs with their internal pull-ups disabled.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, LSTRB, and  $R/\overline{W}$  while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero. Writing the opposite state into them in single chip mode does not change the operation of the associated Port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to narrow or wide expanded mode and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

### 4.2.1.2 Normal Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E bit 4 is configured as the E clock output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general purpose I/O pins (initially high-impedance inputs with internal pull-up resistors enabled). Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure Port E pins to act as bus control outputs instead of general purpose I/O pins.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The Port E bit 2 pin can be reconfigured as the  $R/\overline{W}$  bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit

would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

The Port E bit 3 pin can be reconfigured as the  $\overline{\text{LSTRB}}$  bus control signal by writing “1” to the LSTRE bit in PEAR. The default condition of this pin is a general purpose input because the  $\overline{\text{LSTRB}}$  function is not needed in all expanded wide applications.

The Port E bit 4 pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. The E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

#### 4.2.1.3 Normal Expanded Narrow Mode

This mode is used for lower cost production systems that use 8-bit wide external EPROMs or RAMs. Such systems take extra bus cycles to access 16-bit locations but this may be preferred over the extra cost of additional external memory devices.

Ports A and B are configured as a 16-bit address bus and Port A is multiplexed with data. Internal visibility is not available in this mode because the internal cycles would need to be split into two 8-bit cycles.

Since the PEAR register can only be written one time in this mode, use care to set all bits to the desired states during the single allowed write.

The PE3/ $\overline{\text{LSTRB}}$  pin is always a general purpose I/O pin in normal expanded narrow mode. Although it is possible to write the LSTRE bit in PEAR to “1” in this mode, the state of LSTRE is overridden and Port E bit 3 cannot be reconfigured as the  $\overline{\text{LSTRB}}$  output.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode.  $\overline{\text{LSTRB}}$  would also be needed to fully understand system activity. Development systems where pipe status signals are monitored would typically use special expanded wide mode or occasionally special expanded narrow mode.

The PE4/ECLK pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

The PE2/R/W pin is initially configured as a general purpose input with a pull-up but this pin can be reconfigured as the  $\overline{\text{R/W}}$  bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded narrow system includes external devices that can be written such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

#### 4.2.1.4 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or emulation narrow mode. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while E,  $\overline{R/\overline{W}}$ , and  $\overline{LSTRB}$  are configured as bus control outputs and internal visibility is off (IVIS=0), E will remain low for the cycle,  $\overline{R/\overline{W}}$  will remain high, and address, data and the  $\overline{LSTRB}$  pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected,  $\overline{R/\overline{W}}$  will remain high, data will maintain its previous state, and address and  $\overline{LSTRB}$  pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving,  $\overline{R/\overline{W}}$  will remain high, and address, data and the  $\overline{LSTRB}$  pins will remain at their previous state.

#### 4.2.1.5 Emulation Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. These signals allow external memory and peripheral devices to be interfaced to the MCU. These signals can also be used by a logic analyzer to monitor the progress of application programs.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/ $\overline{LSTRB}/\overline{TAGLO}$ , and PE2/ $\overline{R/\overline{W}}$ ) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in emulation mode are restricted.

#### 4.2.1.6 Emulation Expanded Narrow Mode

Expanded narrow modes are intended to allow connection of single 8-bit external memory devices for lower cost systems that do not need the performance of a full 16-bit external data bus. Accesses to internal resources that have been mapped external (i.e., PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, PUCR, RDRIV) will be accessed with a 16-bit data bus on Ports A and B. Accesses of 16-bit external words to addresses which are normally mapped external will be broken into two separate 8-bit accesses using Port A as an 8-bit data bus. Internal operations continue to use full 16-bit data paths. They are only visible externally as 16-bit information if IVIS=1.

Ports A and B are configured as multiplexed address and data output ports. During external accesses, address A15, data D15 and D7 are associated with PA7, address A0 is associated with PB0 and data D8 and D0 are associated with PA0. During internal visible accesses and accesses to internal resources that have been mapped external, address A15 and data D15 is associated with PA7 and address A0 and data D0 is associated with PB0.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/ $\overline{LSTRB}/\overline{TAGLO}$ , and PE2/ $\overline{R/\overline{W}}$ ) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in emulation mode are restricted.

The main difference between special modes and normal modes is that some of the bus control and system control signals cannot be written in emulation modes.

## 4.2.2 Special Operating Modes

There are two special operating modes that correspond to normal operating modes. These operating modes are commonly used in factory testing and system development.

### 4.2.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull-ups disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with pull-ups enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0,  $\overline{\text{LSTRB}}$ , and  $\text{R}/\overline{\text{W}}$  while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

### 4.2.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

## 4.2.3 Test Operating Mode

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

### 4.2.3.1 Peripheral Mode

This mode is intended for Motorola factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different mode. Background debugging should not be used while the MCU is in special peripheral mode

as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

## 4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

### 4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the *HCS12 256K FLASH Block Guide* (Motorola document order number, S12FTS256KV2/D) for more details on the security configuration.

### 4.3.2 Operation of the Secured Microcontroller

#### 4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

#### 4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

### 4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

### 4.4 Low Power Modes

Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode.





## Section 5 Resets and Interrupts

### 5.1 Overview

Consult the Exception Processing section of the *HCS12 Core User Guide* (Motorola order number, HCS12COREUG/D) for information on resets and interrupts.

### 5.2 Vectors

#### 5.2.1 Vector Table

**Table 5-1** lists interrupt sources and vectors in default order of priority.

**Table 5-1 Interrupt Vector Locations**

| Vector Address | Interrupt Source                 | CCR Mask | Local Enable                     | HPRIO Value to Elevate |
|----------------|----------------------------------|----------|----------------------------------|------------------------|
| \$FFFE, \$FFFF | Reset                            | None     | None                             | –                      |
| \$FFFC, \$FFFD | Clock Monitor fail reset         | None     | PLLCTL (CME, SCME)               | –                      |
| \$FFFA, \$FFFB | COP failure reset                | None     | COP rate select                  | –                      |
| \$FFF8, \$FFF9 | Unimplemented instruction trap   | None     | None                             | –                      |
| \$FFF6, \$FFF7 | SWI                              | None     | None                             | –                      |
| \$FFF4, \$FFF5 | XIRQ                             | X-Bit    | None                             | –                      |
| \$FFF2, \$FFF3 | IRQ                              | I-Bit    | IRQCR (IRQEN)                    | \$F2                   |
| \$FFF0, \$FFF1 | Real Time Interrupt              | I-Bit    | CRGINT (RTIE)                    | \$F0                   |
| \$FFEE, \$FFEF | Enhanced Capture Timer channel 0 | I-Bit    | TIE (C0I)                        | \$EE                   |
| \$FFEC, \$FFED | Enhanced Capture Timer channel 1 | I-Bit    | TIE (C1I)                        | \$EC                   |
| \$FFEA, \$FFEB | Enhanced Capture Timer channel 2 | I-Bit    | TIE (C2I)                        | \$EA                   |
| \$FFE8, \$FFE9 | Enhanced Capture Timer channel 3 | I-Bit    | TIE (C3I)                        | \$E8                   |
| \$FFE6, \$FFE7 | Enhanced Capture Timer channel 4 | I-Bit    | TIE (C4I)                        | \$E6                   |
| \$FFE4, \$FFE5 | Enhanced Capture Timer channel 5 | I-Bit    | TIE (C5I)                        | \$E4                   |
| \$FFE2, \$FFE3 | Enhanced Capture Timer channel 6 | I-Bit    | TIE (C6I)                        | \$E2                   |
| \$FFE0, \$FFE1 | Enhanced Capture Timer channel 7 | I-Bit    | TIE (C7I)                        | \$E0                   |
| \$FFDE, \$FFDF | Enhanced Capture Timer overflow  | I-Bit    | TSRC2 (TOF)                      | \$DE                   |
| \$FFDC, \$FFDD | Pulse accumulator A overflow     | I-Bit    | PACTL (PAOVI)                    | \$DC                   |
| \$FFDA, \$FFDB | Pulse accumulator input edge     | I-Bit    | PACTL (PAI)                      | \$DA                   |
| \$FFD8, \$FFD9 | SPI0                             | I-Bit    | SPOCR1 (SPIE, SPTIE)             | \$D8                   |
| \$FFD6, \$FFD7 | SCI0                             | I-Bit    | SC0CR2<br>(TIE, TCIE, RIE, ILIE) | \$D6                   |
| \$FFD4, \$FFD5 | SCI1                             | I-Bit    | SC1CR2<br>(TIE, TCIE, RIE, ILIE) | \$D4                   |
| \$FFD2, \$FFD3 | ATD0                             | I-Bit    | ATDOCTL2 (ASCIE)                 | \$D2                   |
| \$FFD0, \$FFD1 | ATD1                             | I-Bit    | ATD1CTL2 (ASCIE)                 | \$D0                   |
| \$FFCE, \$FFCF | Port J                           | I-Bit    | PTJIF (PTJIE)                    | \$CE                   |
| \$FFCC, \$FFCD | Port H                           | I-Bit    | PTHIF (PTHIE)                    | \$CC                   |
| \$FFCA, \$FFCB | Modulus Down Counter underflow   | I-Bit    | MCCTL (MCZI)                     | \$CA                   |

|                  |                              |       |                      |      |
|------------------|------------------------------|-------|----------------------|------|
| \$FFC8, \$FFC9   | Pulse Accumulator B Overflow | I-Bit | PBCTL(PBOVI)         | \$C8 |
| \$FFC6, \$FFC7   | CRG PLL lock                 | I-Bit | CRGINT(LOCKIE)       | \$C6 |
| \$FFC4, \$FFC5   | CRG Self Clock Mode          | I-Bit | CRGINT (SCMIE)       | \$C4 |
| \$FFC2, \$FFC3   | Reserved                     |       |                      |      |
| \$FFC0, \$FFC1   | IIC Bus                      | I-Bit | IBCR (IBIE)          | \$C0 |
| \$FFBE, \$FFBF   | SPI1                         | I-Bit | SP1CR1 (SPIE, SPTIE) | \$BE |
| \$FFBC, \$FFBD   | SPI2                         | I-Bit | SP2CR1 (SPIE, SPTIE) | \$BC |
| \$FFBA, \$FFBB   | EEPROM                       | I-Bit | EECTL(CCIE, CBEIE)   | \$BA |
| \$FFB8, \$FFB9   | FLASH                        | I-Bit | FCTL(CCIE, CBEIE)    | \$B8 |
| \$FF90 to \$FFB7 | Reserved                     |       |                      |      |
| \$FF8E, \$FF8F   | Port P Interrupt             | I-Bit | PTPIF (PTPIE)        | \$8E |
| \$FF8C, \$FF8D   | PWM Emergency Shutdown       | I-Bit | PWMSDN (PWMIE)       | \$8C |
| \$FF80 to \$FF8B | Reserved                     |       |                      |      |

### 5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

#### 5.3.1 I/O Pins

Refer to the *HCS12 Core User Guide* (Motorola order number, HCS12COREUG/D) for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the *MC9S12A256 Port Integration Module (PIM) Block Guide* (Motorola document order number, S12A256PIMV1/D) for reset configurations of all peripheral module ports.

**NOTE:** For devices assembled in 80-pin QFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to **Table 2-1** for affected pins.

#### 5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

## Section 6 HCS12 Core Block Description

Consult the *HCS12 Core User Guide* (Motorola order number, HCS12COREUG/D) for information about the HCS12 core modules, i.e., central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), breakpoint module (BKP) and background debug mode module (BDM).

## Section 7 Clock and Reset Generator (CRG) Block Description

Consult the *HCS12 Clock and Reset Generator (CRG) Block Guide* (Motorola document order number, S12CRGV3/D) for information about the Clock and Reset Generator module.

### 7.1 Device-Specific Information

#### 7.1.1 $\overline{\text{XCLKS}}$

The  $\overline{\text{XCLKS}}$  input signal is active low (see [2.3.13 PE7 / NOACC / XCLKS — Port E I/O Pin 7](#)).

Refer to Figure 2-3. Pierce Oscillator Connections (XCLKS=1) of the *HCS12 Clock and Reset Generator (CRG) Block Guide* (Motorola document order number, S12CRGV3/D).

## Section 8 Enhanced Capture Timer (ECT) Block Description

Consult the *HCS12 16-Bit, 8-Channel Enhanced Capture Timer (ECT) Block Guide* (Motorola document order number, S12ECT16B8CV1/D) for information about the Enhanced Capture Timer module.

## Section 9 Analog to Digital Converter (ATD) Block Description

There are two Analog to Digital Converters (ATD1 and ATD0) implemented on the MC9S12A256. Consult the *HCS12 10-Bit, 8-Channel Analog-to-Digital Converter (ATD) Block Guide* (Motorola document order number, S12ATD10B8CV2/D) for information about each Analog to Digital Converter module.

## Section 10 Inter-IC Bus (IIC) Block Description

Consult the *HCS12 Inter-Integrated Circuit (IIC) Block Guide* (Motorola document order number, S12IICV2/D) for information about the Inter-IC Bus module.

## Section 11 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI1 and SCI0) implemented on the MC9S12A256 device. Consult the *HCS12 Serial Communications Interface (SCI) Block Guide* (Motorola document order number, S12SCIV2/D) for information about each Serial Communications Interface module.

## Section 12 Serial Peripheral Interface (SPI) Block Description

There are three Serial Peripheral Interfaces (SPI2, SPI1 and SPI0) implemented on MC9S12A256. Consult the *HCS12 Serial Peripheral Interface (SPI) Block Guide* (Motorola document order number, S12SPIV2/D) for information about each Serial Peripheral Interface module.

## Section 13 Pulse Width Modulator (PWM) Block Description

Consult the *HCS12 8-Bit, 8-Channel Pulse Width Modulator (PWM) Block Guide* (Motorola document order number, S12PWM8B8CV1/D) for information about the Pulse Width Modulator module.

## Section 14 Flash EEPROM 256K Block Description

Consult the *HCS12 256K FLASH Block Guide* (Motorola document order number, S12FTS256KV1/D) for information about the flash module.

## Section 15 EEPROM 4K Block Description

Consult the *HCS12 4K EEPROM Block Guide* (Motorola document order number, S12EETS4KV1/D) for information about the EEPROM module.

## Section 16 RAM Block Description

This module supports single-cycle misaligned word accesses.

## Section 17 Port Integration Module (PIM) Block Description

Consult the *MC9S12A128 Port Integration Module (PIM) Block Guide* (Motorola document order number, S12A128PIMV1/D) for information about the Port Integration Module.

## Section 18 Voltage Regulator ( $V_{REG}$ ) Block Description

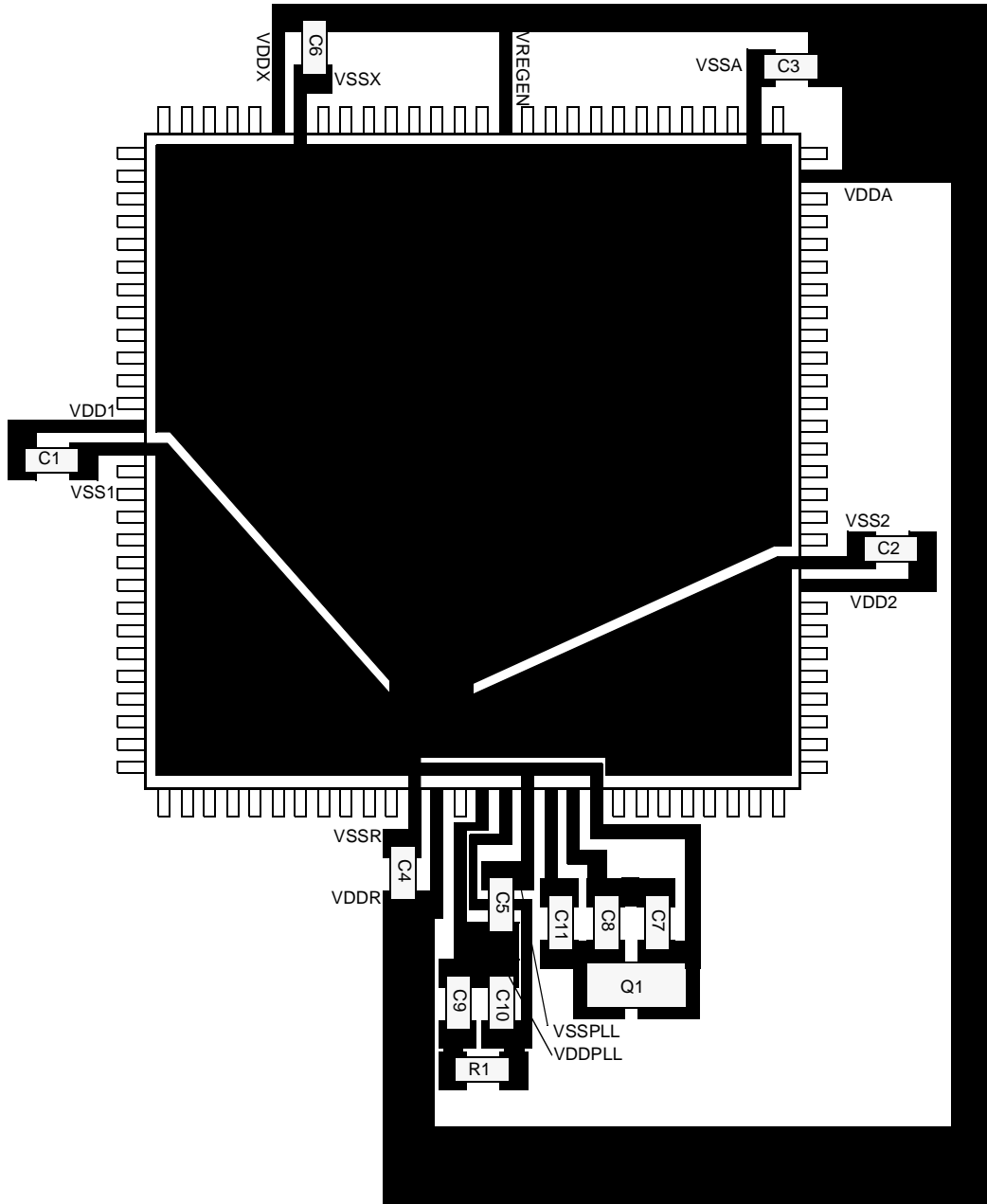
Consult the *HCS12 Voltage Regulator Block Guide* (Motorola document order number, S12VREGV1/D) for information about the dual output linear voltage regulator.

| Component | Purpose                | Type  | Value         |
|-----------|------------------------|---|---------------|
| C1        | $V_{DD1}$ filter cap   | ceramic X7R                                 | 100 .. 220nF  |
| C2        | $V_{DD2}$ filter cap   | ceramic X7R                                 | 100 .. 220nF  |
| C3        | $V_{DDA}$ filter cap   | ceramic X7R                                 | 100nF         |
| C4        | $V_{DDR}$ filter cap   | X7R/tantalum                                | $\geq 100$ nF |
| C5        | $V_{DDPLL}$ filter cap | ceramic X7R                                 | 100nF         |
| C6        | $V_{DDX}$ filter cap   | X7R/tantalum                                | $\geq 100$ nF |
| C7        | OSC load cap           |   |               |
| C8        | OSC load cap           |   |               |
| C9        | PLL loop filter cap    | See <a href="#">A.5.3 Phase Locked Loop</a> |               |
| C10       | PLL loop filter cap    |   |               |
| C11       | DC cutoff cap          |   |               |
| R1        | PLL loop filter res    |   |               |
| Q1        | Quartz                 |   |               |

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

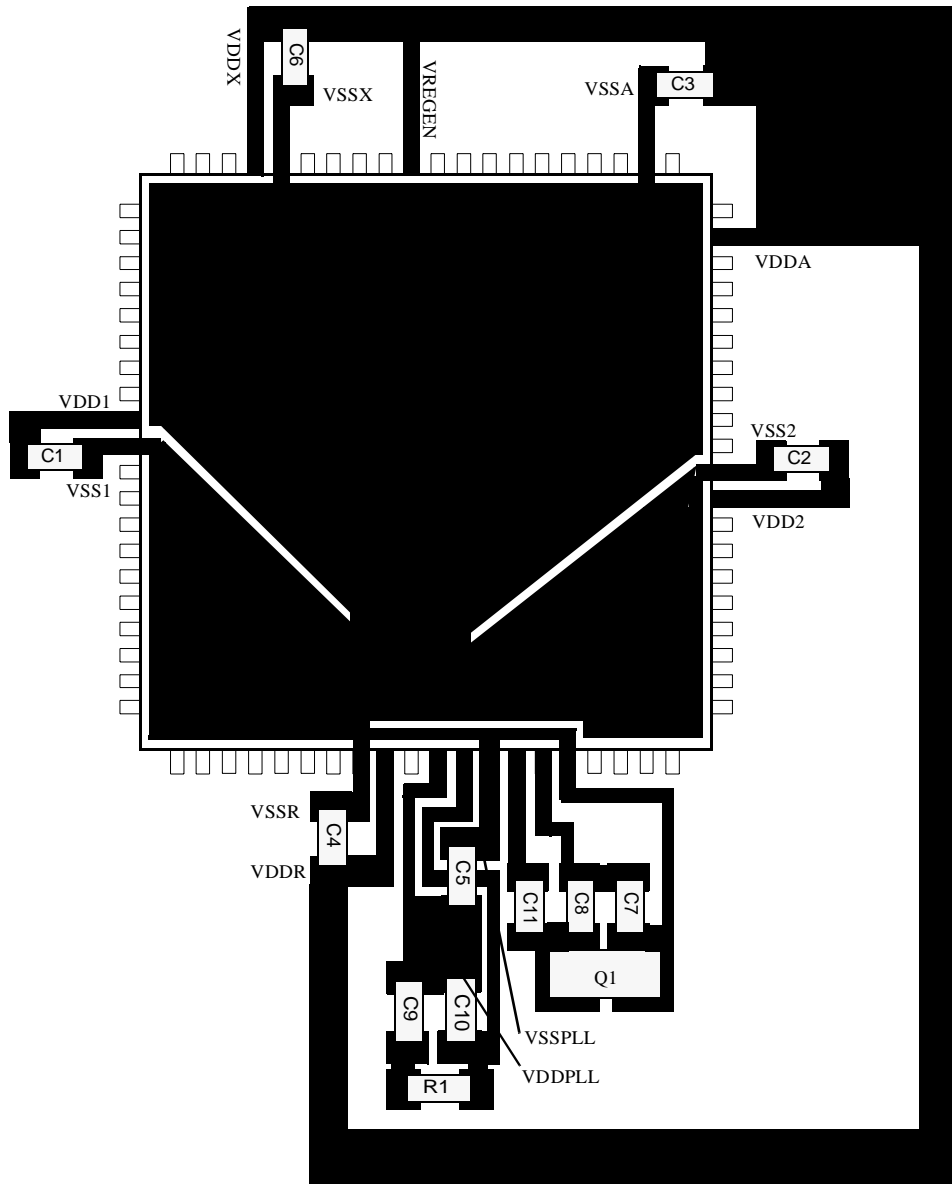
- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins(C1 - C6).
- Central point of the ground star should be the  $V_{SSR}$  pin.
- Use low ohmic low inductance connections between  $V_{SS1}$ ,  $V_{SS2}$ , and  $V_{SSR}$ .
- $V_{SSPLL}$  must be directly connected to  $V_{SSR}$ .
- Keep traces of  $V_{SSPLL}$ , EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the  $V_{DDA}/V_{SSA}$  pins.

Figure 18-1 Recommended PCB Layout 112 LQFP



Freescale Semiconductor, Inc.

**Figure 18-2 Recommended PCB Layout for 80 QFP**





# Appendix A Electrical Characteristics

## A.1 General

**NOTE:** *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Motorola and are subject to change without notice.*

This supplement contains the most accurate electrical information for the MC9S12A256 microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

### A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

**NOTE:** *This classification is shown in the column labeled “C” in the parameter tables where appropriate.*

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

## A.1.2 Power Supply

The MC9S12A256 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the digital core.

The  $V_{DDA}$ ,  $V_{SSA}$  pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

The  $V_{DDX}$ ,  $V_{SSX}$ ,  $V_{DDR}$ , and  $V_{SSR}$  pairs supply the I/O pins,  $V_{DDR}$  supplies also the internal voltage regulator.

$V_{DD1}$ ,  $V_{SS1}$ ,  $V_{DD2}$ , and  $V_{SS2}$  are the supply pins for the digital logic,  $V_{DDPLL}$ ,  $V_{SSPLL}$  supply the oscillator and the PLL.

$V_{SS1}$  and  $V_{SS2}$  are internally connected by metal.

$V_{DDA}$ ,  $V_{DDX}$ ,  $V_{DDR}$  as well as  $V_{SSA}$ ,  $V_{SSX}$ ,  $V_{SSR}$  are connected by anti-parallel diodes for ESD protection.

**NOTE:** *In the following context  $V_{DD5}$  is used for either  $V_{DDA}$ ,  $V_{DDR}$ , and  $V_{DDX}$ ;  $V_{SS5}$  is used for either  $V_{SSA}$ ,  $V_{SSR}$ , and  $V_{SSX}$  unless otherwise noted.  $I_{DD5}$  denotes the sum of the currents flowing into the  $V_{DDA}$ ,  $V_{DDX}$  and  $V_{DDR}$  pins.  $V_{DD}$  is used for  $V_{DD1}$ ,  $V_{DD2}$ , and  $V_{DDPLL}$ ,  $V_{SS}$  is used for  $V_{SS1}$ ,  $V_{SS2}$ , and  $V_{SSPLL}$ .  $I_{DD}$  is used for the sum of the currents flowing into  $V_{DD1}$  and  $V_{DD2}$ .*

## A.1.3 Pins

There are four groups of functional pins.

### A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins. The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

### A.1.3.2 Analog Reference

This group is made up by the  $V_{RH}$  and  $V_{RL}$  pins.

### A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by  $V_{DDPLL}$ .

### A.1.3.4 TEST

This pin is used for production testing only.

### A.1.3.5 $V_{\text{REGEN}}$

This pin is used to enable the on chip voltage regulator.

## A.1.4 Current Injection

Power supply must maintain regulation within operating  $V_{\text{DD5}}$  or  $V_{\text{DD}}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{\text{in}} > V_{\text{DD5}}$ ) is greater than  $I_{\text{DD5}}$ , the injection current may flow out of  $V_{\text{DD5}}$  and could result in external power supply going out of regulation. Ensure external  $V_{\text{DD5}}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

## A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either  $V_{\text{SS5}}$  or  $V_{\text{DD5}}$ ).

**Table A-1 Absolute Maximum Ratings<sup>1</sup>**

| Num | Rating  | Symbol           | Min   | Max  | Unit |
|-----|---|------------------|-------|------|------|
| 1   | I/O, Regulator and Analog Supply Voltage  | $V_{DD5}$        | -0.3  | 6.0  | V    |
| 2   | Digital Logic Supply Voltage <sup>2</sup>   | $V_{DD}$         | -0.3  | 3.0  | V    |
| 3   | PLL Supply Voltage <sup>2</sup>   | $V_{DDPLL}$      | -0.3  | 3.0  | V    |
| 4   | Voltage difference $V_{DDX}$ to $V_{DDR}$ and $V_{DDA}$                                 | $\Delta V_{DDX}$ | -0.3  | 0.3  | V    |
| 5   | Voltage difference $V_{SSX}$ to $V_{SSR}$ and $V_{SSA}$                                 | $\Delta V_{SSX}$ | -0.3  | 0.3  | V    |
| 6   | Digital I/O Input Voltage   | $V_{IN}$         | -0.3  | 6.0  | V    |
| 7   | Analog Reference  | $V_{RH}, V_{RL}$ | -0.3  | 6.0  | V    |
| 8   | XFC, EXTAL, XTAL inputs   | $V_{ILV}$        | -0.3  | 3.0  | V    |
| 9   | TEST input  | $V_{TEST}$       | -0.3  | 10.0 | V    |
| 10  | Instantaneous Maximum Current<br>Single pin limit for all digital I/O pins <sup>3</sup> | $I_D$            | -25   | +25  | mA   |
| 11  | Instantaneous Maximum Current<br>Single pin limit for XFC, EXTAL, XTAL <sup>4</sup>     | $I_{DL}$         | -25   | +25  | mA   |
| 12  | Instantaneous Maximum Current<br>Single pin limit for TEST <sup>5</sup>                 | $I_{DT}$         | -0.25 | 0    | mA   |
| 13  | Storage Temperature Range   | $T_{stg}$        | - 65  | 155  | °C   |

NOTES:

- Beyond absolute maximum ratings device might be damaged.
- The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
- All digital I/O pins are internally clamped to  $V_{SSX}$  and  $V_{DDX}$ ,  $V_{SSR}$  and  $V_{DDR}$  or  $V_{SSA}$  and  $V_{DDA}$ .
- Those pins are internally clamped to  $V_{SSPLL}$  and  $V_{DDPLL}$ .
- This pin is clamped low to  $V_{SSPLL}$ , but not clamped high. This pin must be tied low in applications.

## A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table A-2 ESD and Latch-up Test Conditions**

| Model      | Description                                     | Symbol | Value       | Unit |
|------------|---|--------|-------------|------|
| Human Body | Series Resistance                               | R1     | 1500        | Ohm  |
|            | Storage Capacitance                             | C      | 100         | pF   |
|            | Number of Pulse per pin<br>positive<br>negative | -      | -<br>3<br>3 |      |
| Machine    | Series Resistance                               | R1     | 0           | Ohm  |
|            | Storage Capacitance                             | C      | 200         | pF   |
|            | Number of Pulse per pin<br>positive<br>negative | -      | -<br>3<br>3 |      |
| Latch-up   | Minimum input voltage limit                     |        | -2.5        | V    |
|            | Maximum input voltage limit                     |        | 7.5         | V    |

**Table A-3 ESD and Latch-Up Protection Characteristics**

| Num | C | Rating  | Symbol    | Min          | Max | Unit |
|-----|---|---|-----------|--------------|-----|------|
| 1   | C | Human Body Model (HBM)  | $V_{HBM}$ | 2000         | -   | V    |
| 2   | C | Machine Model (MM)  | $V_{MM}$  | 200          | -   | V    |
| 3   | C | Charge Device Model (CDM)   | $V_{CDM}$ | 500          | -   | V    |
| 4   | C | Latch-up Current at $T_A = 125^\circ\text{C}$<br>positive<br>negative | $I_{LAT}$ | +100<br>-100 | -   | mA   |
| 5   | C | Latch-up Current at $T_A = 27^\circ\text{C}$<br>positive<br>negative  | $I_{LAT}$ | +200<br>-200 | -   | mA   |

## A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

**NOTE:** Please refer to the temperature rating of the device (C) with regards to the ambient temperature  $T_A$  and the junction temperature  $T_J$ . For power dissipation calculations refer to [A.1.8 Power Dissipation and Thermal Characteristics](#).

**Table A-4 Operating Conditions**

| Rating  | Symbol           | Min  | Typ | Max  | Unit |
|---|------------------|------|-----|------|------|
| I/O, Regulator and Analog Supply Voltage                | $V_{DD5}$        | 4.5  | 5   | 5.25 | V    |
| Digital Logic Supply Voltage <sup>1</sup>               | $V_{DD}$         | 2.35 | 2.5 | 2.75 | V    |
| PLL Supply Voltage <sup>2</sup>                         | $V_{DDPLL}$      | 2.35 | 2.5 | 2.75 | V    |
| Voltage Difference $V_{DDX}$ to $V_{DDR}$ and $V_{DDA}$ | $\Delta V_{DDX}$ | -0.1 | 0   | 0.1  | V    |
| Voltage Difference $V_{SSX}$ to $V_{SSR}$ and $V_{SSA}$ | $\Delta V_{SSX}$ | -0.1 | 0   | 0.1  | V    |
| Oscillator  | $f_{osc}$        | 0.5  | -   | 16   | MHz  |
| Bus Frequency   | $f_{bus}$        | 0.5  | -   | 25   | MHz  |
| <b>MC9S12A256C</b>                                      |                  |      |     |      |      |
| Operating Junction Temperature Range                    | $T_J$            | -40  | -   | 100  | °C   |
| Operating Ambient Temperature Range <sup>2</sup>        | $T_A$            | -40  | 27  | 85   | °C   |

**NOTES:**

1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.
2. Please refer to [A.1.8 Power Dissipation and Thermal Characteristics](#) for more details about the relation between ambient temperature  $T_A$  and device junction temperature  $T_J$ .

## A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \Theta_{JA})$$

$T_J$  = Junction Temperature, [°C]

$T_A$  = Ambient Temperature, [°C]

$P_D$  = Total Chip Power Dissipation, [W]

$\Theta_{JA}$  = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

$P_{INT}$  = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

$P_{IO}$  is the sum of all output currents on I/O ports associated with  $V_{DDX}$  and  $V_{DDR}$ .

For  $R_{DSON}$  is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

$I_{DDR}$  is the current shown in **Table A-7** and not the overall current flowing into  $V_{DDR}$ , which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

$P_{IO}$  is the sum of all output currents on I/O ports associated with  $V_{DDX}$  and  $V_{DDR}$ .

**Table A-5 Thermal Package Characteristics<sup>1</sup>**

| Num | C | Rating   | Symbol        | Min | Typ | Max | Unit |
|-----|---|--|---------------|-----|-----|-----|------|
| 1   | T | Thermal Resistance LQFP112, single sided PCB <sup>2</sup>                        | $\theta_{JA}$ | -   | -   | 54  | °C/W |
| 2   | T | Thermal Resistance LQFP112, double sided PCB with 2 internal planes <sup>3</sup> | $\theta_{JA}$ | -   | -   | 41  | °C/W |
| 3   | T | Thermal Resistance LQFP 80, single sided PCB                                     | $\theta_{JA}$ | -   | -   | 51  | °C/W |
| 4   | T | Thermal Resistance LQFP 80, double sided PCB with 2 internal planes              | $\theta_{JA}$ | -   | -   | 41  | °C/W |

NOTES:

1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

### A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g., not all pins feature pull up/down resistances.



Table A-6 5V I/O Characteristics

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |   |   |                        |                      |     |                      |         |
|--|---|---|------------------------|----------------------|-----|----------------------|---------|
| Num  | C | Rating  | Symbol                 | Min                  | Typ | Max                  | Unit    |
| 1  | P | Input High Voltage  | $V_{IH}$               | $0.65 \cdot V_{DD5}$ | -   | -                    | V       |
|  | T | Input High Voltage  | $V_{IH}$               | -                    | -   | $V_{DD5} + 0.3$      | V       |
| 2  | P | Input Low Voltage   | $V_{IL}$               | -                    | -   | $0.35 \cdot V_{DD5}$ | V       |
|  | T | Input Low Voltage   | $V_{IL}$               | $V_{SS5} - 0.3$      | -   | -                    | V       |
| 3  | C | Input Hysteresis  | $V_{HYS}$              |                      | 250 |                      | mV      |
| 4  | P | Input Leakage Current (pins in high impedance input mode) <sup>1</sup><br>$V_{in} = V_{DD5}$ or $V_{SS5}$   | $I_{in}$               | -2.5                 | -   | 2.5                  | $\mu$ A |
| 5  | P | Output High Voltage (pins in output mode)<br>Partial Drive $I_{OH} = +2$ mA<br>Full Drive $I_{OH} = +10$ mA | $V_{OH}$               | $V_{DD5} - 0.8$      | -   | -                    | V       |
| 6  | P | Output Low Voltage (pins in output mode)<br>Partial Drive $I_{OL} = +2$ mA<br>Full Drive $I_{OL} = +10$ mA  | $V_{OL}$               | -                    | -   | 0.8                  | V       |
| 7  | P | Internal Pull Up Device Current, tested at $V_{IL}$ Max.  | $I_{PUL}$              | -                    | -   | -130                 | $\mu$ A |
| 8  | P | Internal Pull Up Device Current, tested at $V_{IH}$ Min.  | $I_{PUH}$              | -10                  | -   | -                    | $\mu$ A |
| 9  | P | Internal Pull Down Device Current, tested at $V_{IH}$ Min.  | $I_{PDH}$              | -                    | -   | 130                  | $\mu$ A |
| 10   | P | Internal Pull Down Device Current, tested at $V_{IL}$ Max.  | $I_{PDL}$              | 10                   | -   | -                    | $\mu$ A |
| 11   | D | Input Capacitance   | $C_{in}$               |                      | 6   | -                    | pF      |
| 12   | T | Injection current <sup>2</sup><br>Single Pin limit<br>Total Device Limit. Sum of all injected currents      | $I_{ICS}$<br>$I_{ICP}$ | -2.5<br>-25          | -   | 2.5<br>25            | mA      |
| 13   | P | Port H, J, P Interrupt Input Pulse filtered <sup>3</sup>  | $t_{PULSE}$            |                      |     | 3                    | $\mu$ s |
| 14   | P | Port H, J, P Interrupt Input Pulse passed <sup>3</sup>  | $t_{PULSE}$            | 10                   |     |                      | $\mu$ s |

## NOTES:

- Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8°C to 12°C in the temperature range from 50°C to 125°C.
- Refer to [A.1.4 Current Injection](#), for more details
- Parameter only applies in STOP or Pseudo STOP mode.

## A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

### A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

### A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

**Table A-7 Supply Current Characteristics**

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |                            |   |            |     |  |             |      |
|--|----------------------------|---|------------|-----|--|-------------|------|
| Num  | C                          | Rating  | Symbol     | Min | Typ                                    | Max         | Unit |
| 1  | P                          | Run supply currents<br>Single Chip, Internal regulator enabled  | $I_{DD5}$  |     |  | 65          | mA   |
| 2  | P<br>P                     | Wait Supply current<br>All modules enabled, PLL on<br>only RTI enabled <sup>1</sup>   | $I_{DDW}$  |     |  | 40<br>5     | mA   |
| 3  | C<br>P<br>C<br>C<br>P<br>C | Pseudo Stop Current (RTI and COP disabled) <sup>1, 2</sup><br>-40°C<br>27°C<br>70°C<br>85°C<br>"C" Temp Option 100°C<br>105°C | $I_{DDPS}$ |     | 370<br>400<br>450<br>550<br>600<br>650 | 500<br>1600 | μA   |
| 4  | C<br>C<br>C<br>C<br>C<br>C | Pseudo Stop Current (RTI and COP enabled) <sup>1, 2</sup><br>-40°C<br>27°C<br>70°C<br>85°C<br>105°C                           | $I_{DDPS}$ |     | 570<br>600<br>650<br>750<br>850        |             | μA   |
| 5  | C<br>P<br>C<br>C<br>P<br>C | Stop Current <sup>2</sup><br>-40°C<br>27°C<br>70°C<br>85°C<br>"C" Temp Option 100°C<br>105°C                                  | $I_{DDS}$  |     | 12<br>25<br>100<br>130<br>160<br>200   | 100<br>1200 | μA   |

NOTES:

1. PLL off
2. At those low power dissipation levels  $T_J = T_A$  can be assumed

## A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

### A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:

$V_{SSA} \leq V_{RL} \leq V_{IN} \leq V_{RH} \leq V_{DDA}$ . This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

**Table A-8 ATD Operating Characteristics**

| Conditions are shown in <b>Table A-4</b> unless otherwise noted |   |  |                              |                          |      |                          |                   |
|---|---|--|------------------------------|--------------------------|------|--------------------------|-------------------|
| Num   | C | Rating   | Symbol                       | Min                      | Typ  | Max                      | Unit              |
| 1   | D | Reference Potential<br>Low<br>High   | $V_{RL}$<br>$V_{RH}$         | $V_{SSA}$<br>$V_{DDA}/2$ |      | $V_{DDA}/2$<br>$V_{DDA}$ | V<br>V            |
| 2   | C | Differential Reference Voltage <sup>1</sup>  | $V_{RH}-V_{RL}$              | 4.50                     | 5.00 | 5.25                     | V                 |
| 3   | D | ATD Clock Frequency  | $f_{ATDCLK}$                 | 0.5                      |      | 2.0                      | MHz               |
| 4   | D | ATD 10-Bit Conversion Period<br>Clock Cycles <sup>2</sup><br>Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$ | $N_{CONV10}$<br>$T_{CONV10}$ | 14<br>7                  |      | 28<br>14                 | Cycles<br>$\mu s$ |
| 5   | D | ATD 8-Bit Conversion Period<br>Clock Cycles <sup>2</sup><br>Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$  | $N_{CONV8}$<br>$T_{CONV8}$   | 12<br>6                  |      | 26<br>13                 | Cycles<br>$\mu s$ |
| 6   | D | Recovery Time ( $V_{DDA}=5.0$ Volts)   | $t_{REC}$                    |                          |      | 20                       | $\mu s$           |
| 7   | P | Reference Supply current 2 ATD blocks on   | $I_{REF}$                    |                          |      | 0.750                    | mA                |
| 8   | P | Reference Supply current 1 ATD block on  | $I_{REF}$                    |                          |      | 0.375                    | mA                |

NOTES:

1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

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## A.2.2 Factors Influencing Accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

### A.2.2.1 Source Resistance

Due to the input pin leakage current as specified in [Table A-6](#) in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance  $R_S$  specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

### A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage  $\leq 1_{LSB}$ , then the external filter capacitor,  $C_f \geq 1024 * (C_{INS} - C_{INN})$ .

### A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of \$3FF (\$FF in 8-bit mode) for analog inputs greater than  $V_{RH}$  and \$000 for values less than  $V_{RL}$  unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.

The additional input voltage error on the converted channel can be calculated as  $V_{ERR} = K * R_S * I_{INJ}$ , with  $I_{INJ}$  being the sum of the currents injected into the two pins adjacent to the converted channel.

**Table A-9 ATD Electrical Characteristics**

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |   |   |                        |      |     |           |            |
|--|---|---|------------------------|------|-----|-----------|------------|
| Num  | C | Rating  | Symbol                 | Min  | Typ | Max       | Unit       |
| 1  | C | Max input Source Resistance                         | $R_S$                  | -    | -   | 1         | K $\Omega$ |
| 2  | T | Total Input Capacitance<br>Non Sampling<br>Sampling | $C_{INN}$<br>$C_{INS}$ |      |     | 10<br>22  | pF         |
| 3  | C | Disruptive Analog Input Current                     | $I_{NA}$               | -2.5 |     | 2.5       | mA         |
| 4  | C | Coupling Ratio positive current injection           | $K_p$                  |      |     | $10^{-4}$ | A/A        |
| 5  | C | Coupling Ratio negative current injection           | $K_n$                  |      |     | $10^{-2}$ | A/A        |

### A.2.3 ATD Accuracy

**Table A-10** specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

**Table A-10 ATD Conversion Performance**

| Conditions are shown in <b>Table A-4</b> unless otherwise noted                                      |   |                                    |        |      |      |     |        |
|--|---|------------------------------------|--------|------|------|-----|--------|
| $V_{REF} = V_{RH} - V_{RL} = 5.12V$ . Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV |   |                                    |        |      |      |     |        |
| $f_{ATDCLK} = 2.0MHz$  |   |                                    |        |      |      |     |        |
| Num  | C | Rating                             | Symbol | Min  | Typ  | Max | Unit   |
| 1  | P | 10-Bit Resolution                  | LSB    |      | 5    |     | mV     |
| 2  | P | 10-Bit Differential Nonlinearity   | DNL    | -1   |      | 1   | Counts |
| 3  | P | 10-Bit Integral Nonlinearity       | INL    | -2.5 | ±1.5 | 2.5 | Counts |
| 4  | P | 10-Bit Absolute Error <sup>1</sup> | AE     | -3   | ±2.0 | 3   | Counts |
| 5  | P | 8-Bit Resolution                   | LSB    |      | 20   |     | mV     |
| 6  | P | 8-Bit Differential Nonlinearity    | DNL    | -0.5 |      | 0.5 | Counts |
| 7  | P | 8-Bit Integral Nonlinearity        | INL    | -1.0 | ±0.5 | 1.0 | Counts |
| 8  | P | 8-Bit Absolute Error <sup>1</sup>  | AE     | -1.5 | ±1.0 | 1.5 | Counts |

NOTES:

1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

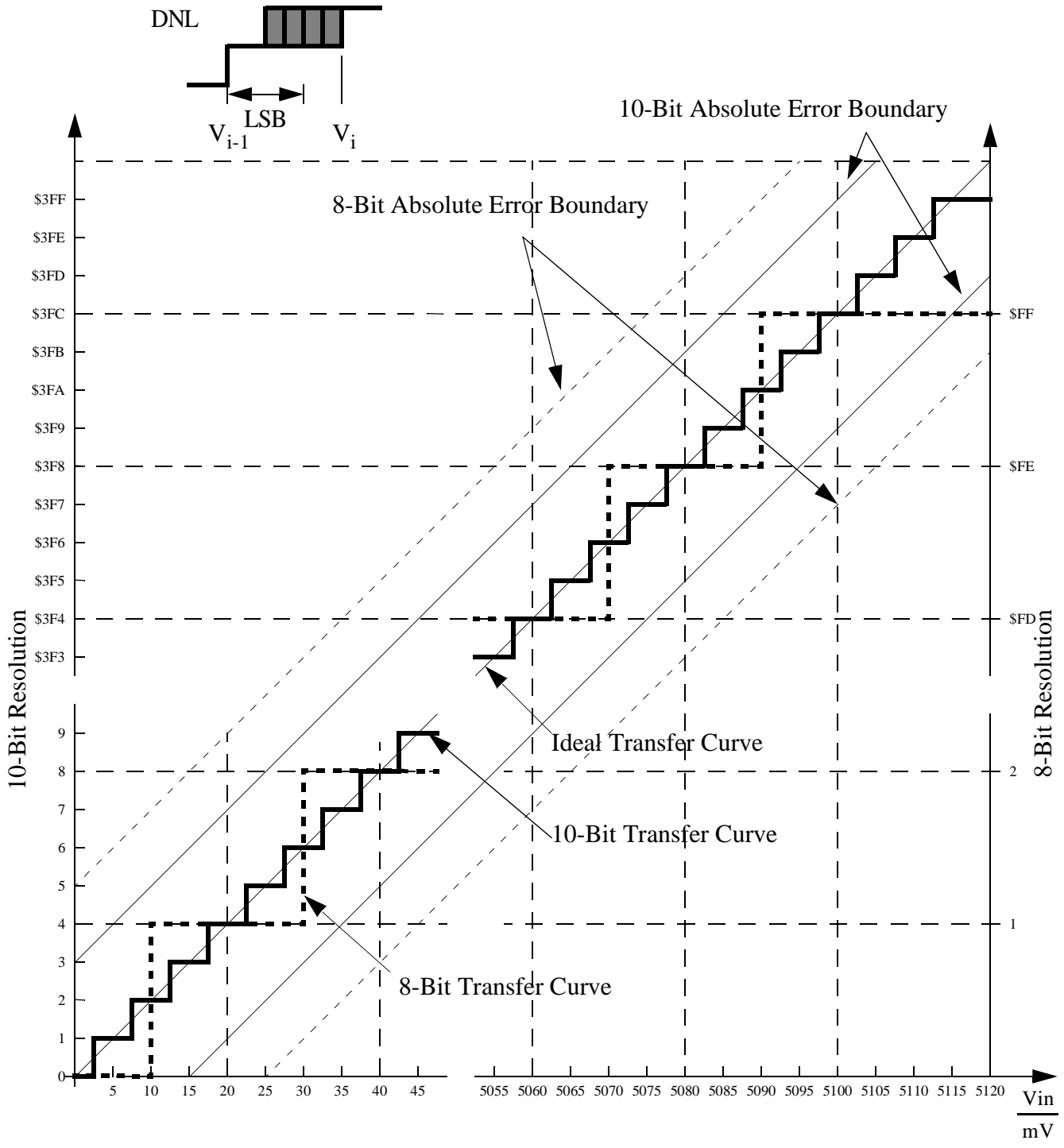
For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^n DNL(i) = \frac{V_n - V_0}{1LSB} - n$$



**Figure A-1 ATD Accuracy Definitions**

**NOTE:** *Figure A-1 shows only definitions, for specification values refer to [Table A-10](#).*

## A.3 NVM, Flash, and EEPROM

**NOTE:** Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.

### A.3.1 NVM Timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency  $f_{\text{NVMOSC}}$  is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as  $f_{\text{NVMOP}}$ .

The minimum program and erase times shown in **Table A-11** are calculated for maximum  $f_{\text{NVMOP}}$  and maximum  $f_{\text{bus}}$ . The maximum times are calculated for minimum  $f_{\text{NVMOP}}$  and a  $f_{\text{bus}}$  of 2MHz.

#### A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency  $f_{\text{NVMOP}}$  and can be calculated according to the following formula.

$$t_{\text{swpgm}} = 9 \cdot \frac{1}{f_{\text{NVMOP}}} + 25 \cdot \frac{1}{f_{\text{bus}}}$$

#### A.3.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{\text{bwpgm}} = 4 \cdot \frac{1}{f_{\text{NVMOP}}} + 9 \cdot \frac{1}{f_{\text{bus}}}$$

The time to program a whole row is:

$$t_{\text{brpgm}} = t_{\text{swpgm}} + 31 \cdot t_{\text{bwpgm}}$$

Burst programming is more than 2 times faster than single word programming.

### A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{\text{era}} \approx 4000 \cdot \frac{1}{f_{\text{NVMOP}}}$$

The setup time can be ignored for this operation.

### A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{\text{mass}} \approx 20000 \cdot \frac{1}{f_{\text{NVMOP}}}$$

The setup time can be ignored for this operation.

### A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{\text{check}} \approx \text{location} \cdot t_{\text{cyc}} + 10 \cdot t_{\text{cyc}}$$



Table A-11 NVM Timing Characteristics

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |   |  |              |                    |     |                     |           |
|--|---|--|--------------|--------------------|-----|---------------------|-----------|
| Num  | C | Rating   | Symbol       | Min                | Typ | Max                 | Unit      |
| 1  | D | External Oscillator Clock                              | $f_{NVMOSC}$ | 0.5                |     | 50 <sup>1</sup>     | MHz       |
| 2  | D | Bus frequency for Programming or Erase Operations      | $f_{NVMBUS}$ | 1                  |     |                     | MHz       |
| 3  | D | Operating Frequency                                    | $f_{NVMOP}$  | 150                |     | 200                 | kHz       |
| 4  | P | Single Word Programming Time                           | $t_{swpgm}$  | 46 <sup>2</sup>    |     | 74.5 <sup>3</sup>   | $\mu$ s   |
| 5  | D | Flash Burst Programming consecutive word <sup>4</sup>  | $t_{bwpgm}$  | 20.4 <sup>2</sup>  |     | 31 <sup>3</sup>     | $\mu$ s   |
| 6  | D | Flash Burst Programming Time for 32 Words <sup>4</sup> | $t_{brpgm}$  | 678.4 <sup>2</sup> |     | 1035.5 <sup>3</sup> | $\mu$ s   |
| 7  | P | Sector Erase Time                                      | $t_{era}$    | 20 <sup>5</sup>    |     | 26.7 <sup>3</sup>   | ms        |
| 8  | P | Mass Erase Time  | $t_{mass}$   | 100 <sup>5</sup>   |     | 133 <sup>3</sup>    | ms        |
| 9  | D | Blank Check Time Flash per block                       | $t_{check}$  | 11 <sup>6</sup>    |     | 32778 <sup>7</sup>  | $t_{cyc}$ |
| 10   | D | Blank Check Time EEPROM per block                      | $t_{check}$  | 11 <sup>6</sup>    |     | 2058 <sup>7</sup>   | $t_{cyc}$ |

## NOTES:

- Restrictions for oscillator in crystal mode apply!
- Minimum Programming times are achieved under maximum NVM operating frequency  $f_{NVMOP}$  and maximum bus frequency  $f_{bus}$ .
- Maximum Erase and Programming times are achieved under particular combinations of  $f_{NVMOP}$  and bus frequency  $f_{bus}$ . Refer to formulae in [A.3.1.1 Single Word Programming](#)- [A.3.1.4 Mass Erase](#) for guidance.
- urst Programming operations are not applicable to EEPROM
- Minimum Erase times are achieved under maximum NVM operating frequency  $f_{NVMOP}$ .
- Minimum time, if first word in the array is not blank
- Maximum time to complete check on an erased block

### A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

**NOTE:** All values shown in [Table A-12](#) are target values and subject to further extensive characterization.

**Table A-12 NVM Reliability Characteristics**

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |   |                             |        |                         |
|--|---|-----------------------------|--------|-------------------------|
| Num  | C | NVM Array                   | Cycles | Data Retention Lifetime |
| 1  | C | Flash/EEPROM (–40 to +85°C) | 1000   | 10 years                |
| 2  | C | EEPROM (–40 to +85°C)       | 10,000 | 10 years                |

**NOTE:** Flash cycling performance is 1000 cycles at –40 to + 85°C. Data Retention is specified for 10 years.

**NOTE:** EEPROM cycling performance is 10,000 cycles at –40 to +85°C. Data retention is specified for 10 years.

**NOTE:** These figures are provided for commercial quality levels not automotive.

## A.4 Voltage Regulator

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits. No external DC load is allowed.

**Table A-13 Voltage Regulator Recommended Load Capacitances**

| Rating                           | Symbol        | Min | Typ | Max | Unit |
|----------------------------------|---------------|-----|-----|-----|------|
| Load Capacitance on $V_{DD1, 2}$ | $C_{LVDD}$    |     | 220 |     | nF   |
| Load Capacitance on $V_{DDPLL}$  | $C_{LVDDPLL}$ |     | 220 |     | nF   |

## A.5 Reset, Oscillator, and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

### A.5.1 Startup

**Table A-14** summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the *HCS12 Clock and Reset Generator (CRG) Block Guide* (Motorola document order number, S12CRGV3/D).

**Table A-14 Startup Characteristics**

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |   |   |             |      |     |      |           |
|--|---|---|-------------|------|-----|------|-----------|
| Num  | C | Rating  | Symbol      | Min  | Typ | Max  | Unit      |
| 1  | T | POR release level   | $V_{PORR}$  |      |     | 2.07 | V         |
| 2  | T | POR assert level  | $V_{PORA}$  | 0.97 |     |      | V         |
| 3  | D | Reset input pulse width, minimum input time                 | $PW_{RSTL}$ | 2    |     |      | $t_{osc}$ |
| 4  | D | Startup from Reset  | $n_{RST}$   | 192  |     | 196  | $n_{osc}$ |
| 5  | D | Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode | $PW_{IRQ}$  | 20   |     |      | ns        |
| 6  | D | Wait recovery startup time                                  | $t_{WRS}$   |      |     | 14   | $t_{cyc}$ |

#### A.5.1.1 POR

The release level  $V_{PORR}$  and the assert level  $V_{PORA}$  are derived from the  $V_{DD}$  supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time  $t_{CQOUT}$  no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by  $n_{uposc}$ .

#### A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when  $V_{DD5}$  is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

#### A.5.1.3 External Reset

When external reset is asserted for a time greater than  $PW_{RSTL}$  the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

### A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

### A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After  $t_{WRS}$  the CPU starts fetching the interrupt vector.

## A.5.2 Oscillator

The device features an internal Colpitts oscillator. By asserting the  $\overline{XCLKS}$  input during reset this oscillator can be bypassed allowing the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail.  $t_{CQOUT}$  specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time  $t_{UPOSC}$ . The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency  $f_{CMFA}$ .

**Table A-15 Oscillator Characteristics**

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted |   |  |              |      |       |         |         |
|--|---|--|--------------|------|-------|---------|---------|
| Num  | C | Rating   | Symbol       | Min  | Typ   | Max     | Unit    |
| 1  | C | Crystal oscillator range                                 | $f_{OSC}$    | 0.5  |       | 16      | MHz     |
| 2  | P | Startup Current  | $i_{OSC}$    | 100  |       |         | $\mu A$ |
| 3  | C | Oscillator start-up time                                 | $t_{UPOSC}$  |      | $8^1$ | $100^2$ | ms      |
| 4  | D | Clock Quality check time-out                             | $t_{CQOUT}$  | 0.45 |       | 2.5     | s       |
| 5  | P | Clock Monitor Failure Assert Frequency                   | $f_{CMFA}$   | 50   | 100   | 200     | KHz     |
| 6  | P | External square wave input frequency <sup>3</sup>        | $f_{EXT}$    | 0.5  |       | 50      | MHz     |
| 7  | D | External square wave pulse width low                     | $t_{EXTL}$   | 9.5  |       |         | ns      |
| 8  | D | External square wave pulse width high                    | $t_{EXTH}$   | 9.5  |       |         | ns      |
| 9  | D | External square wave rise time                           | $t_{EXTR}$   |      |       | 1       | ns      |
| 10   | D | External square wave fall time                           | $t_{EXTF}$   |      |       | 1       | ns      |
| 11   | D | Input Capacitance (EXTAL, XTAL pins)                     | $C_{IN}$     |      | 9     |         | pF      |
| 12   | C | DC Operating Bias in Colpitts Configuration on EXTAL Pin | $V_{DCBIAS}$ |      | 1.1   |         | V       |

NOTES:

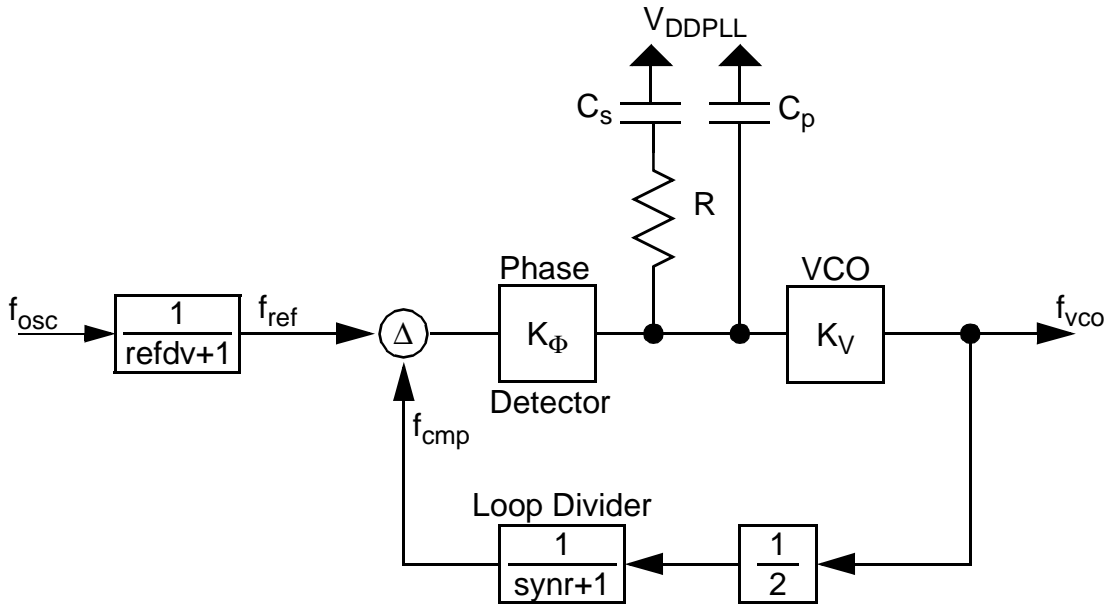
- $f_{OSC} = 4\text{MHz}$ ,  $C = 22\text{pF}$ .
- Maximum value is for extreme cases using high Q, low frequency crystals
- $XCLKS = 0$  during reset

### A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL's Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

#### A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.



**Figure A-2 Basic PLL Functional Diagram**

The following procedure can be used to calculate the resistance and capacitance values using typical values for  $K_1$ ,  $f_1$  and  $i_{ch}$  from [Table A-16](#).

The VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{VCO})}{K_1 \cdot 1V}}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V$$

$i_{ch}$  is the current in tracking mode.

The loop bandwidth  $f_C$  should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50.  $\zeta = 0.9$  ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{\text{ref}}}{\pi \cdot (\zeta + \sqrt{1 + \zeta^2})} \cdot \frac{1}{50} \rightarrow f_C < \frac{f_{\text{ref}}}{4 \cdot 50}; (\zeta = 0.9)$$

And finally the frequency relationship is defined as

$$n = \frac{f_{\text{VCO}}}{f_{\text{ref}}} = 2 \cdot (\text{synr} + 1)$$

With the above inputs the resistance can be calculated as:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_{\Phi}}$$

The capacitance  $C_s$  can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9)$$

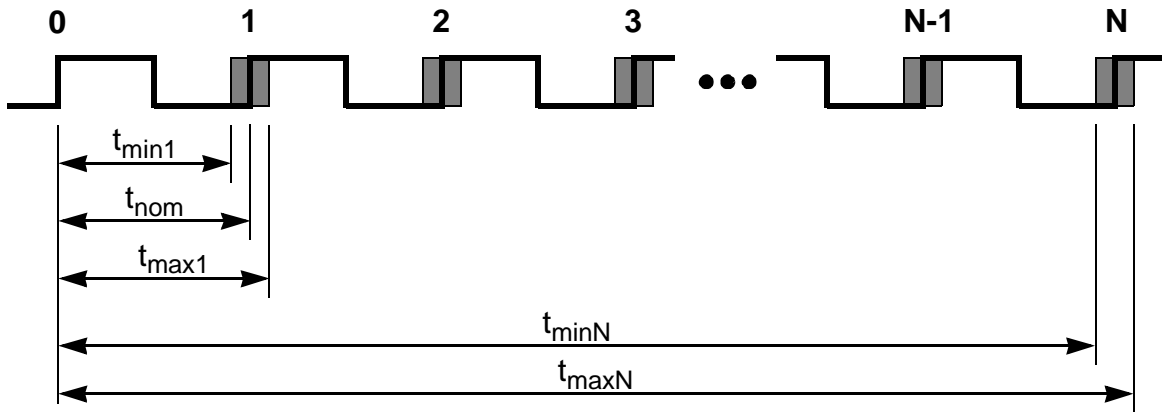
The capacitance  $C_p$  should be chosen in the range of:

$$C_s / 20 \leq C_p \leq C_s / 10$$

The stabilization delays shown in [Table A-16](#) are dependant on PLL operational settings and external component selection (e.g. crystal, XFC filter).

### A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in [Figure A-2](#). With each transition of the clock  $f_{\text{cmp}}$ , the deviation from the reference clock  $f_{\text{ref}}$  is measured and input voltage to the VCO is adjusted accordingly. The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in [Figure A-3](#).



**Figure A-3 Jitter Definitions**

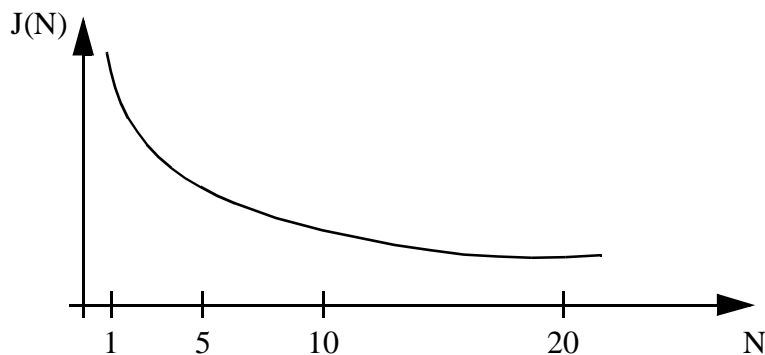
The relative deviation of  $t_{nom}$  is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For  $N < 100$ , the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$



**Figure A-4 Maximum Bus Clock Jitter Approximation**

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.



Table A-16 PLL Characteristics

| Conditions are shown in Table A-4 unless otherwise noted |   |  |                   |     |      |      |                |
|--|---|--|-------------------|-----|------|------|----------------|
| Num  | C | Rating   | Symbol            | Min | Typ  | Max  | Unit           |
| 1  | P | Self Clock Mode frequency                                  | $f_{SCM}$         | 1   |      | 5.5  | MHz            |
| 2  | D | VCO locking range  | $f_{VCO}$         | 8   |      | 50   | MHz            |
| 3  | D | Lock Detector transition from Acquisition to Tracking mode | $ \Delta_{trk} $  | 3   |      | 4    | % <sup>1</sup> |
| 4  | D | Lock Detection   | $ \Delta_{Lock} $ | 0   |      | 1.5  | % <sup>1</sup> |
| 5  | D | Un-Lock Detection  | $ \Delta_{unt} $  | 0.5 |      | 2.5  | % <sup>1</sup> |
| 6  | D | Lock Detector transition from Tracking to Acquisition mode | $ \Delta_{unt} $  | 6   |      | 8    | % <sup>1</sup> |
| 7  | C | PLLON Total Stabilization delay (Auto Mode) <sup>2</sup>   | $t_{stab}$        |     | 0.5  |      | ms             |
| 8  | D | PLLON Acquisition mode stabilization delay <sup>2</sup>    | $t_{acq}$         |     | 0.3  |      | ms             |
| 9  | D | PLLON Tracking mode stabilization delay <sup>2</sup>       | $t_{al}$          |     | 0.2  |      | ms             |
| 10   | D | Fitting parameter VCO loop gain                            | $K_1$             |     | -120 |      | MHz/V          |
| 11   | D | Fitting parameter VCO loop frequency                       | $f_1$             |     | 75   |      | MHz            |
| 12   | D | Charge pump current acquisition mode                       | $ i_{ch} $        |     | 38.5 |      | $\mu$ A        |
| 13   | D | Charge pump current tracking mode                          | $ i_{ch} $        |     | 3.5  |      | $\mu$ A        |
| 14   | C | Jitter fit parameter 1 <sup>2</sup>                        | $j_1$             |     |      | 1.1  | %              |
| 15   | C | Jitter fit parameter 2 <sup>2</sup>                        | $j_2$             |     |      | 0.13 | %              |

## NOTES:

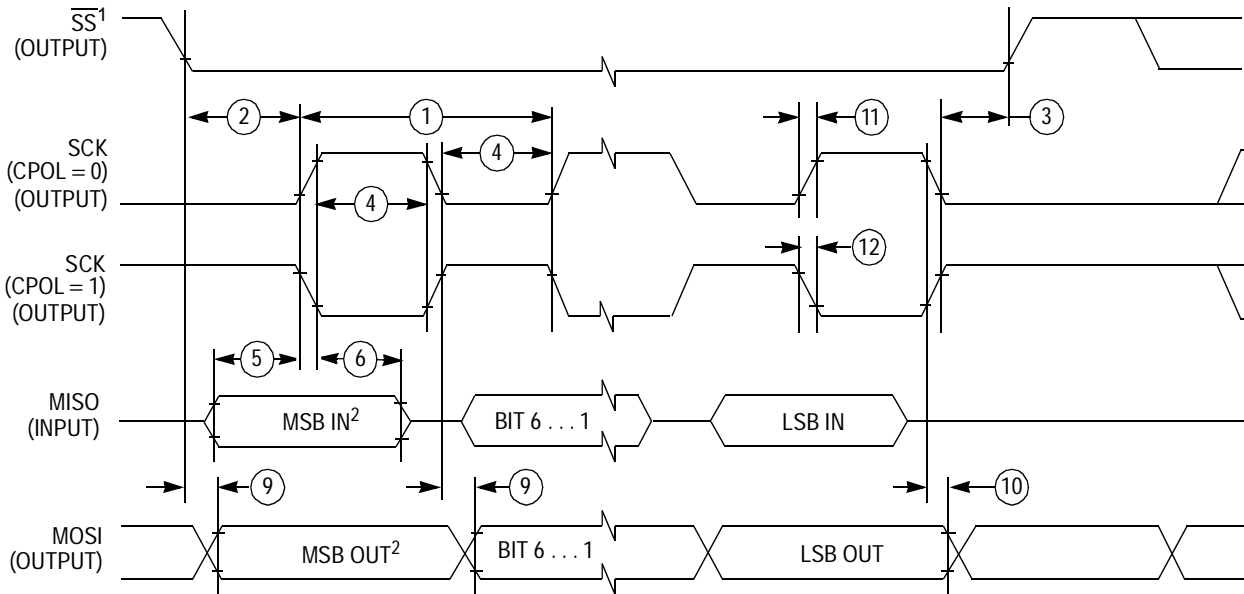
1. % deviation from target frequency

2.  $f_{REF} = 4\text{MHz}$ ,  $f_{BUS} = 25\text{MHz}$  equivalent  $f_{VCO} = 50\text{MHz}$ :  $REFDV = \#\$03$ ,  $SYNR = \#\$018$ ,  $C_s = 4.7\text{nF}$ ,  $C_p = 470\text{pF}$ ,  $R_s = 10\text{K}\Omega$ .

## A.6 SPI

### A.6.1 Master Mode

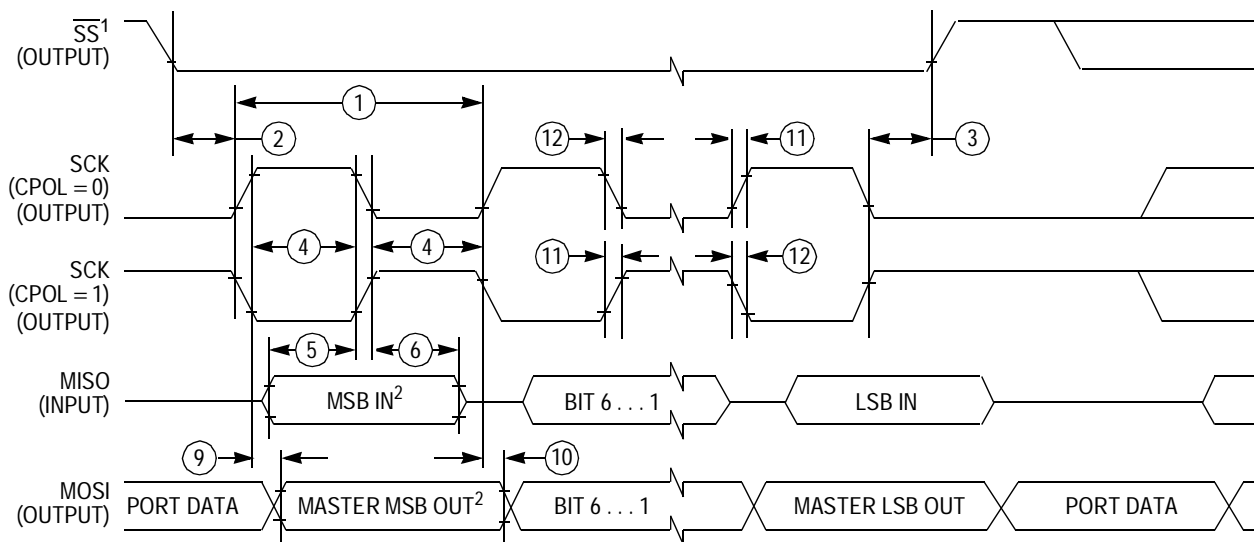
Figure A-5 and Figure A-6 illustrate the master mode timing. Timing values are shown in Table A-17.



1. If configured as output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-5 SPI Master Timing (CPHA = 0)



- 1. If configured as output
- 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6 SPI Master Timing (CPHA =1)

Table A-17 SPI Master Mode Timing Characteristics<sup>1</sup>

Conditions are shown in [Table A-4](#) unless otherwise noted, C<sub>LOAD</sub> = 200pF on all outputs

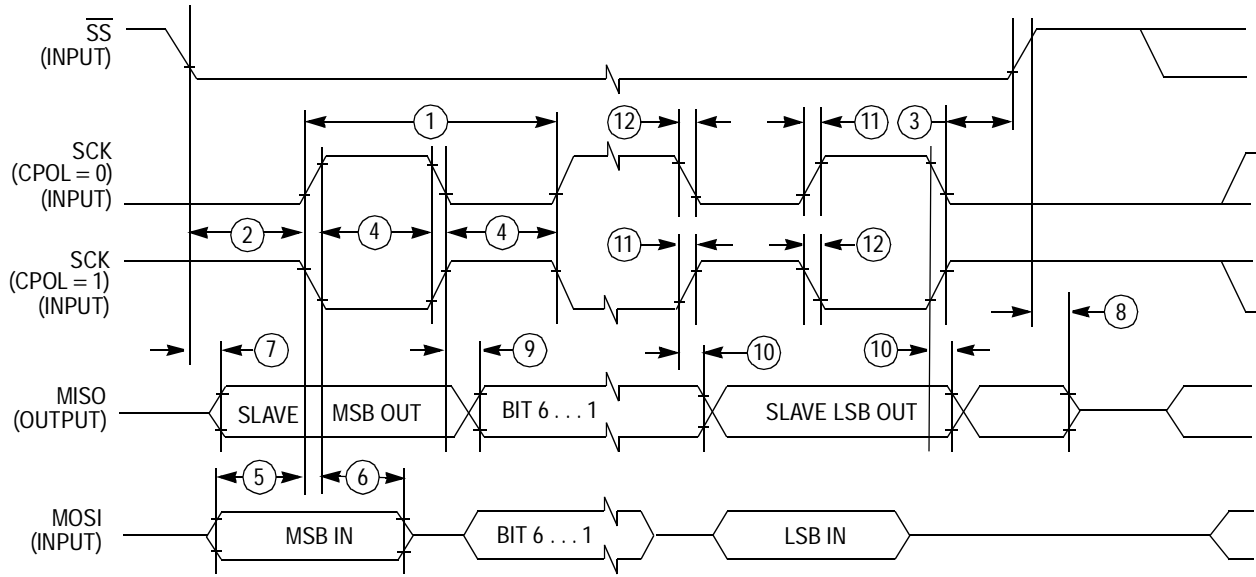
| Num | C | Rating   | Symbol            | Min                   | Typ | Max                   | Unit             |
|-----|---|--|-------------------|-----------------------|-----|-----------------------|------------------|
| 1   | P | Operating Frequency                              | f <sub>op</sub>   | DC                    |     | 1/4                   | f <sub>bus</sub> |
| 1   | P | SCK Period t <sub>sck</sub> = 1./f <sub>op</sub> | t <sub>sck</sub>  | 4                     |     | 2048                  | t <sub>bus</sub> |
| 2   | D | Enable Lead Time                                 | t <sub>lead</sub> | 1/2                   |     | —                     | t <sub>sck</sub> |
| 3   | D | Enable Lag Time                                  | t <sub>lag</sub>  | 1/2                   |     |                       | t <sub>sck</sub> |
| 4   | D | Clock (SCK) High or Low Time                     | t <sub>wsck</sub> | t <sub>bus</sub> - 30 |     | 1024 t <sub>bus</sub> | ns               |
| 5   | D | Data Setup Time (Inputs)                         | t <sub>su</sub>   | 25                    |     |                       | ns               |
| 6   | D | Data Hold Time (Inputs)                          | t <sub>hi</sub>   | 0                     |     |                       | ns               |
| 9   | D | Data Valid (after Enable Edge)                   | t <sub>v</sub>    |                       |     | 25                    | ns               |
| 10  | D | Data Hold Time (Outputs)                         | t <sub>ho</sub>   | 0                     |     |                       | ns               |
| 11  | D | Rise Time Inputs and Outputs                     | t <sub>r</sub>    |                       |     | 25                    | ns               |
| 12  | D | Fall Time Inputs and Outputs                     | t <sub>f</sub>    |                       |     | 25                    | ns               |

NOTES:

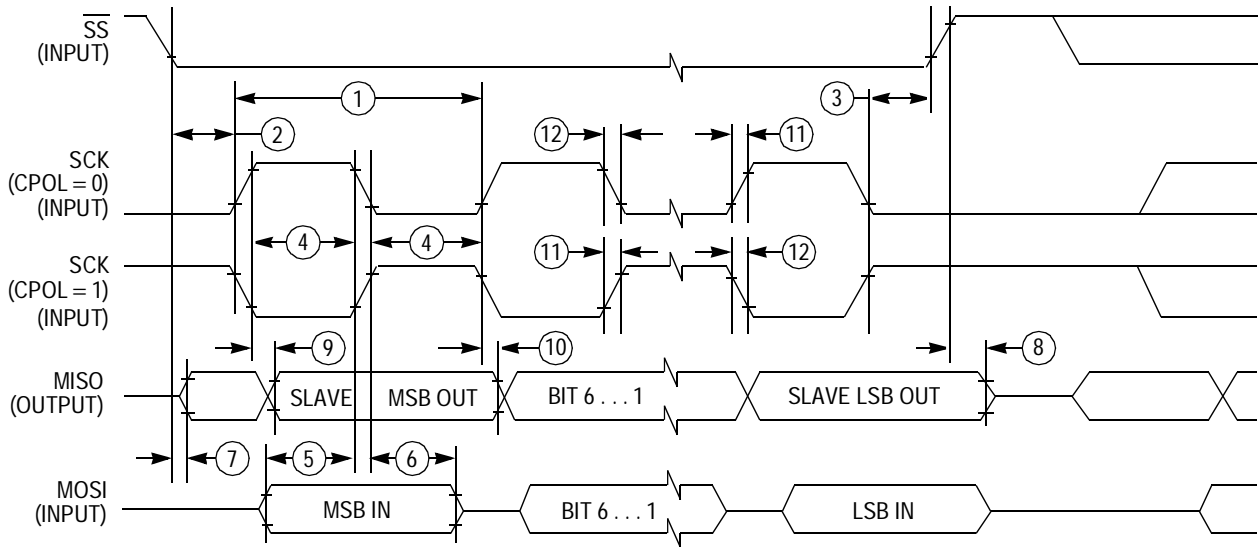
- 1. The numbers 7, 8 in the column labeled "Num" are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in [Table A-18](#).

### A.6.2 Slave Mode

Figure A-7 and Figure A-8 illustrate the slave mode timing. Timing values are shown in Table A-18.



**Figure A-7 SPI Slave Timing (CPHA = 0)**



**Figure A-8 SPI Slave Timing (CPHA = 1)**

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**Table A-18 SPI Slave Mode Timing Characteristics**

Conditions are shown in [Table A-4](#) unless otherwise noted, C<sub>LOAD</sub> = 200pF on all outputs

| Num | C | Rating   | Symbol            | Min                   | Typ | Max  | Unit             |
|-----|---|--|-------------------|-----------------------|-----|------|------------------|
| 1   | P | Operating Frequency                              | f <sub>op</sub>   | DC                    |     | 1/4  | f <sub>bus</sub> |
| 1   | P | SCK Period t <sub>sck</sub> = 1./f <sub>op</sub> | t <sub>sck</sub>  | 4                     |     | 2048 | t <sub>bus</sub> |
| 2   | D | Enable Lead Time                                 | t <sub>lead</sub> | 1                     |     |      | t <sub>cyc</sub> |
| 3   | D | Enable Lag Time                                  | t <sub>lag</sub>  | 1                     |     |      | t <sub>cyc</sub> |
| 4   | D | Clock (SCK) High or Low Time                     | t <sub>wsck</sub> | t <sub>cyc</sub> - 30 |     |      | ns               |
| 5   | D | Data Setup Time (Inputs)                         | t <sub>su</sub>   | 25                    |     |      | ns               |
| 6   | D | Data Hold Time (Inputs)                          | t <sub>hi</sub>   | 25                    |     |      | ns               |
| 7   | D | Slave Access Time                                | t <sub>a</sub>    |                       |     | 1    | t <sub>cyc</sub> |
| 8   | D | Slave MISO Disable Time                          | t <sub>dis</sub>  |                       |     | 1    | t <sub>cyc</sub> |
| 9   | D | Data Valid (after SCK Edge)                      | t <sub>v</sub>    |                       |     | 25   | ns               |
| 10  | D | Data Hold Time (Outputs)                         | t <sub>ho</sub>   | 0                     |     |      | ns               |
| 11  | D | Rise Time Inputs and Outputs                     | t <sub>r</sub>    |                       |     | 25   | ns               |
| 12  | D | Fall Time Inputs and Outputs                     | t <sub>f</sub>    |                       |     | 25   | ns               |

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## A.7 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-9** with the actual timing values shown on table **Table A-19**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

### A.7.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

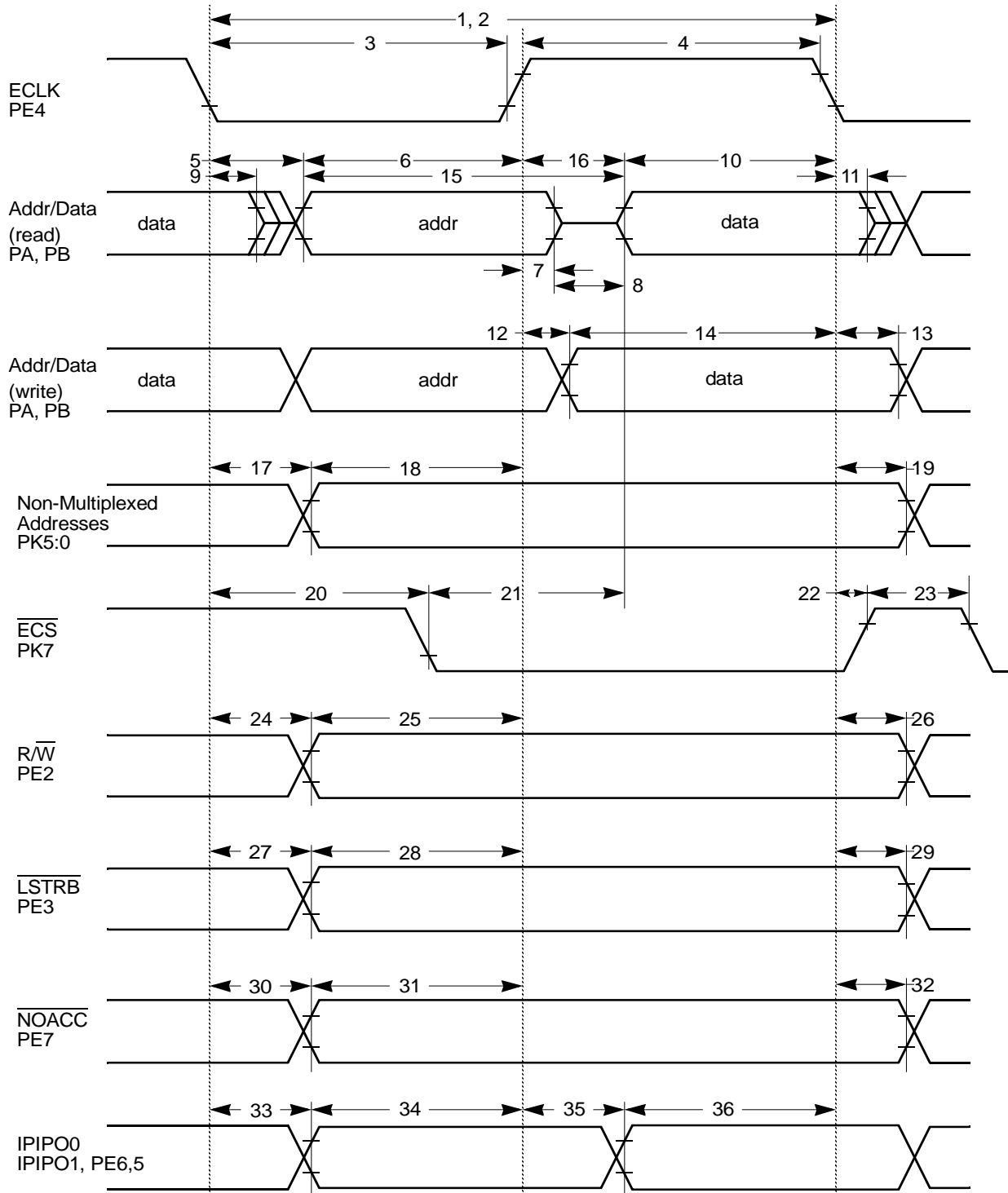


Figure A-9 General External Bus Timing

**Table A-19 Expanded Bus Timing Characteristics**

Conditions are shown in **Table A-4** unless otherwise noted,  $C_{LOAD} = 50\text{pF}$

| Num | C | Rating   | Symbol     | Min | Typ | Max  | Unit |
|-----|---|--|------------|-----|-----|------|------|
| 1   | P | Frequency of operation (E-clock)                                       | $f_o$      | 0   |     | 25.0 | MHz  |
| 2   | P | Cycle time   | $t_{cyc}$  | 40  |     |      | ns   |
| 3   | D | Pulse width, E low   | $PW_{EL}$  | 19  |     |      | ns   |
| 4   | D | Pulse width, E high <sup>1</sup>                                       | $PW_{EH}$  | 19  |     |      | ns   |
| 5   | D | Address delay time   | $t_{AD}$   |     |     | 8    | ns   |
| 6   | D | Address valid time to E rise ( $PW_{EL} - t_{AD}$ )                    | $t_{AV}$   | 11  |     |      | ns   |
| 7   | D | Muxed address hold time  | $t_{MAH}$  | 2   |     |      | ns   |
| 8   | D | Address hold to data valid   | $t_{AHDS}$ | 7   |     |      | ns   |
| 9   | D | Data hold to address   | $t_{DHA}$  | 2   |     |      | ns   |
| 10  | D | Read data setup time   | $t_{DSR}$  | 13  |     |      | ns   |
| 11  | D | Read data hold time  | $t_{DHR}$  | 0   |     |      | ns   |
| 12  | D | Write data delay time  | $t_{DDW}$  |     |     | 7    | ns   |
| 13  | D | Write data hold time   | $t_{DHW}$  | 2   |     |      | ns   |
| 14  | D | Write data setup time <sup>1</sup> ( $PW_{EH} - t_{DDW}$ )             | $t_{DSW}$  | 12  |     |      | ns   |
| 15  | D | Address access time <sup>1</sup> ( $t_{cyc} - t_{AD} - t_{DSR}$ )      | $t_{ACCA}$ | 19  |     |      | ns   |
| 16  | D | E high access time <sup>1</sup> ( $PW_{EH} - t_{DSR}$ )                | $t_{ACCE}$ | 6   |     |      | ns   |
| 17  | D | Non-multiplexed address delay time                                     | $t_{NAD}$  |     |     | 6    | ns   |
| 18  | D | Non-muxed address valid to E rise ( $PW_{EL} - t_{NAD}$ )              | $t_{NAV}$  | 15  |     |      | ns   |
| 19  | D | Non-multiplexed address hold time                                      | $t_{NAH}$  | 2   |     |      | ns   |
| 20  | D | Chip select delay time   | $t_{CSD}$  |     |     | 16   | ns   |
| 21  | D | Chip select access time <sup>1</sup> ( $t_{cyc} - t_{CSD} - t_{DSR}$ ) | $t_{ACCS}$ | 11  |     |      | ns   |
| 22  | D | Chip select hold time  | $t_{CSH}$  | 2   |     |      | ns   |
| 23  | D | Chip select negated time   | $t_{CSN}$  | 8   |     |      | ns   |
| 24  | D | Read/write delay time  | $t_{RWD}$  |     |     | 7    | ns   |
| 25  | D | Read/write valid time to E rise ( $PW_{EL} - t_{RWD}$ )                | $t_{RWV}$  | 14  |     |      | ns   |
| 26  | D | Read/write hold time   | $t_{RWH}$  | 2   |     |      | ns   |
| 27  | D | Low strobe delay time  | $t_{LSD}$  |     |     | 7    | ns   |
| 28  | D | Low strobe valid time to E rise ( $PW_{EL} - t_{LSD}$ )                | $t_{LSV}$  | 14  |     |      | ns   |
| 29  | D | Low strobe hold time   | $t_{LSH}$  | 2   |     |      | ns   |
| 30  | D | NOACC strobe delay time  | $t_{NOD}$  |     |     | 7    | ns   |
| 31  | D | NOACC valid time to E rise ( $PW_{EL} - t_{NOD}$ )                     | $t_{NOV}$  | 14  |     |      | ns   |

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**Table A-19 Expanded Bus Timing Characteristics (Continued)**

| Conditions are shown in <a href="#">Table A-4</a> unless otherwise noted, $C_{LOAD} = 50\text{pF}$ |   |  |           |     |     |     |      |
|--|---|--|-----------|-----|-----|-----|------|
| Num  | C | Rating   | Symbol    | Min | Typ | Max | Unit |
| 32   | D | NOACC hold time  | $t_{NOH}$ | 2   |     |     | ns   |
| 33   | D | IPIPO[1:0] delay time                                      | $t_{P0D}$ | 2   |     | 7   | ns   |
| 34   | D | IPIPO[1:0] valid time to E rise ( $PW_{EL} - t_{P0D}$ )    | $t_{P0V}$ | 11  |     |     | ns   |
| 35   | D | IPIPO[1:0] delay time <sup>1</sup> ( $PW_{EH} - t_{P1V}$ ) | $t_{P1D}$ | 2   |     | 25  | ns   |
| 36   | D | IPIPO[1:0] valid time to E fall                            | $t_{P1V}$ | 11  |     |     | ns   |

## NOTES:

1. Affected by clock stretch: add  $N \times t_{cyc}$  where  $N=0,1, 2$  or  $3$ , depending on the number of clock stretches.

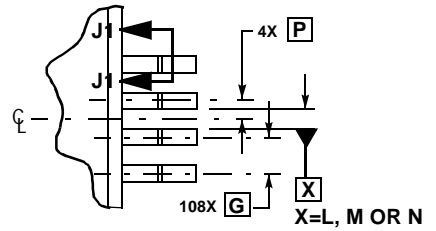
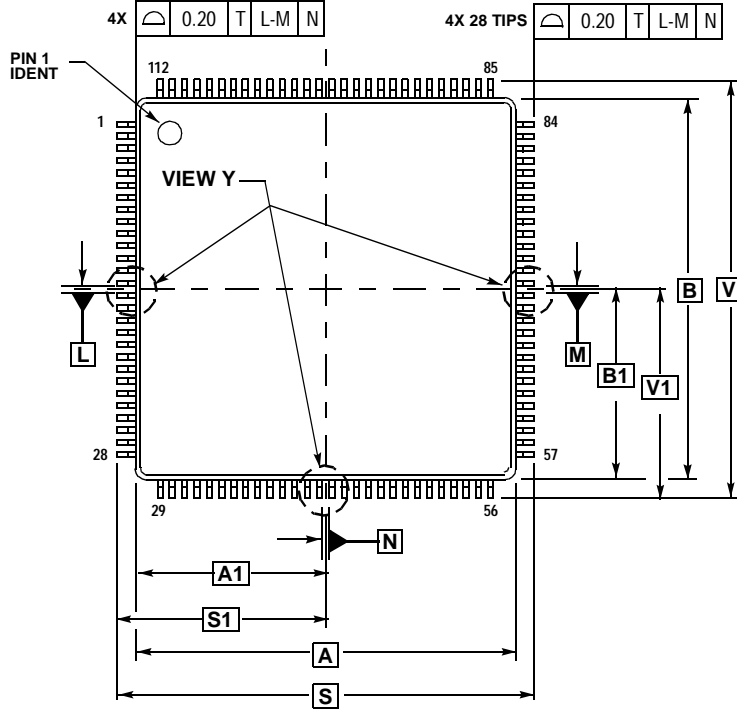


## Appendix B Package Information

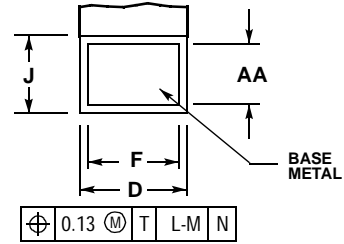
### B.1 General

This section provides the physical dimensions of the MC9S12A256 packages.

## B.2 112-Pin LQFP Package



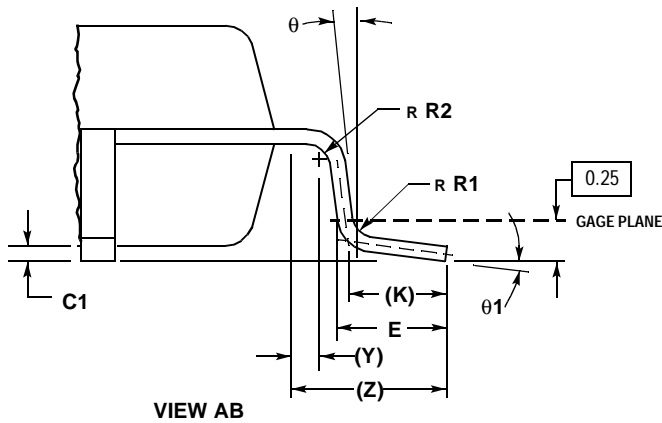
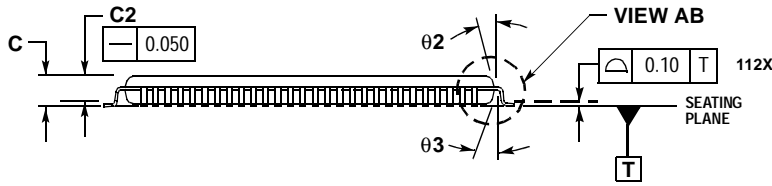
VIEW Y



SECTION J1-J1  
ROTATED 90° COUNTERCLOCKWISE

NOTES:

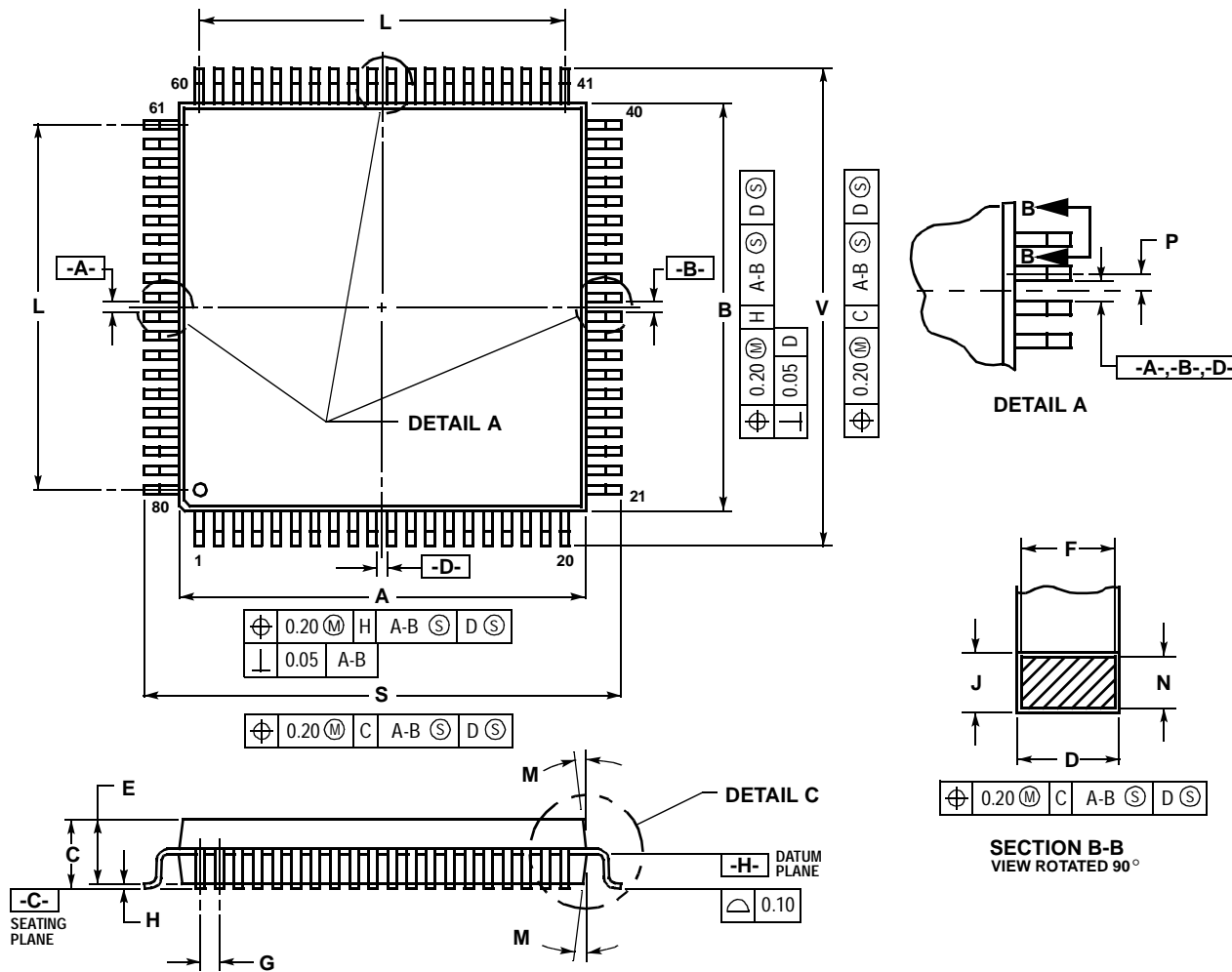
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR



| DIM     | MILLIMETERS |       |
|---------|-------------|-------|
|         | MIN         | MAX   |
| A       | 20.000      | BSC   |
| A1      | 10.000      | BSC   |
| B       | 20.000      | BSC   |
| B1      | 10.000      | BSC   |
| C       | ---         | 1.600 |
| C1      | 0.050       | 0.150 |
| C2      | 1.350       | 1.450 |
| D       | 0.270       | 0.370 |
| E       | 0.450       | 0.750 |
| F       | 0.270       | 0.330 |
| G       | 0.650       | BSC   |
| J       | 0.090       | 0.170 |
| K       | 0.500       | REF   |
| P       | 0.325       | BSC   |
| R1      | 0.100       | 0.200 |
| R2      | 0.100       | 0.200 |
| S       | 22.000      | BSC   |
| S1      | 11.000      | BSC   |
| V       | 22.000      | BSC   |
| V1      | 11.000      | BSC   |
| Y       | 0.250       | REF   |
| Z       | 1.000       | REF   |
| AA      | 0.090       | 0.160 |
| theta   | 0°          | 8°    |
| theta 1 | 3°          | 7°    |
| theta 2 | 11°         | 13°   |
| theta 3 | 11°         | 13°   |

Figure B-1 112-Pin LQFP Mechanical Dimensions (Case no. 987)

### B.3 80-Pin QFP Package



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
  5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
  6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 13.90       | 14.10 |
| B   | 13.90       | 14.10 |
| C   | 2.15        | 2.45  |
| D   | 0.22        | 0.38  |
| E   | 2.00        | 2.40  |
| F   | 0.22        | 0.33  |
| G   | 0.65 BSC    |       |
| H   | ---         | 0.25  |
| J   | 0.13        | 0.23  |
| K   | 0.65        | 0.95  |
| L   | 12.35 REF   |       |
| M   | 5°          | 10°   |
| N   | 0.13        | 0.17  |
| P   | 0.325 BSC   |       |
| Q   | 0°          | 7°    |
| R   | 0.13        | 0.30  |
| S   | 16.95       | 17.45 |
| T   | 0.13        | ---   |
| U   | 0°          |       |
| V   | 16.95       | 17.45 |
| W   | 0.35        | 0.45  |
| X   | 1.6 REF     |       |

Figure B-2 80-Pin QFP Mechanical Dimensions (Case no. 841B)

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## User Guide End Sheet

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