19-0850; Rev 0; 7/07

EVALUATION KIT AVAILABLE

2-Wire Interfaced Low-EMI Key Switch Controller/GPO

MAX7359

General Description

The MAX7359 I²C interfaced peripheral provides microprocessors with management of up to 64 key switches. Key codes are generated for each press and release of a key for easier implementation of multiple key entries. Key inputs are monitored statically, not dynamically, to ensure low-EMI operation. The switches can be metallic or resistive (carbon) with up to 5kΩ of resistance.

The MAX7359 features autosleep and autowake to further minimize the power consumption of the device. The autosleep feature puts the device in a low-power state (1µA typ) after a sleep timeout period. The autowake feature configures the MAX7359 to return to normal operating mode from sleep upon a key press.

The key controller debounces and maintains a FIFO of key-press and release events (including autorepeat, if enabled). An interrupt ($\overline{INT}$) output can be configured to alert key presses either as they occur, or at maximum rate.

Any of the column drivers (COL2/PORT2–COL7/PORT7) or the $\overline{INT}$, if not used, can function as a general-purpose output (GPO).

The MAX7359 is offered in a small 24-pin TQFN (3.5mm x 3.5mm) package for cell phones, pocket PCs, and other portable consumer electronic applications. The MAX7359 operates over the -40°C to +85°C temperature range.

Applications

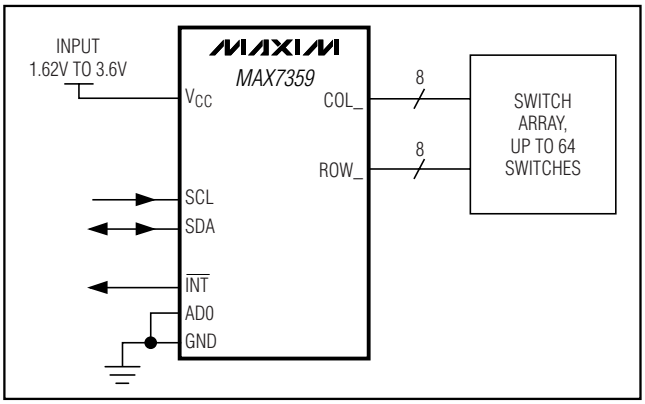
Cell Phones

PDAs

Handheld Games

Portable Consumer Electronics

Typical Application Circuit



Pin Configuration appears at end of data sheet.

Features

- **Optional Key Release Detection on All Keys**
- **Monitor Up to 64 Keys**
- **1.62V to 3.6V Operation**
- **Autosleep and Autowake to Minimize Current Consumption**
- **Under 1µA Sleep Current**
- **FIFO Queues Up to 16 Debounced Key Events**
- **Key Debounce Time User Configurable from 9ms to 40ms**
- **Low-EMI Design Uses Static Matrix Monitoring**
- **Hardware Interrupt at the FIFO Level or at the End of Definable Time Period**
- **Up to Seven Open-Drain Logic Outputs Available Capable of Driving LEDs**
- **400kbps, 5.5V-Tolerant, 2-Wire Serial Interface**
- **Selectable 2-Wire, Serial-Bus Timeout**
- **Four I²C Address Choices**
- **Small, 24-Pin TQFN Package (3.5mm x 3.5mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX7359ETG+	-40°C to +85°C	24 TQFN-EP* (3.5mm x 3.5mm)	T243A3-1

+Denotes a lead-free package.

**EP = Exposed paddle.*

2-Wire Interfaced Low-EMI Key Switch Controller/GPO

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} .....-0.3V to +4V
COL2/PORT2–COL7/PORT7 .....-0.3V to +4V
SDA, SCL, AD0, $\overline{INT}$.....-0.3V to +6V
All Other Pins.....-0.3V to (V_{CC} + 0.3V)
DC Current on COL2/PORT2–COL7/PORT7 .....25mA
GND Current 80mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 15.4mW/°C above +70°C).....1229mW
Operating Temperature Range (T_{MIN} to T_{MAX}) .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.62V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 2.5V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}		1.62		3.60	V
Operating Supply Current	I_{CC}	All key switches open, oscillator running, COL2–COL7 configured as key switches		25	60	µA
		N keys pressed		(25 + 20 x N)		
Sleep-Mode Supply Current	I_{SL}			0.6	5	µA
POR			1.0		1.6	V
POR Hysteresis	PORHYST	V_{CC} rising		42		mV
Key-Switch Source Current	I_{KEY}			20	35	µA
Key-Switch Source Voltage	V_{KEY}	Operating mode		0.42	0.55	V
Key-Switch Resistance	R_{KEY}	(Note 3)			5	kΩ
Startup Time from Shutdown	t_{START}			2000	2400	µs
Output Low Voltage COL2/PORT2 to COL7/PORT7	V_{OLPORT}	I_{SINK} = 10mA			0.2	V
$\overline{INT}$ Output	V_{OLINT}	I_{SINK} = 10mA			0.5	V
Oscillator Frequency	F_{OSC}			64		kHz
SERIAL-INTERFACE SPECIFICATIONS						
Serial Bus Timeout	t_{OUT}	With bus timeout enabled	10		40	ms
Input High Voltage SDA, SCL, AD0	V_{IH}		0.7 x V_{CC}			V
Input Low Voltage SDA, SCL, AD0	V_{IL}				0.3 x V_{CC}	V
Output Low Voltage SDA	V_{OLPORT}	I_{SINK} = 10mA			0.4	V
Input Leakage Current		V_{CC} = 0 to 6V	-1		+1	µA

I²C TIMING CHARACTERISTICS

(V_{CC} = 1.62V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 2.5V, T_A = +25°C.) (Notes 1, 2) (Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance (SCL, SDA, AD0)	C_{IN}	(Notes 3, 4)			10	pF
SCL Serial-Clock Frequency	f_{SCL}	Bus timeout disabled	0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 5)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F.TX}$	(Notes 3, 6)		$20 + 0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 3, 7)			50	ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF

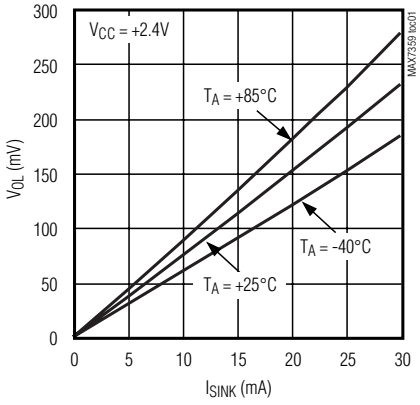
Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: All digital inputs at V_{CC} or GND.
Note 3: Guaranteed by design.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.
Note 5: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 6: $I_{SINK} \leq 6mA$. C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.
Note 7: Input filters on the SDA, SCL, and AD0 inputs suppress noise spikes less than 50ns.

2-Wire Interfaced Low-EMI Key Switch Controller/GPO

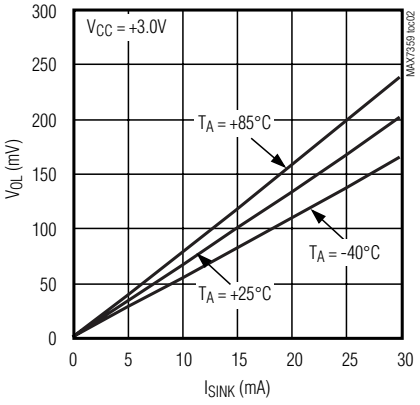
Typical Operating Characteristics

(V_{CC} = 2.5V, T_A = +25°C, unless otherwise noted.)

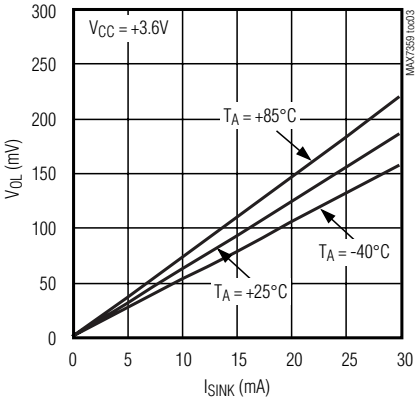
GPO PORT OUTPUT LOW VOLTAGE vs. SINK CURRENT



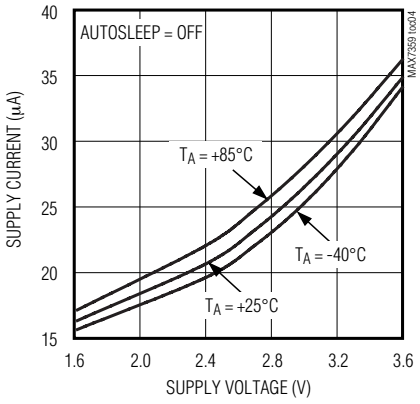
GPO PORT OUTPUT LOW VOLTAGE vs. SINK CURRENT



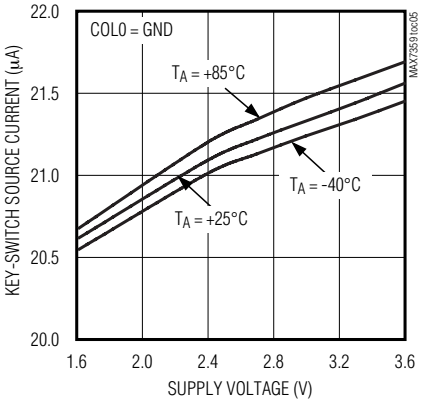
GPO PORT OUTPUT LOW VOLTAGE vs. SINK CURRENT



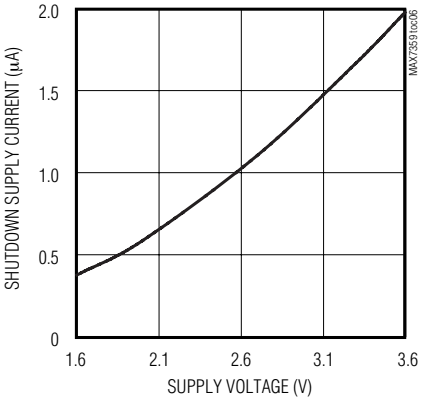
SUPPLY CURRENT vs. SUPPLY VOLTAGE



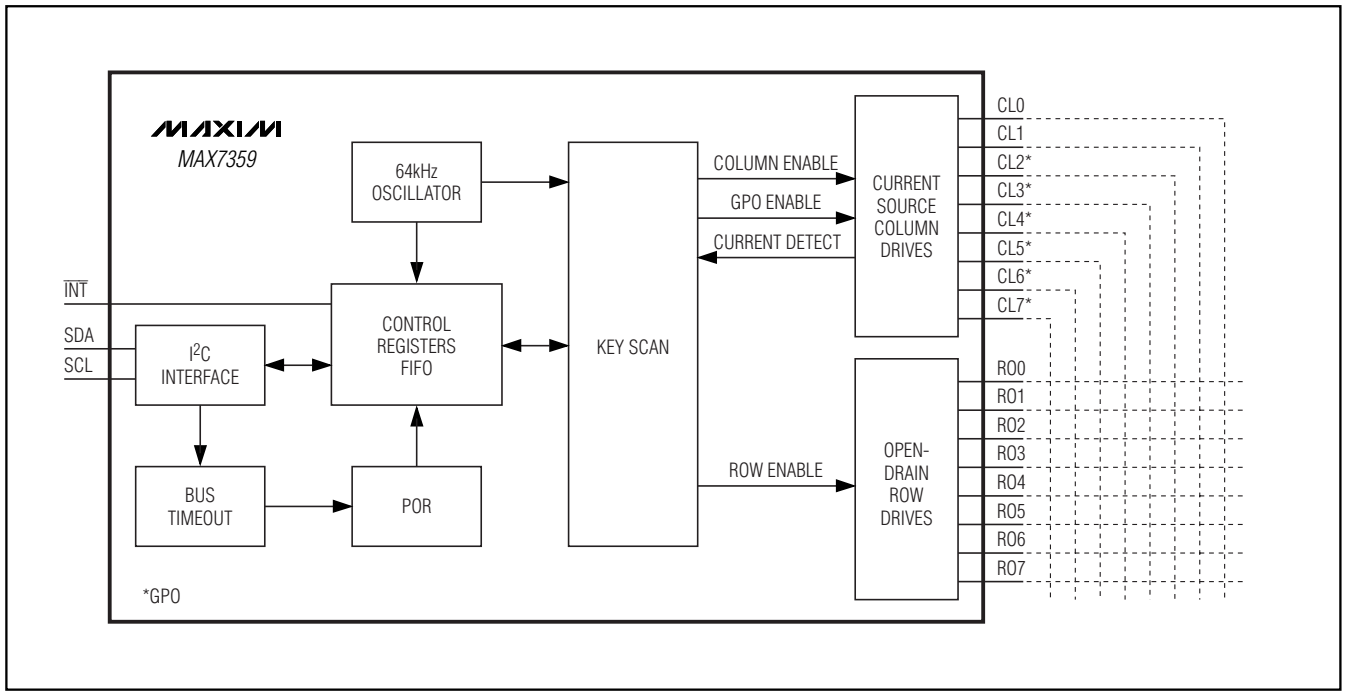
KEY-SWITCH SOURCE CURRENT vs. SUPPLY VOLTAGE



SLEEP MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



Functional Block Diagram



2-Wire Interfaced Low-EMI Key Switch Controller/GPO

Pin Description

PIN	NAME	FUNCTION
1	ROW2	Row Input from Key Matrix. Leave ROW2 unconnected or connect to GND if unused.
2	ROW3	Row Input from Key Matrix. Leave ROW3 unconnected or connect to GND if unused.
3	COL3/PORT3	Column Output to Key Matrix or GPO. Leave COL3/PORT3 unconnected if unused.
4	COL4/PORT4	Column Output to Key Matrix or GPO. Leave COL4/PORT4 unconnected if unused.
5	ROW4	Row Input from Key Matrix. Leave ROW4 unconnected or connect to GND if unused.
6	ROW5	Row Input from Key Matrix. Leave ROW5 unconnected or connect to GND if unused.
7	ROW6	Row Input from Key Matrix. Leave ROW6 unconnected or connect to GND if unused.
8	ROW7	Row Input from Key Matrix. Leave ROW7 unconnected or connect to GND if unused.
9	COL6/PORT6	Column Output to Key Matrix or GPO. Leave COL6/PORT6 unconnected if unused.
10	COL5/PORT5	Column Output to Key Matrix or GPO. Leave COL5/PORT5 unconnected if unused.
11	COL2/PORT2	Column Output to Key Matrix or GPO. Leave COL2/PORT2 unconnected if unused.
12	COL1	Column Output to Key Matrix. Leave COL1 unconnected if unused.
13	COL0	Column Output to Key Matrix. Leave COL0 unconnected if unused.
14	I.C.	Internally Connected. Connect to GND for normal operation.
15	GND	Ground
16	AD0	Adddress Input. ADO selects up to four device slave addresses (Table 10).
17	SDA	I²C-Compatible, Serial-Data I/O
18	SCL	I²C-Compatible, Serial-Clock Input
19	$\overline{INT}$	Active-Low Interrupt Output. $\overline{INT}$ is open drain.
20	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with a 0.047µF or higher ceramic capacitor.
21	N.C.	No Connection. Not internally connected.
22	COL7/PORT7	Column Output to Key Matrix or GPO. Leave COL7/PORT7 unconnected is unused.
23	ROW0	Row Input from Key Matrix. Leave ROW0 unconnected or connect to GND if unused.
24	ROW1	Row Input from Key Matrix. Leave ROW1 unconnected or connect to GND if unused.
—	EP	Exposed Paddle. EP internally is connected to GND. Connect EP to a ground plane to increase thermal performance.

Detailed Description

The MAX7359 is a microprocessor peripheral low-noise key-switch controller that monitors up to 64 key switches with optional autorepeat, and key events are presented in a 16-byte FIFO. Key-switch functionality can be traded to provide up to six open-drain logic outputs.

The MAX7359 features an automatic sleep mode and automatic wakeup that further reduce supply current consumption. The MAX7359 can be configured to enter sleep mode after a programmable time following a key event. The FIFO content is maintained during sleep mode and can be read in sleep mode. The MAX7359 does not enter autosleep when a key is held down. The autowake feature takes the MAX7359 out of sleep mode following a key-press event. Autosleep and autowake can be disabled.

Interrupt requests can be configured to be issued on a programmable number of FIFO entries, or can be set to a period of time to prevent overloading the microprocessor with too many interrupts. The key-switch status can be checked at any time by reading the key-switch FIFO. A 1-byte read access returns both the next key-event in the FIFO (if there is one) and the FIFO status, so it is easy to operate the MAX7359 by polling. If the $\overline{INT}$ pin is not required, it can be configured as an open-drain general-purpose output (GPO) capable of driving an LED.

If the application requires fewer keys to be scanned, up to six of the key-switch outputs can be configured as open-drain GPOs capable of driving LEDs. For each key-switch output used as a GPO, the number of key switches that can be scanned is reduced by eight.

Key-Scan Controller

Key inputs are scanned statically, not dynamically, to ensure low-EMI operation. As inputs only toggle in response to switch changes, the key matrix can be routed closer to sensitive circuit nodes.

The key controller debounces and maintains a FIFO of key-press and release events (including autorepeated key presses, if autorepeat is enabled). Table 1 shows keys order.

Initial Power-Up

On power-up, all control registers are set to power-up values and the MAX7359 is in sleep mode (Table 2).

Registers Description

Keys FIFO Register (0x00)

The keys FIFO register contains the information pertaining to the status of the keys FIFO, as well as the key events that have been debounced (Table 3). Bits D0 to D5 denote which of the 64 keys have been debounced and the keys are numbered as in Table 1.

D7 indicates if there is more data in the FIFO except when D5:D0 indicate key 63 or key 62. When D5:D0 indicate key 63 or key 62, the host should read one more time to determine whether there is more data in FIFO. It is better to use key 62 and key 63 for rarely used keys. D6 indicates if it is a key-press or release event except when D5:D0 indicate key 63 or key 62.

Reading the key-scan FIFO clears the interrupt $\overline{INT}$ depending on the setting of bit D5 in the configuration register (0x01).

Configuration Register (0x01)

The configuration register controls the I^2C bus timeout feature, enables key release detection, enables autowake, and determines how $\overline{INT}$ should be deasserted. By writing to bit D7, you can put the MAX7359 into sleep mode or operating mode, however, autosleep and autowake, when enabled, also change the status of this bit (Table 4).

Table 1. Key-Switch Mapping

PIN	COL0	COL1	COL2/PORT2	COL3/PORT3	COL4/PORT4	COL5/PORT5	COL6/PORT6	COL7/PORT7
ROW0	KEY 0	KEY 8	KEY 16	KEY 24	KEY 32	KEY 40	KEY 48	KEY 56
ROW1	KEY 1	KEY 9	KEY 17	KEY 25	KEY 33	KEY 41	KEY 49	KEY 57
ROW2	KEY 2	KEY 10	KEY 18	KEY 26	KEY 34	KEY 42	KEY 50	KEY 58
ROW3	KEY 3	KEY 11	KEY 19	KEY 27	KEY 35	KEY 43	KEY 51	KEY 59
ROW4	KEY 4	KEY 12	KEY 20	KEY 28	KEY 36	KEY 44	KEY 52	KEY 60
ROW5	KEY 5	KEY 13	KEY 21	KEY 29	KEY 37	KEY 45	KEY 53	KEY 61
ROW6	KEY 6	KEY 14	KEY 22	KEY 30	KEY 38	KEY 46	KEY 54	KEY 62
ROW7	KEY 7	KEY 15	KEY 23	KEY 31	KEY 39	KEY 47	KEY 55	KEY 63

Table 2. Register Address Map and Power-Up Condition

ADDRESS CODE (hex)	READ/WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x00	Read only	0x3F	Keys FIFO	Read FIFO key scan data out
0x01	R/$\overline{W}$	0x0A	Configuration	Power down, key release enable, autowakeup, and I^2C timeout enable
0x02	R/$\overline{W}$	0xFF	Debounce	Key debounce time setting and GPO enable
0x03	R/$\overline{W}$	0x00	Interrupt	$\overline{INT}$ frequency setting
0x04	R/$\overline{W}$	0xFE	Ports	Ports 2–7 and $\overline{INT}$ GPO control
0x05	R/$\overline{W}$	0x00	Key repeat	Delay and frequency for key repeat
0x06	R/$\overline{W}$	0x07	Sleep	Idle time to autosleep

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Table 3. Keys FIFO Register Format (0x00)

SPECIAL FUNCTION	KEYS FIFO REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
The key number indicated by D5:D0 is a key event. D7 is always for a key press of key 62 and key 63. When D7 is 0, the key read is the last data in the FIFO. When D7 is 1, there is more data in the FIFO. When D6 is 1, key data read from FIFO is a key release. When D6 is 0, key data read from FIFO is a key press.	FIFO empty flag	Key release flag	X	X	X	X	X	X
FIFO is empty.	0	0	1	1	1	1	1	1
FIFO is overflow. Continue to read data in FIFO.	0	1	1	1	1	1	1	1
Key 63 is pressed. Read one more time to determine whether there is more data in FIFO.	1	0	1	1	1	1	1	1
Key 63 is released. Read one more time to determine whether there is more data in FIFO.	1	1	1	1	1	1	1	1
Key repeat. Indicates the last data in FIFO.	0	0	1	1	1	1	1	0
Key repeat. Indicates more data in FIFO.	0	1	1	1	1	1	1	0
Key 62 is pressed. Read one more time to determine whether there is more data in FIFO.	1	0	1	1	1	1	1	0
Key 62 is released. Read one more time to determine whether there is more data in FIFO.	1	1	1	1	1	1	1	0

Table 4. Configuration Register Format (0x01)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION		DEFAULT VALUE
D7	Sleep	0	Sleep mode	I²C write, autosleep and autowakeup all can change this bit. This bit can be read back by I²C any time for current status.	0
		1	Operating mode		
D6	Reserved	0	This bit must always be 0. Improper operation may result by writing a 1 to this location.		0
D5	INTERRUPT	0	Clear when FIFO empty		0
		1	Clear after host read. In this mode, I²C should read FIFO until interrupt condition removed, or further INT may be lost.		
D4	Reserved	0	This bit must always be 0. Improper operation may result by writing a 1 to this location.		0
D3	Key release enable	0	Disable		1
		1	Enable		
D2	Reserved	0	This bit must always be 0. Improper operation results by writing a 1 to this location.		0
D1	Wakeup	0	Disable		1
		1	Key press wakeup enable		
D0	Timeout enable	0	I²C timeout enabled		0
		1	I²C timeout disabled		

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Debounce Register (0x02)

The debounce register sets the time for each debounce cycle, as well as setting whether the GPO ports are enabled or disabled. Bits D0 through D4 set the debounce time in increments of 1ms starting at 9ms and ending at 40ms (Table 5). Bits D5 through D7 set which of the GPO ports is enabled. Note the GPO ports can be enabled only in the combinations shown in Table 5, from all disabled to all enabled.

Table 5. Debounce Register Format (0x02)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	PORTS ENABLE			DEBOUNCE TIME				
Debounce time is 9ms	X	X	X	0	0	0	0	0
Debounce time is 10ms	X	X	X	0	0	0	0	1
Debounce time is 11ms	X	X	X	0	0	0	1	0
Debounce time is 12ms	X	X	X	0	0	0	1	1
. . .								
Debounce time is 37ms	X	X	X	1	1	1	0	0
Debounce time is 38ms	X	X	X	1	1	1	0	1
Debounce time is 39ms	X	X	X	1	1	1	1	0
Debounce time is 40ms	X	X	X	1	1	1	1	1
GPO ports disabled (full key-scan functionality)	0	0	0	X	X	X	X	X
GPO port 7 enabled	0	0	1	X	X	X	X	X
GPO ports 7 and 6 enabled	0	1	0	X	X	X	X	X
GPO ports 7, 6, and 5 enabled	0	1	1	X	X	X	X	X
GPO ports 7, 6, 5, and 4 enabled	1	0	0	X	X	X	X	X
GPO ports 7, 6, 5, 4, and 3 enabled	1	0	1	X	X	X	X	X
GPO ports 7, 6, 5, 4, 3, and 2 enabled	1	1	X	X	X	X	X	X
Power-up default setting	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Interrupt Register (0x03)

The interrupt register contains information related to the settings of the interrupt request function, as well as the status of the $\overline{INT}$ output, which can also be configured as a GPO. If bits D0 through D7 are set to 0x00, the $\overline{INT}$ output is configured as a GPO that is controlled by bit D1 in the port register. There are two types of interrupts, the FIFO based-interrupt and time-based interrupt. The time-based interrupt can be configured to assert $\overline{INT}$ after a number of debounce cycles. By setting bits D0 through D4 to an appropriate value, the interrupt can be asserted at the end of the selected number of debounce cycles following a key event (Table 6). This number ranges from 1 to 31 debounce cycles. The FIFO based interrupt can be configured to assert $\overline{INT}$ when there are between 4 through 16 key events stored in the FIFO. Bits D7 through D5 set the FIFO based interrupt. Both interrupts can be configured simultaneously and $\overline{INT}$ asserts depending on which condition is met first. $\overline{INT}$ deasserts depending on the status of bit D5 in the configuration register.

Table 6. Interrupt Register Format (0x03)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	FIFO-BASED $\overline{INT}$			TIME-BASED $\overline{INT}$				
$\overline{INT}$ used as GPO	0	0	0	0	0	0	0	0
FIFO based $\overline{INT}$ disabled	0	0	0	Not all zero				
$\overline{INT}$ asserts every debounce cycles	0	0	0	0	0	0	0	1
$\overline{INT}$ asserts every 2 debounce cycles	0	0	0	0	0	0	1	0
	. . .							
$\overline{INT}$ asserts every 29 debounce	0	0	0	1	1	1	0	1
$\overline{INT}$ asserts every 30 debounce	0	0	0	1	1	1	1	0
$\overline{INT}$ asserts every 31 debounce	0	0	0	1	1	1	1	1
Time based $\overline{INT}$ disabled	Not all zero			0	0	0	0	0
$\overline{INT}$ asserts when FIFO has 2 key events	0	0	1	0	0	0	0	0
$\overline{INT}$ asserts when FIFO has 4 key events	0	1	0	0	0	0	0	0
$\overline{INT}$ asserts when FIFO has 6 key events	0	1	1	0	0	0	0	0
	. . .							
$\overline{INT}$ asserts when FIFO has 16 key events	1	1	1	0	0	0	0	0
Both time base and FIFO based interrupts active	Not all zero			Not all zero				
Power-up default setting	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Ports Register (0x04)

The ports register sets the values of ports 2 through 7 and the $\overline{INT}$ port when configured as open-drain GPOs. The settings in this register are ignored for ports not configured as GPOs, and a read from this register returns the values stored in the register (Table 7).

Autorepeat Register (0x05)

The MAX7359 autorepeat feature notifies the host that at least one key has been pressed for a continuous period of time. The autorepeat register enables or disables this feature, sets the time delay after the last key event before the key repeat code (0x7E) is entered into the FIFO, and sets the frequency at which the key repeat code is entered into the FIFO thereafter. Bit D7 specifies whether the autorepeat function is enabled with 0 denoting autorepeat disabled and 1 denoting autorepeat enabled. Bits D0 through D3 specify the autorepeat delay in terms of debounce cycles ranging from eight debounce cycles to 128 debounce cycles (Table 8). Bits D4 through D6 specify the autorepeat rate or frequency ranging from 4 to 32 debounce cycles.

When autorepeat is enabled, holding the key pressed results in a key repeat event that is denoted by 0x7E. The key being pressed does not show up again in the FIFO.

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Table 7. Ports Register Format (0x04)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT 7 Control	0	Clear port 7 low	1
		1	Set port 7 high (high impedance)	
D6	PORT 6 Control	0	Clear port 6 low	1
		1	Set port 6 high (high impedance)	
D5	PORT 5 Control	0	Clear port 5 low	1
		1	Set port 5 high (high impedance)	
D4	PORT 4 Control	0	Clear port 4 low	1
		1	Set port 4 high (high impedance)	
D3	PORT 3 Control	0	Clear port 3 low	1
		1	Set port 3 high (high impedance)	
D2	PORT 2 Control	0	Clear port 2 low	1
		1	Set port 2 high (high impedance)	
D1	$\overline{INT}$ Port Control	0	Clear port $\overline{INT}$ low	1
		1	Set port $\overline{INT}$ high (high impedance)	
D0	Reserved	0	—	0

Table 8. Autorepeat Register Format (0x05)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	ENABLE	AUTOREPEAT RATE			AUTOREPEAT DELAY			
Autorepeat is disabled	0	X	X	X	X	X	X	X
Autorepeat is enabled	1	AUTOREPEAT RATE			AUTOREPEAT DELAY			
Key-switch autorepeat delay is 8 debounce cycles	1	X	X	X	0	0	0	0
Key-switch autorepeat delay is 16 debounce cycles	1	X	X	X	0	0	0	1
Key-switch autorepeat delay is 24 debounce cycles	1	X	X	X	0	0	1	0
. . .								
Key-switch autorepeat delay is 112 debounce cycles	1	X	X	X	1	1	0	1
Key-switch autorepeat delay is 120 debounce cycles	1	X	X	X	1	1	1	0
Key-switch autorepeat delay is 128 debounce cycles	1	X	X	X	1	1	1	1
Key-switch autorepeat frequency is 4 debounce cycles	1	0	0	0	X	X	X	X
Key-switch autorepeat frequency is 8 debounce cycles	1	0	0	1	X	X	X	X
Key-switch autorepeat frequency is 12 debounce cycles	1	0	1	0	X	X	X	X
. . .								
Key switch autorepeat frequency is 32 debounce cycles	1	1	1	1	X	X	X	X
Power-up default setting	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Only one autorepeat code is entered into the FIFO, regardless of the number of keys pressed. The autorepeat code continues to be entered in the FIFO at the frequency set by the bits D4–D1 until another key event is recorded. Following the key-release event, if any keys are still pressed, the MAX7359 restarts the autorepeat sequence.

Autosleep Register (0x06)

Autosleep puts the MAX7359 in sleep mode to draw minimal current. When enabled, the MAX7359 enters sleep mode if no keys are pressed for the autosleep time (Table 9).

Sleep Mode

In sleep mode, the MAX7359 draws minimal current. Switch matrix current sources are turned off and pulled up to V_{CC}. Writing a 0 to D7 in the configuration register (0x01) puts the device in sleep mode. Writing a 1 to D7 or a key press, when the part is programmed to autowake, can take the MAX7359 out of sleep mode. Bit D7 in the configuration register gives the sleep mode status and can be read anytime. The FIFO data is maintained while in sleep mode.

Autowake

Key presses initiate autowake and the MAX7359 goes into operating mode. Key presses that autowake the MAX7359 are not lost. When a key is pressed while the MAX7359 is in sleep mode, all analog circuitry, including switch matrix current sources, turn on in 2ms. The initial key needs to be pressed for 2ms plus the debounce time to be stored in the FIFO. Autowakeup can be disabled by writing a 0 to D1 in the configuration register (0x01).

Serial Interface

Figure 1 shows the 2-wire serial interface timing details.

Serial Addressing

The MAX7359 operates as a slave that sends and receives data through an I^2C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX7359 and generates the SCL clock that synchronizes the data transfer.

The MAX7359's SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The MAX7359's SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 2) sent by a master, followed by the MAX7359 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, 1 or more data bytes, and finally a STOP condition.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 3). The data on SDA must remain stable while SCL is high.

Table 9. Autosleep Register Format (0x06)

REGISTER	REGISTER DATA							
AUTOSLEEP REGISTER	RESERVED					AUTOSHUTDOWN TIME		
	D7	D6	D5	D4	D3	D2	D1	D0
No Autosleep	0	0	0	0	0	0	0	0
Autosleep for (ms)								
8192	0	0	0	0	0	0	0	1
4096	0	0	0	0	0	0	1	0
2048	0	0	0	0	0	0	1	1
1024	0	0	0	0	0	1	0	0
512	0	0	0	0	0	1	0	1
256	0	0	0	0	0	1	1	0
256	0	0	0	0	0	1	1	1
Power-up default settings	0	0	0	0	0	1	1	1

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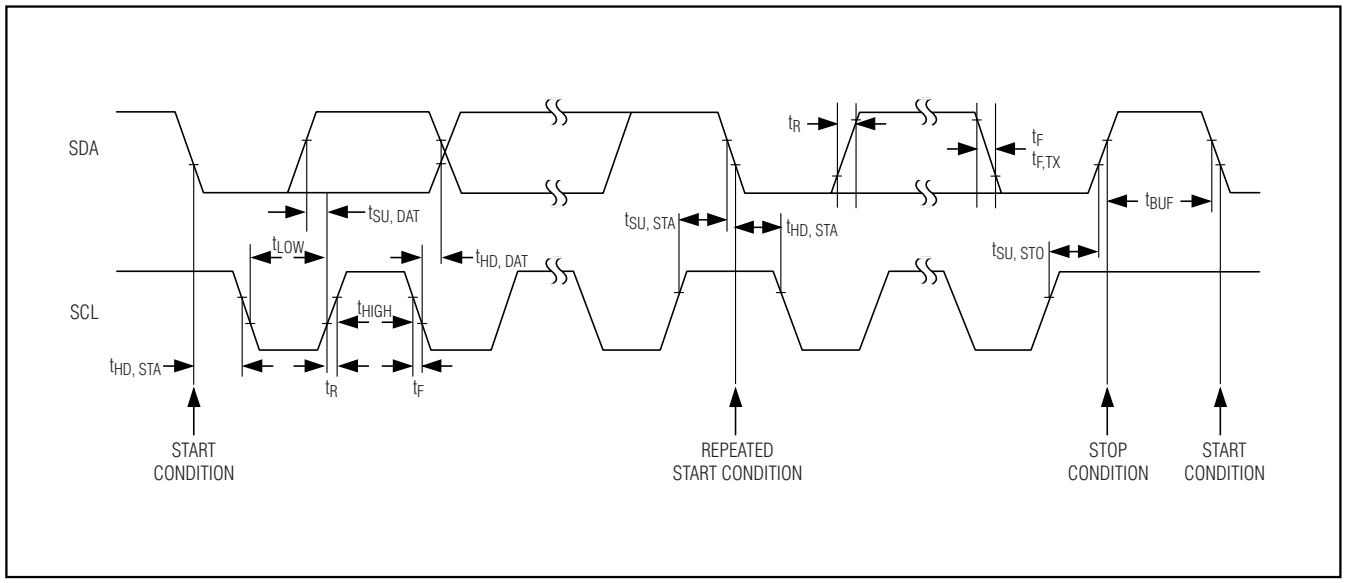

Figure 1. 2-Wire Serial Interface Timing Details

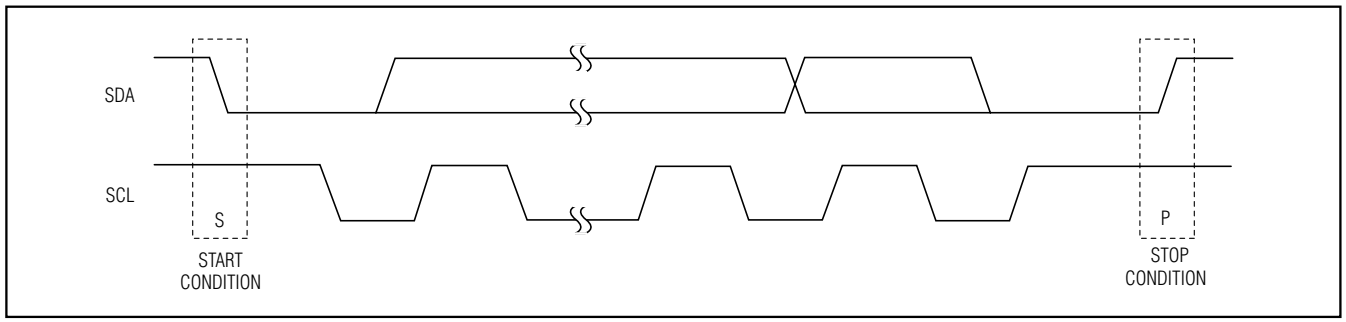

Figure 2. Start and Stop Conditions

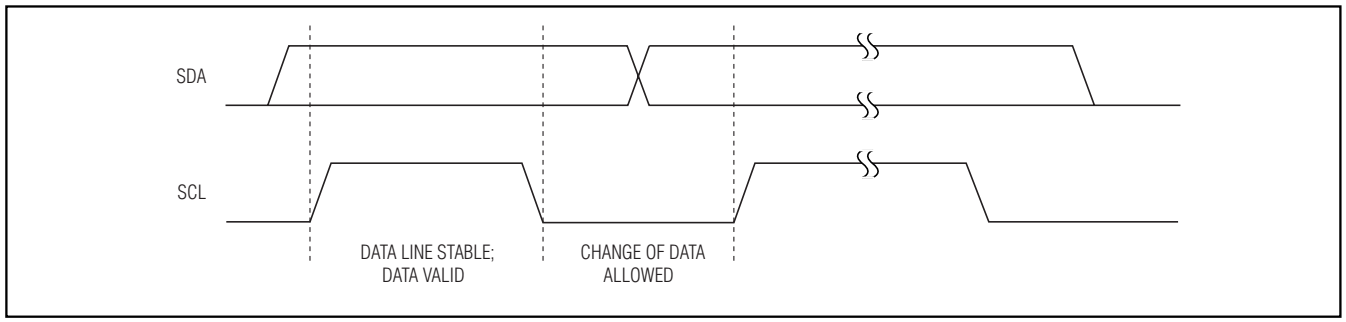

Figure 3. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 4), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7359, the MAX7359 generates the acknowledge bit because the MAX7359 is the recipient. When the MAX7359 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Addresses

The MAX7359 has a 7-bit long slave address (Figure 5). The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

The first 4 bits (MSBs) of the MAX7359 slave address are always 0111. Slave address bits A3, A2, and A1 correspond, by the matrix in Table 10, to the states of the device address input AD0, and A0 corresponds to the R/$\overline{W}$ bit. The AD0 input can be connected to any of four signals: GND, V_{CC}, SDA, or SCL, giving four possible slave address pairs, allowing up to four MAX7359 devices to share the bus. Because SDA and SCL are dynamic signals, care must be taken to ensure that AD0 transitions no sooner than the signals on the SDA and SCL pins.

The MAX7359 monitors the bus continuously, waiting for a START condition followed by its slave address. When the MAX7359 recognizes its slave address, it acknowledges and is then ready for continued communication.

Bus Timeout

The MAX7359 features a 20ms minimum bus timeout on the 2-wire serial interface, largely to prevent the MAX7359 from holding the SDA I/O low during a read transaction if the SCL hangs for any reason before a serial transaction has been completed. Bus timeout operates by causing the MAX7359 to internally terminate a serial transaction, either read or write, if SCL low exceeds 20ms. After a bus timeout, the MAX7359 waits for a valid START condition before responding to a consecutive transmission. This feature can be enabled or disabled under user control by writing to the configuration register (Table 4).

Table 10. 2-Wire Interface Address Map

PIN ADO	DEVICE ADDRESS							
	A7	A6	A5	A4	A3	A2	A1	A0
GND	0	1	1	1	0	0	0	R/$\overline{W}$
V_{CC}	0	1	1	1	0	1	0	R/$\overline{W}$
SDA	0	1	1	1	1	0	0	R/$\overline{W}$
SCL	0	1	1	1	1	1	1	R/$\overline{W}$

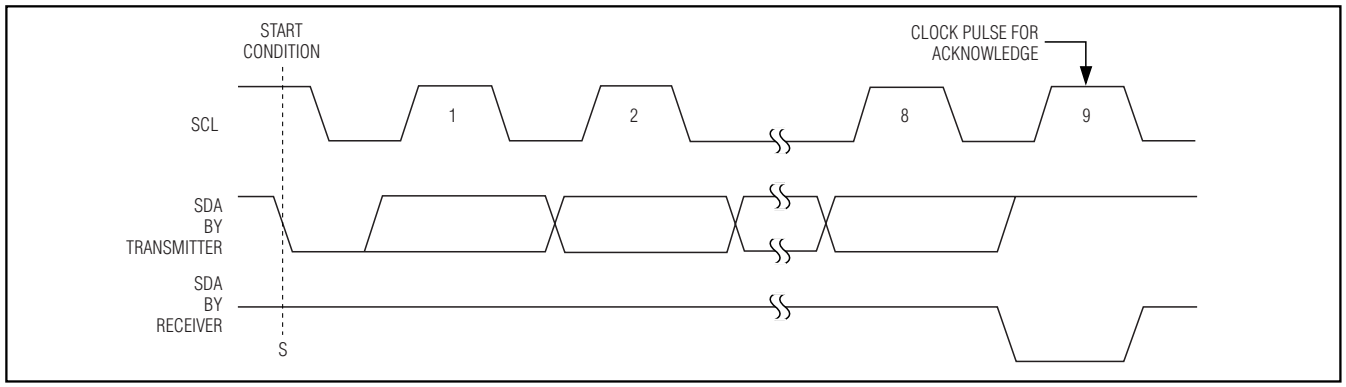

Figure 4. Acknowledge

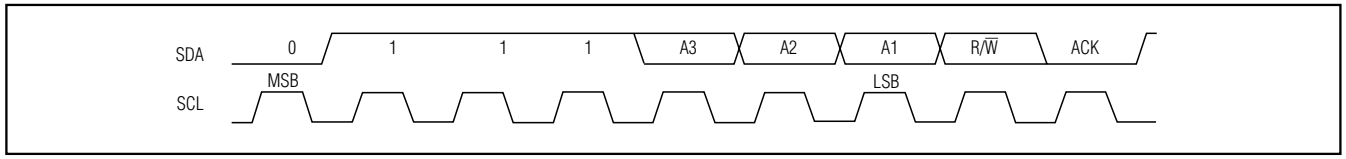

Figure 5. Slave Address

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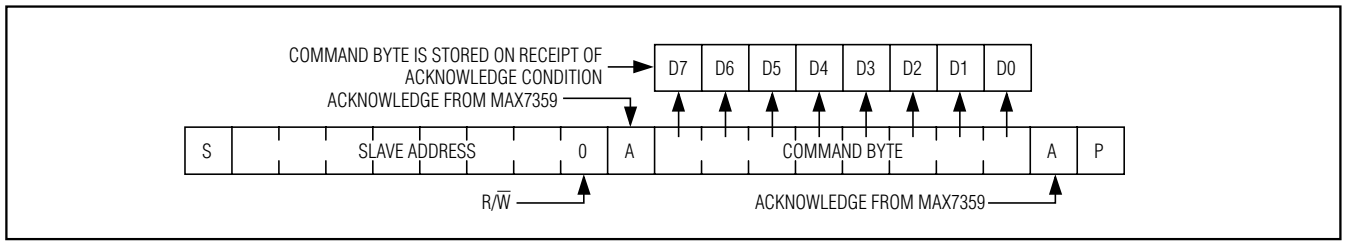

Figure 6. Command Byte Received

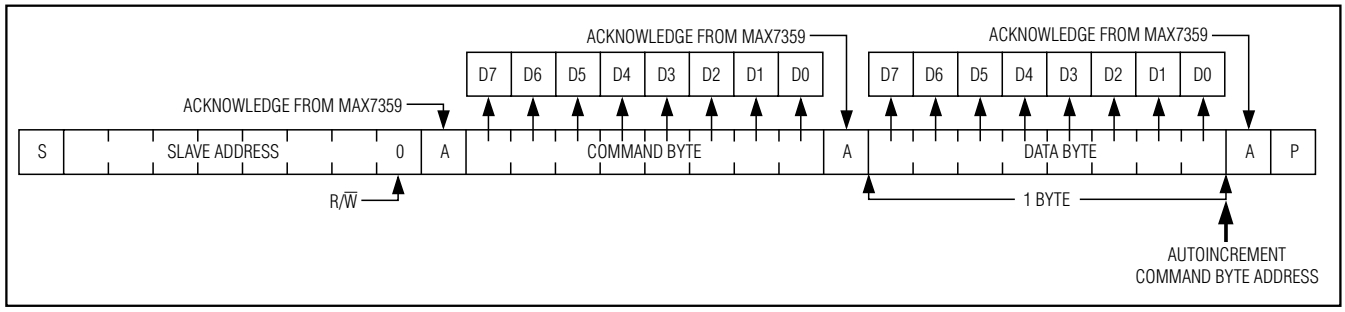

Figure 7. Command and Single Data Byte Received

Message Format for Writing the Key-Scan Controller

A write to the MAX7359 comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX7359 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the MAX7359 takes no further action (Figure 6) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX7359 selected by the command byte (Figure 7).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX7359 internal registers (Table 7) because the command byte address generally autoincrements (Table 11).

Message Format for Reading the Key-Scan Controller

The MAX7359 is read using the MAX7359's internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 11). Thus, a read is initiated by first configuring the MAX7359's command byte by performing a write (Figure 6). The master can now read n consecutive bytes from the MAX7359, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address is generally autoincremented after the write (Figure 8, Table 11).

Table 11. Autoincrement Rules

REGISTER FUNCTION	ADDRESS CODE (hex)	AUTOINCREMENT ADDRESS (hex)
Keys FIFO	0x00	0x00
Autoshutdown	0x06	0x00
All other	0x01 thru 0x05	Addr + 0x01

Operation with Multiple Masters

If the MAX7359 is operated on a 2-wire interface with multiple masters, a master reading the MAX7359 should use a repeated start between the write that sets the MAX7359's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX7359's address pointer but before master 1 has read the data. If master 2 subsequently resets the MAX7359's address pointer, master 1's read may be from an unexpected location.

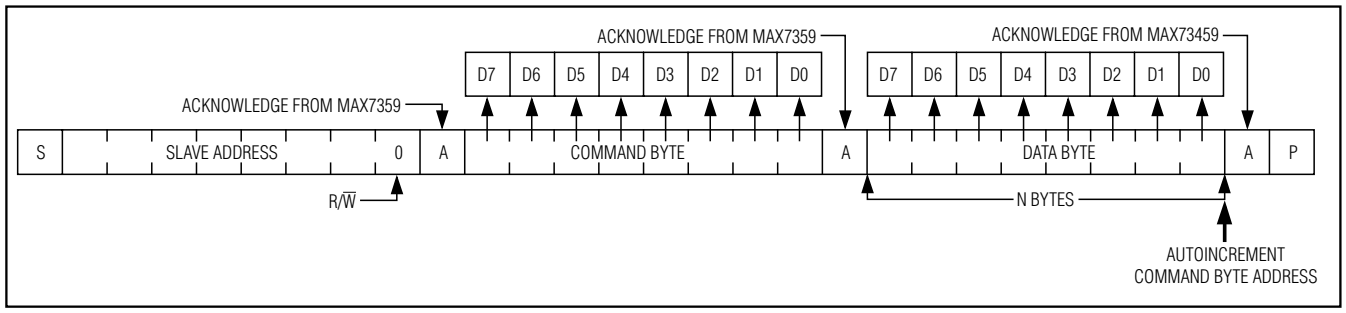

Figure 8. N Data Bytes Received

Command Address Autoincrementing

Address autoincrementing allows the MAX7359 to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX7359 generally increments after each data byte is written or read (Table 11). Autoincrement only works when doing a multiburst read or write.

Applications Information

Ghost-Key Elimination

Ghost keys are a phenomenon inherent with key-switch matrices. When three switches located at the corners of a matrix rectangle are pressed simultaneously, the switch that is located at the last corner of the rectangle (the ghost key) also appears to be pressed. This occurs because the potentials at the two sides of the ghost-key switch are identical due to the other three connections—the switch is electrically shorted by the combination of the other three switches (Figure 9). Because the key appears to be pressed electrically, it is impossible to detect which of the four keys is the ghost key.

The MAX7359 employs a proprietary scheme that detects any three-key combination that generates a fourth ghost key, and does not report the third key that causes a ghost key event. This means that although ghost keys are never reported, many combinations of three keys are effectively ignored when pressed at the same time. Applications requiring three-key combinations (such as <Ctrl><Alt><Del>) must ensure that the three keys are not wired in positions that define the vertices of a rectangle (Figure 10). There is no limit on the number of keys that can be pressed simultaneously as long as the keys do not generate ghost key events and FIFO is not full.

Low-EMI Operation

The MAX7359 uses two techniques to minimize EMI radiating from the key-switch wiring. First, the voltage across the switch matrix never exceeds 0.55V when not in sleep mode, irrespective of supply voltage V_{CC}. This reduces the voltage swing at any node when a switch is pressed to 0.55V maximum. Second, the keys are not dynamically scanned, which would cause the key-switch wiring to continuously radiate interference. Instead, the keys are monitored for current draw (only occurs when pressed), and debounce circuitry only operates when one or more keys are actually pressed.

Power-Supply Considerations

The MAX7359 operates with a 1.62V to 3.6V power-supply voltage. Bypass the power supply to GND with a 0.047µF or higher ceramic capacitor as close as possible to the device.

Switch On-Resistance

The MAX7359 is designed to be insensitive to resistance either in the key switches or the switch routing to and from the appropriate COLx and ROWx up to 5kΩ. These controllers are therefore compatible with low-cost membrane and conductive carbon switches.

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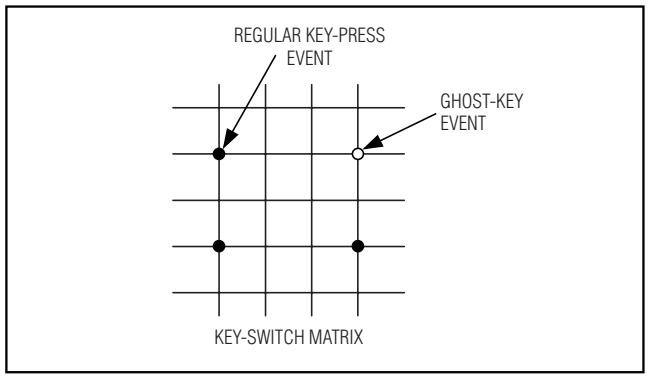


Figure 9. Ghost-Key Phenomenon

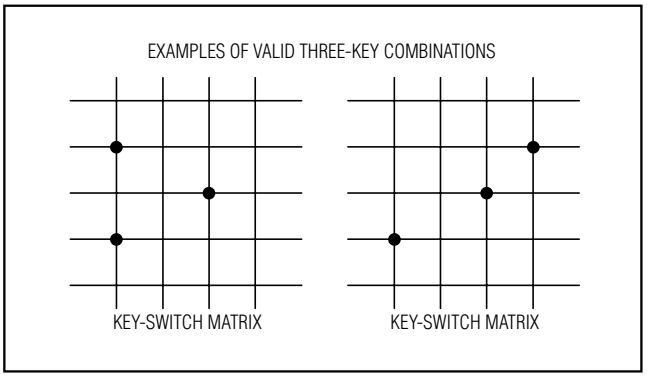
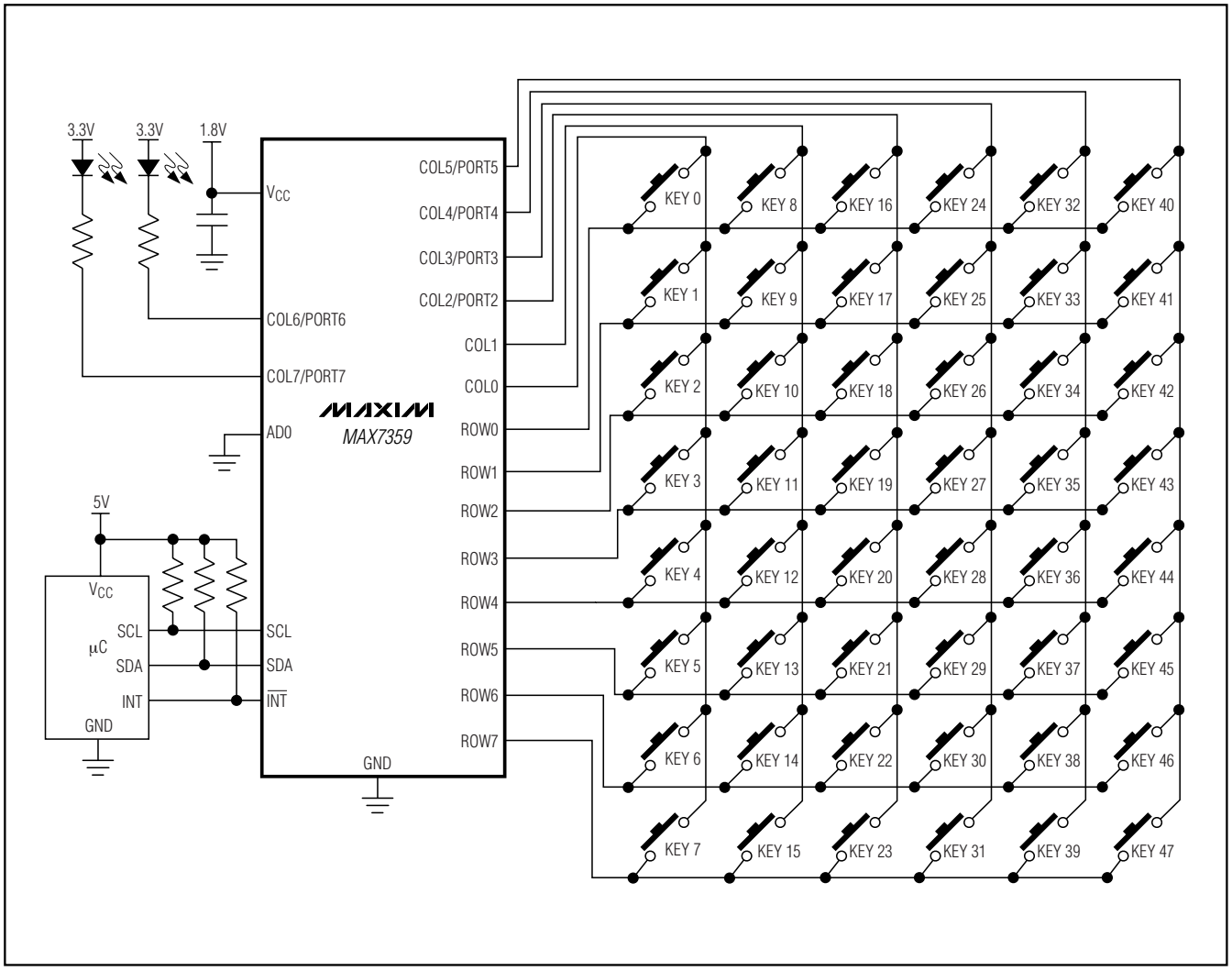


Figure 10. Valid Three-Key Combinations

Chip Information

PROCESS: BiCMOS

Typical Application Circuit



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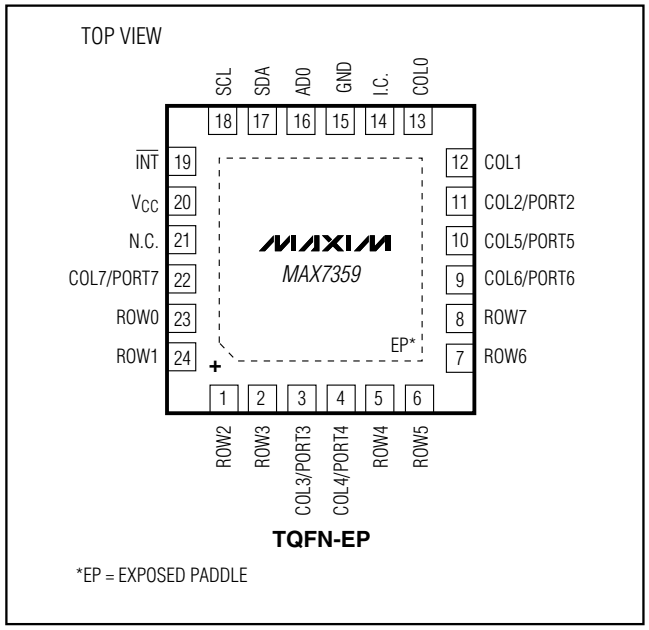
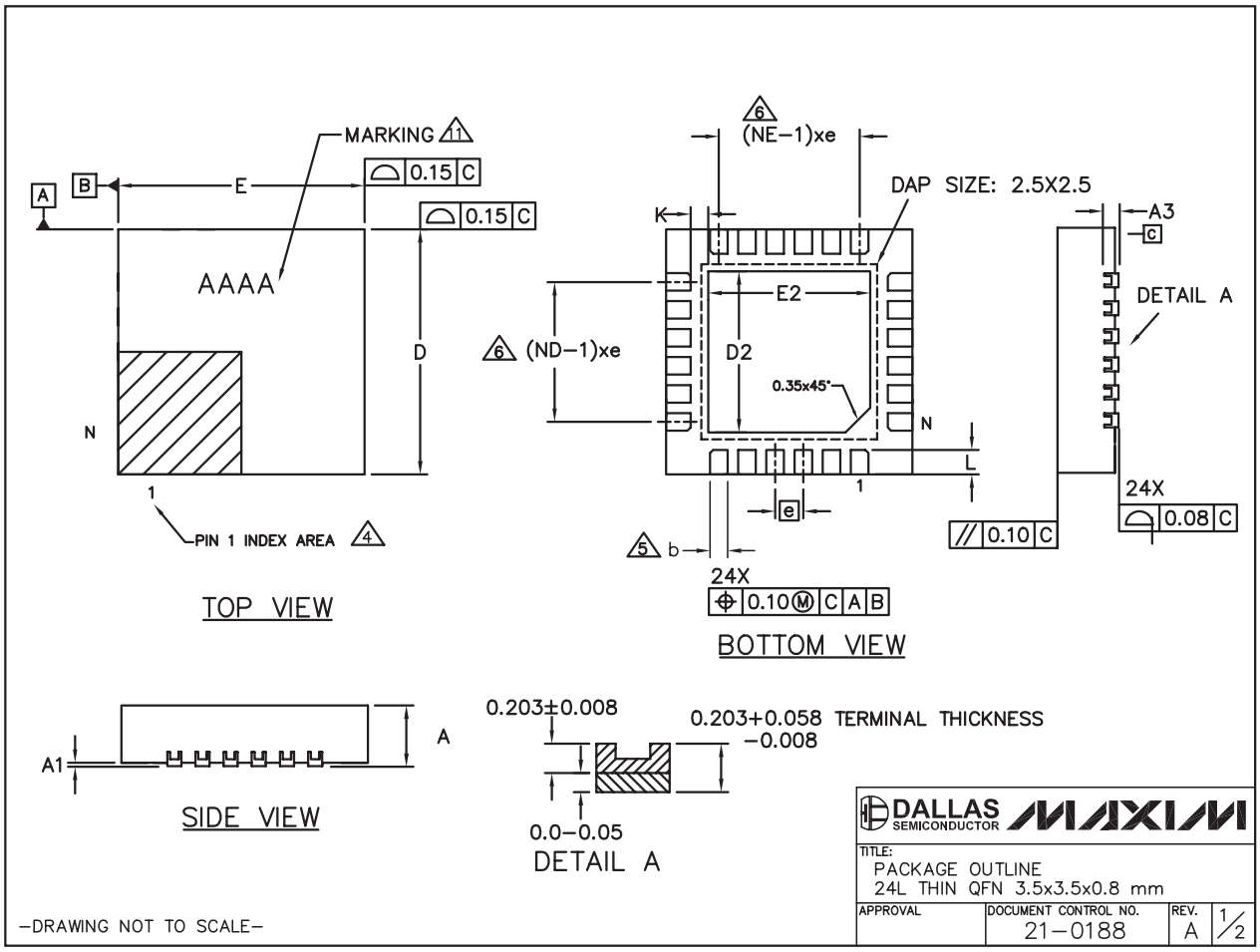
Pin Configuration



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



2-Wire Interfaced Low-EMI Key Switch Controller/GPO

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. REFER TO JEDEC MO–220 EXCEPT D2, E2, & L DIMENSIONS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.

COMMON DIMENSION				NOTE
REF.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
A1	0	–	0.05	
A3		0.20 REF		
b	0.15	0.20	0.25	
D	3.40	3.50	3.60	
E	3.40	3.50	3.60	
e		0.40 BSC.		
K	0.25	–	–	
L	0.30	0.35	0.40	
N		24		
ND		6		
NE		6		

EXPOSED PAD VARIATIONS						
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T243A3–1	2.20	2.30	2.40	2.20	2.30	2.40

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 24L THIN QFN 3.5x3.5x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0188	A	2/2

–DRAWING NOT TO SCALE–