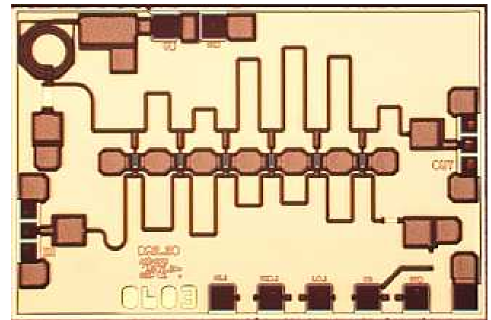
Features

- ♦ **0.1 Watt Saturated Output Power Level**
- ♦ **4 dB Typical Noise Figure**
- ♦ **Select-at-Test Biasing**
- ♦ **MSAG™ Process**



Description

The MAAMGM0002-Die is a 0.1W Distributed Amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. The MMIC can be used as a broadband amplifier stage or as a driver stage in high power applications.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multifunction Self-Aligned Gate Process.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- ♦ **Test Equipment**
- ♦ **Electronic Warfare**
- ♦ **Radar**

Also Available in:

		SAMPLES	
Description	**Ceramic Package**	**Sample Board (Die)**	**Sample Board (Packaged)**
Part Number	MAAMGM0002	MAAMGM0002-DIE-SMB	MAAMGM0002-SMB

Electrical Characteristics: $T_B = 40°C$[1], $Z_0 = 50\Omega$, $V_{DD} = 5V$, $I_{DQ} = 75$ mA[2], $P_{in} = 13$ dBm

Parameter	Symbol	Minimum	Typical	Maximum	Units
Bandwidth	f	1.0		18.0	GHz
Output Power	P_{OUT}	19.5	21		dBm
Power Added Efficiency	PAE		12		%
1-dB Compression Point	P1dB		20		dBm
Small Signal Gain	G	7	9		dB
Noise Figure	NF		4		dB
Output TOI	OTOI		31		dBm
Input VSWR f = 2 GHz	VSWR		1.7:1	2:1	
Output VSWR f = 2 GHz	VSWR		1.7:1	2:1	
Gate Current	I_{GG}		< 2		mA
Drain Current	I_{DD}		100	150	mA

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –1.0 and –0.3 V to achieve I_{DQ} indicated.**

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• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

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Maximum Ratings[3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	19.0	dBm
Drain Voltage	V_{DD}	+7.0	V
Gate Voltage	V_{GG}	-1.5	V
Gate Voltage, Select at Test	HI, MID, LO	-6.0	V
Quiescent Drain Current (No RF)	I_{DQ}	120	mA
Quiescent DC Power Dissipation (No RF)	P_{DISS}	0.5	W
Junction Temperature	T_J	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions[4]

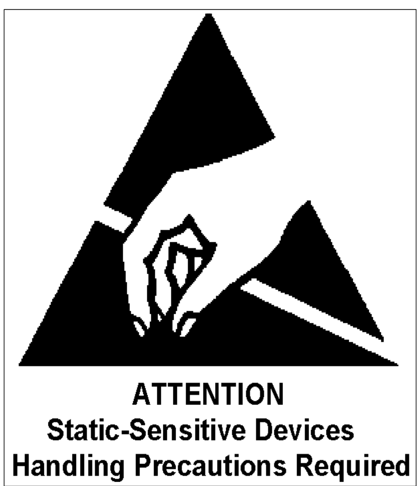
Parameter	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	4.5	5.0	5.5	V
Gate Voltage	V_{GG}	-1.0	-0.6	-0.3	V
Gate Voltage, Select at Test	HI, MID, LO		-5.0		V
Input Power	P_{IN}		13	17	dBm
Thermal Resistance	Θ_{JC}		91.2		°C/W
MMIC Base Temperature	T_B			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.
5. MMIC Base Temperature = 170°C — Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps according to which configuration you are using.

Select-at-Test Gate Bias Figure 5a.	Direct Gate Bias Figure 5b.
1. With V_{DD} = 0, apply V_{GG} = -5V to HI, MID or LO for desired I_{DQ}. 2. Set V_{DD} = 5V. Confirm I_{DQ}. 3. Power down sequence in reverse. 4.Turn off V_{GG} last.	1. With V_{DD} = 0 V, set V_{GG} = -0.8 V. 2. Set V_{DD} = 5 V. 3. Adjust V_{GG} for desired I_{DQ}. 4. Power down sequence in reverse. 5. Turn off V_{GG} last.



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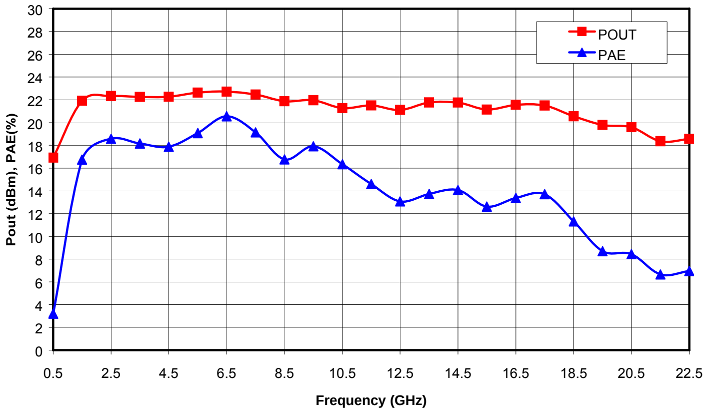

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 5V, P_{in} = 14dBm.

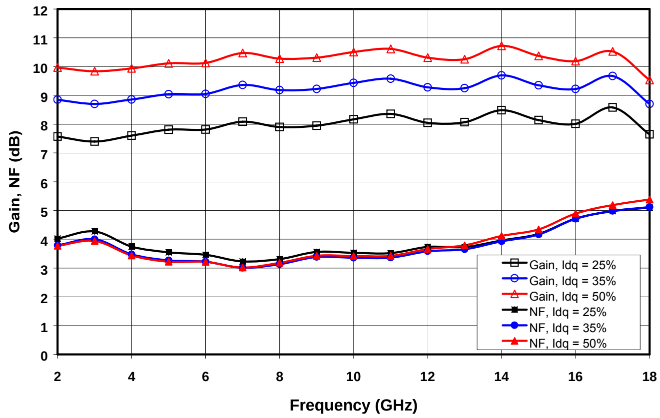

Figure 2. Gain and Noise Figure vs Idq as a Relative Percentage of Idss (50% Idss ~ 100 mA).

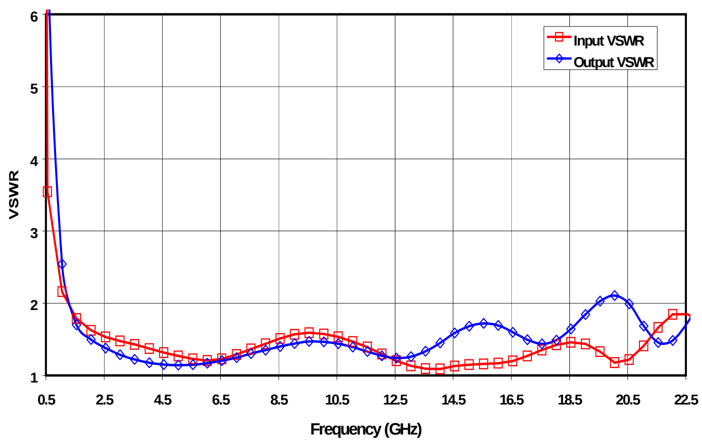

Figure 3. Input and Output VSWR.

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Mechanical Information

Chip Size: 2.98 x 1.98 x 0.075 mm (118 x 78 x 3 mils)

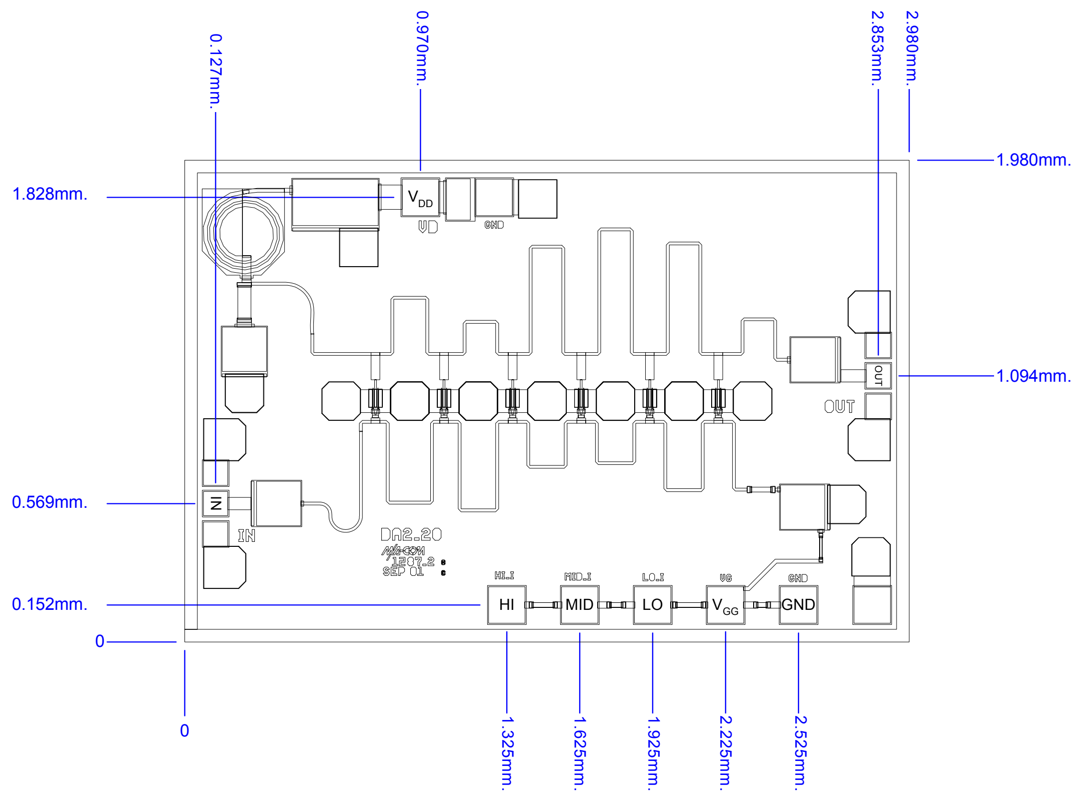


Figure 4. Die Layout

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF: IN, OUT	100 x 100	4 x 4
Drain Supply Voltage: V_{DD}	150 x 150	6 x 6
Direct Gate Supply Voltage: V_{GG}	150 x 150	6 x 6
Select-at-Test Gate Supply Voltage: HI, MID, LO	150 x 150	6 x 6
Ground: GND	150 x 150	6 x 6

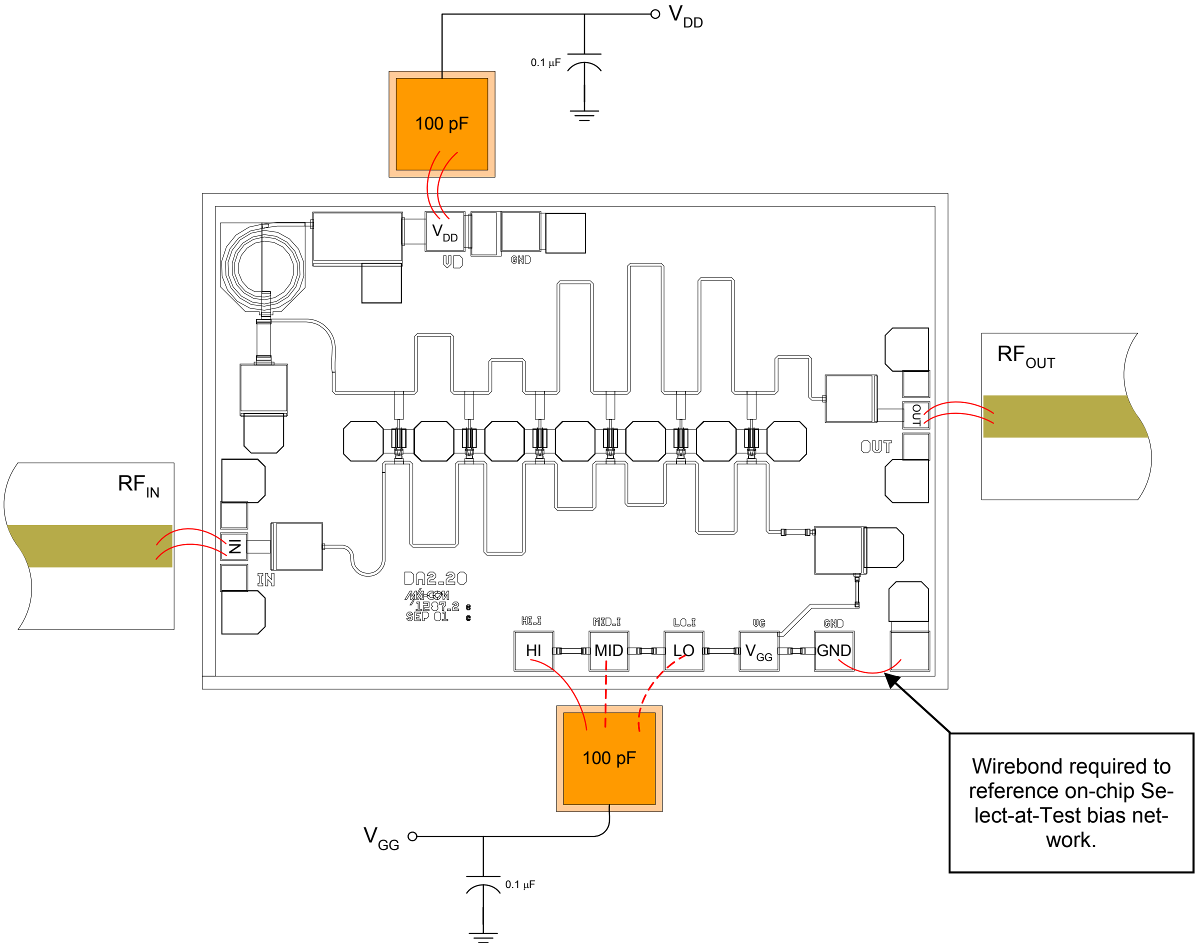


Figure 5a. Required Bonding for Select-at-Test Gate Bias Configuration. Support circuitry typical of MMIC characterization fixture for CW testing.

Pad	Applied Voltage (V)	% IDSS
HI	-5	50
MID	-5	35
LO	-5	25

Assembly and Bonding Diagram

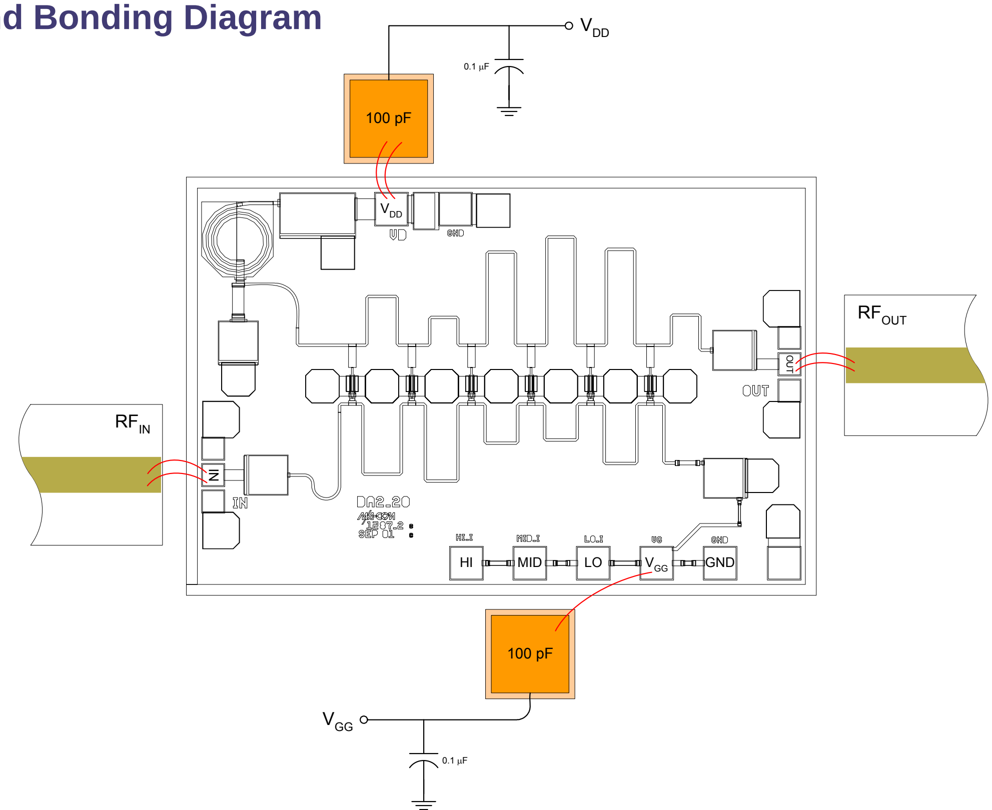


Figure 5b. Required Bonding for Direct Application of Gate Bias. Support circuitry typical of MMIC characterization fixture for CW testing.

Pad	Applied Voltage (V)	% IDSS
V_{GG}	-1.0 to -0.3	25 - 50

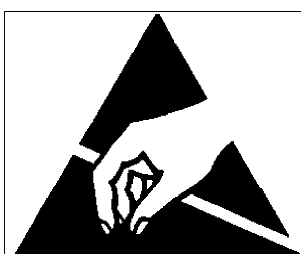
Die Handling:

Refer to Application Note AN3016.

Assembly Instructions:

Die Attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 310 °C to less than 7 minutes. Refer to Application Note AN3017 for more detailed information.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.



ATTENTION
Static-Sensitive Devices
Handling Precautions Required

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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