M36P0R9070E0

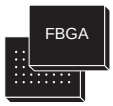
512 Mbit (x16, Multiple Bank, Multi-Level, Burst) Flash memory 128 Mbit (Burst) PSRAM, 1.8V supply, Multi-Chip Package

Feature summary

- Multi-Chip Package
  - 1 die of 512 Mbit (32Mb x 16, Multiple Bank, Multi-Level, Burst) Flash Memory
  - 1 die of 128Mbit (8Mb x16) PSRAM
- Supply voltage
  - V_{DDF} = V_{CCP} = V_{DDQ} = 1.7 to 1.95V
  - V_{PPF} = 9V for fast program
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code: 8819
- ECOPACK® package available

Flash memory

- Synchronous / Asynchronous Read
  - Synchronous Burst Read mode: 108MHz, 66MHz
  - Asynchronous Page Read mode
  - Random Access: 96ns
- Programming time
  - 4.2µs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple bank memory array: 64 Mbit banks
  - Four Extended Flash Array (EFA) Blocks of 64 Kbits
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between read and write operations
- Security
  - 2112-bit user programmable OTP Cells
  - 64-bit unique device number
- 100,000 program/erase cycles per block
- Common Flash Interface (CFI)



TFBGA107 (ZAC)

- Block locking
  - All Blocks locked at power-up
  - Any combination of Blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with V_{PPF} = V_{SS}

PSRAM

- Access time: 70ns
- User-selectable operating modes
  - Asynchronous modes: Random Read, and Write, Page Read
  - Synchronous modes: NOR-Flash, Full Synchronous (Burst Read and Write)
- Asynchronous Page Read
  - Page Size: 4, 8 or 16 Words
  - Subsequent Read Within Page: 20ns
- Burst Read
  - Fixed Length (4, 8, 16 or 32 Words) or Continuous
  - Maximum Clock Frequency: 80MHz
- Low Power Consumption
  - Active Current: < 25mA
  - Standby Current: 200µA
  - Deep Power-Down Current: 10µA
- Low Power Features
  - Partial Array Self Refresh (PASR)
  - Deep Power-Down (DPD) Mode

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1 Summary description

The M36P0R9070E0 combines two memory devices in one Multi-Chip Package:

- 512-Mbit Multiple Bank Flash memory (the M58PR512J).
- 128 Mbit PSRAM (the M69KB128AB).

The purpose of this document is to describe how the two memory components operate with respect to each other. It should be read in conjunction with the M58PRxxxJ and M69KB128AB datasheets, where all specifications required to operate the Flash memory and PSRAM components are fully detailed. The M58PR512J and M69KB128AB datasheets are available from *www.st.com*.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA107 package. It is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

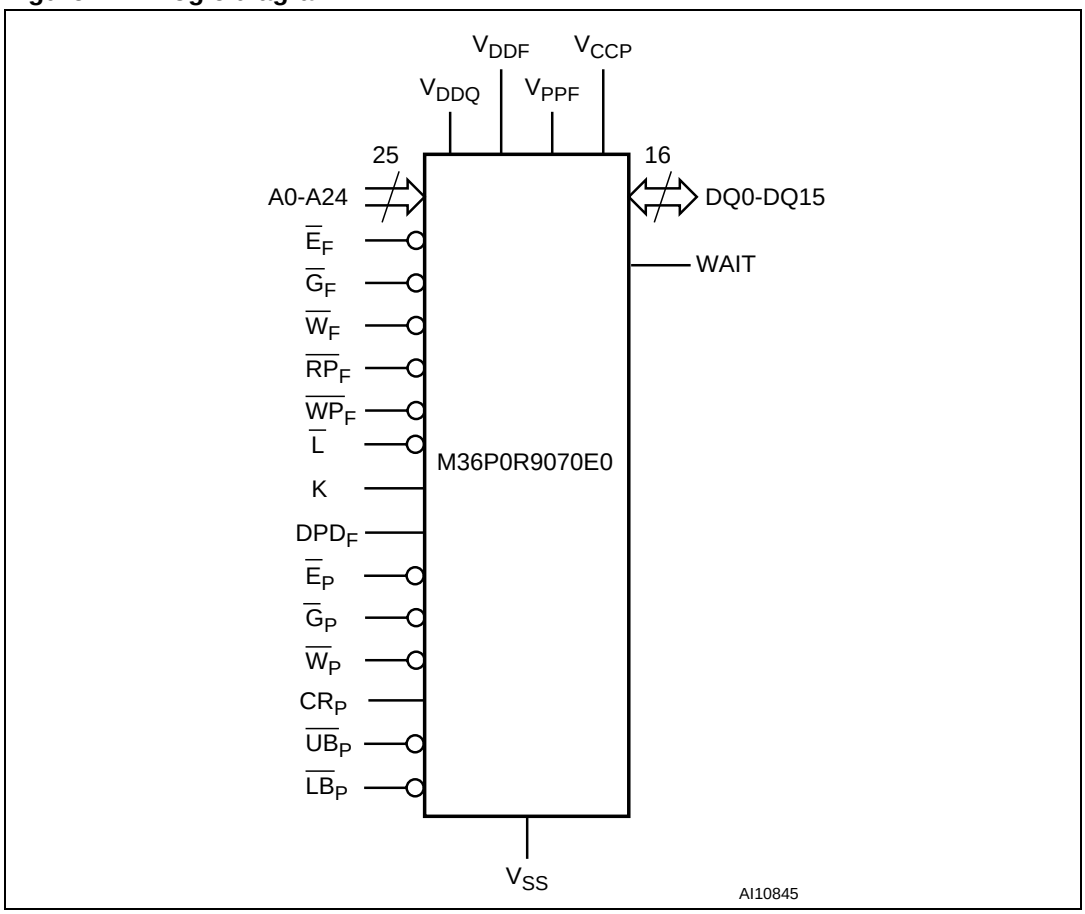
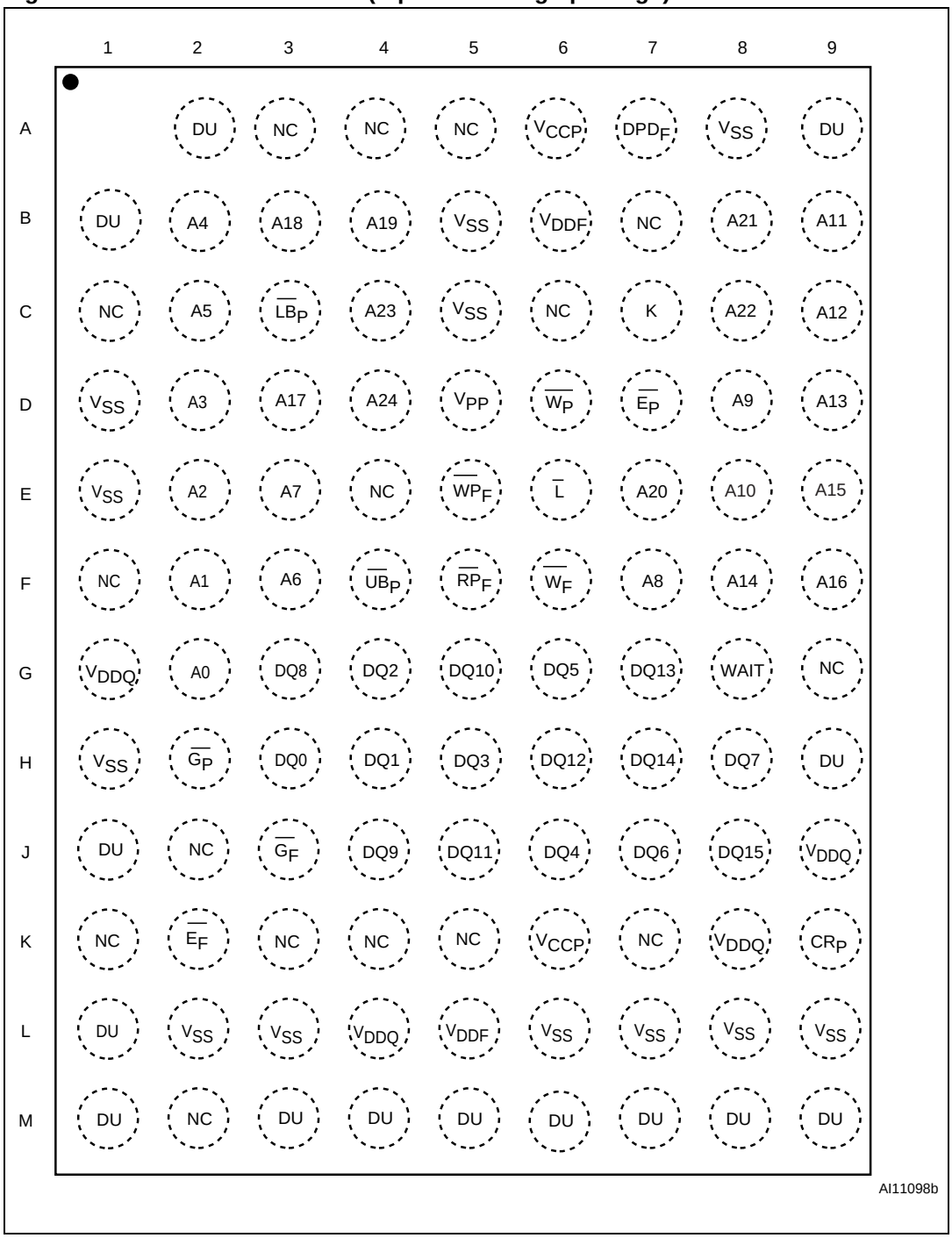


Table 1. Signal names

A0-A24(1)	Address Inputs
DQ0-DQ15	Common Data Input/Output
V_{DDQ}	Common Flash and PSRAM Power Supply for I/O Buffers
V_{PPF}	Flash Memory Optional Supply Voltage for Fast Program & Erase
V_{DDF}	Flash Memory Power Supply
V_{CCP}	PSRAM Power Supply
V_{SS}	Ground
$\overline{L}$	Latch Enable input
K	Burst Clock
WAIT	Wait Output
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory	
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable Input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
DPD_F	Deep Power-Down
PSRAM	
$\overline{E}_P$	Chip Enable Input
$\overline{G}_P$	Output Enable Input
$\overline{W}_P$	Write Enable Input
CR_P	Configuration Register Enable Input
$\overline{UB}_P$	Upper Byte Enable Input
$\overline{LB}_P$	Lower Byte Enable Input

1. A23-A24 are Address Inputs for the Flash memory component only.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1., Logic diagram* and *Table 1., Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A24)

Addresses A0-A22 are common inputs for the Flash memory and PSRAM components. Addresses A23 and A24 are inputs for Flash memory components only. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable signal ($\overline{W}_F$), while the PSRAM is accessed through the Chip Enable signal ($\overline{E}_P$) and the Write Enable signal ($\overline{W}_P$).

$\overline{E}_F$ Low, and $\overline{E}_P$ must not be Low at the same time.

2.2 Data input/output (DQ0-DQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

For the PSRAM component, the upper Byte Data Inputs/Outputs (DQ8-DQ15) carry the data to or from the upper part of the selected address when Upper Byte Enable ($\overline{UB}_P$) is driven Low. The lower Byte Data Inputs/Outputs (DQ0-DQ7) carry the data to or from the lower part of the selected address when Lower Byte Enable ($\overline{LB}_P$) is driven Low. When both $\overline{UB}_P$ and $\overline{LB}_P$ are disabled, the Data Inputs/ Outputs are high impedance.

2.3 Latch Enable ($\overline{L}$)

The Latch Enable pin is common to the Flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KB128AB for the PSRAM and M58PR512J for the Flash memory.

2.4 Clock (K)

The Clock input pin is common to the Flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KB128AB for the PSRAM and M58PR512J for the Flash memory.

2.5 Wait (WAIT)

WAIT is an output pin common to the Flash memory and PSRAM components. However the WAIT signal does not behave in the same way for the PSRAM and the Flash memory.

For details of how it behaves, please refer to the M69KB128AB datasheet for the PSRAM and to the M58PR512J datasheet for the Flash memory.

2.6 Flash Chip Enable input ($\overline{E}_F$)

The Flash Chip Enable input activates the control logic, input buffers, decoders and sense amplifiers of the Flash memory component selected. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the corresponding Flash memory are deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to have $\overline{E}_F$ at V_{IL} and $\overline{E}_P$ at V_{IL} at the same time. Only one memory component can be enabled at a time.

2.7 Flash Output Enable inputs ($\overline{G}_F$)

The Output Enable pins control the data outputs during Flash memory Bus Read operations.

2.8 Flash Write Enable ($\overline{W}_F$)

The Write Enable controls the Bus Write operation of the Flash memory Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.9 Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M58PR512J datasheet).

2.10 Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the Flash memories. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to the M58PRxxxJ datasheet, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58PRxxxJ datasheet).

2.11 PSRAM Chip Enable input ($\overline{E}_P$)

The Chip Enable input activates the PSRAM when driven Low (asserted). When deasserted (V_{IH}), the device is disabled, and goes automatically in low-power Standby mode or Deep Power-down mode.

2.12 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$, controls the Bus Write operation of the PSRAM. When asserted (V_{IL}), the device is in Write mode and Write operations can be performed either to the configuration registers or to the memory array.

2.13 PSRAM Output Enable ($\overline{G}_P$)

Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

2.14 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte En-able, $\overline{UB}_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

2.15 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.16 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH}, Write operations load either the value of the Refresh Configuration Register (RCR) or the Bus configuration register (BCR).

2.17 Deep Power-Down input (DPD_F)

The Deep Power-Down input is used to place the device in a Deep Power-Down mode.When the device is in Deep Power-Down mode, the memory cannot be modified and data is protected.

For further details on how the Deep Power-Down input signal works, please refer to the M58PR512J datasheet.

2.18 V_{DDF} Supply Voltages

V_{DDF} provides the power supply to the internal cores of the Flash memory. It is the main power supply for all Flash memory operations (Read, Program and Erase).

2.19 V_{CCP} Supply Voltage

V_{CCP} provides the power supply to the internal core of the PSRAM device. It is the main power supply for all PSRAM operations.

2.20 V_{DDQ} Supply Voltage

V_{DDQ} provides the power supply for the Flash memory and PSRAM I/O pins. This allows all Outputs to be powered independently of the Flash memory and SRAM core power supplies, V_{DDF} and V_{CCP}.

2.21 V_{PPF} Program Supply Voltage

V_{PPF} is both a control input and a power supply pin for the Flash memory. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against Program or Erase, while $V_{PPF} > V_{PP1}$ enables these functions (see the M58PRxxxJ datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

2.22 V_{SS} Ground

V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5., AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for Flash and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is a simultaneous read operations on the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

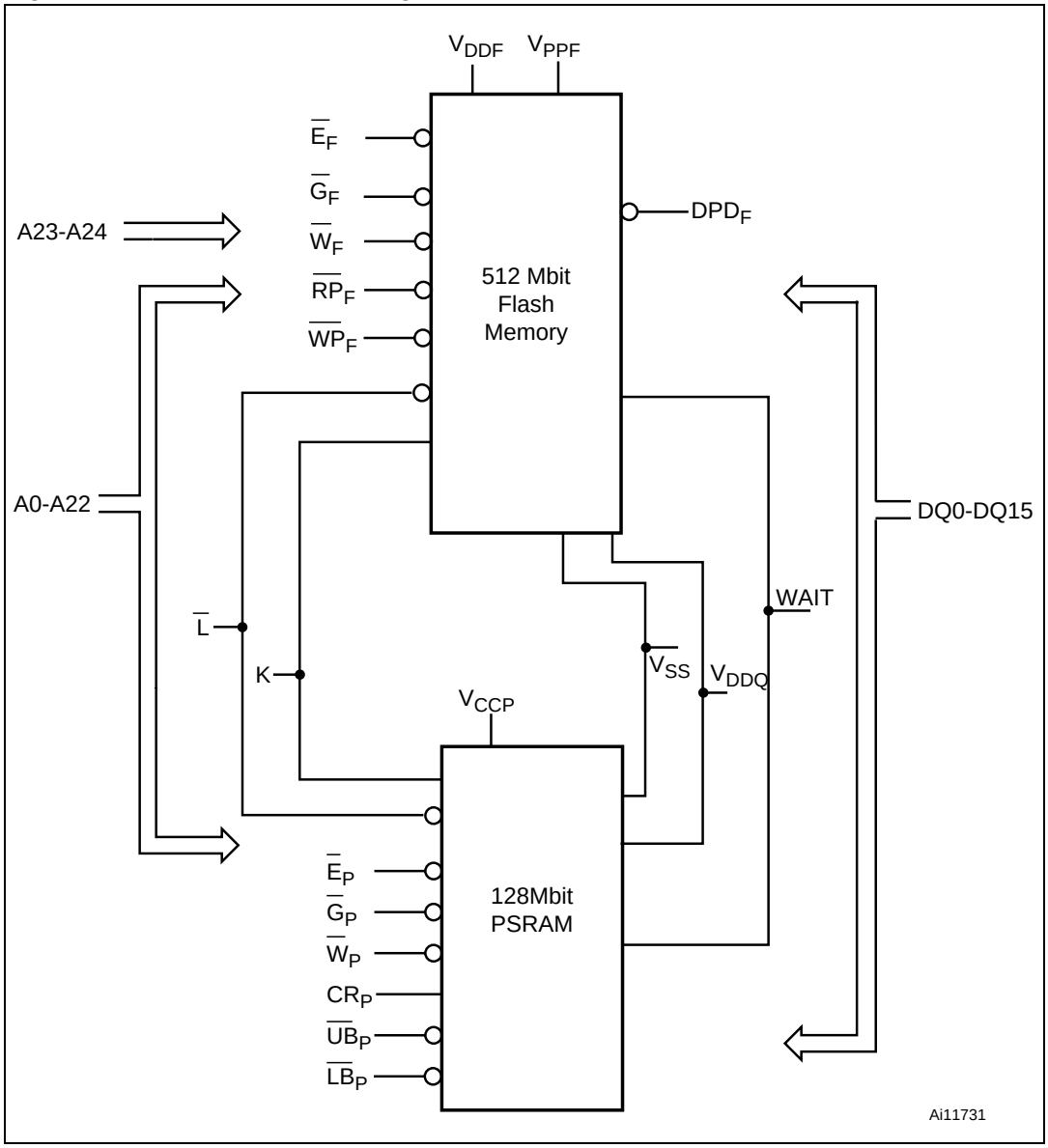


Table 2. Main operating modes(1)

	Operation	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{RP}_F$	DPD_F (2)	WAIT (3)	$\overline{L}$	$\overline{E}_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{UB}_P$	$\overline{LB}_P$	CR_P	A19	A18	A0-A17 A20-A22	DQ0-DQ7	DQ8-DQ15
Flash memory	Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	de-a(4)		V_{IL}(5)	PSRAM must be disabled									Data Output	
	Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	de-a(4)		V_{IL}(5)										Data Input	
	Address Latch	V_{IL}	X	V_{IH}	V_{IH}	de-a(4)		V_{IL}										Data Output or Hi-Z(6)	
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	de-a(4)	Hi-Z	X	Any PSRAM mode is allowed									Hi-Z	
	Standby	V_{IH}	X	X	V_{IH}	de-a(4)	Hi-Z	X										Hi-Z	
	Reset	X	X	X	V_{IL}	de-a(4)	Hi-Z	X										Hi-Z	
	Deep Power-Down	V_{IH}	X	X	V_{IH}	a(7)	Hi-Z	X										Hi-Z	
PSRAM	Word Read	The Flash memory must be disabled					Low-Z	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	Valid			Output Valid	Output Valid
	Lower Byte Read										V_{IL}	V_{IH}	V_{IL}	V_{IL}	Valid			Output Valid	High-Z
	Upper Byte Read										V_{IL}	V_{IL}	V_{IH}	V_{IL}	Valid			High-Z	Output Valid
	Word Write									V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	Valid			Input Valid	Input Valid
	Lower Byte Write										X	V_{IH}	V_{IL}	V_{IL}	Valid			Input Valid	Invalid
	Upper Byte Write										X	V_{IL}	V_{IH}	V_{IL}	Valid			Invalid	Input Valid
	Read CR (CR Controlled Method)									V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	00(RCR)10(BCR)X1(DIDR)(8)		X	BCR/RCR/DIDR Content	
	Program CR (CR Controlled)(9)									V_{IH}	X	X	X		00(RCR)10(BCR)(8)		BCR/RCR Data	High-Z	
	No Operation	Any Flash memory mode is allowed							V_{IL}	X	X	X	X	V_{IL}	X	X	X	X	
	Deep Power-Down(10)						Hi-Z	X	V_{IH}	X	X	X	X	X	X	X	X	High-Z	
	Standby								V_{IH}	X	X	X	X	V_{IL}	X	X	X	High-Z	

1. X = Don't care, de-a = de-asserted, a = asserted, CR = Configuration Register.
2. The DPD_F signal polarity depends on the value of the ECR14 bit.
3. In the Flash memory the WAIT signal polarity is configured using the Set Configuration Register command.
4. If ECR15 is set to '0', the Flash memory cannot enter the Deep Power-Down mode, even if DPD_F is asserted.
5. In the Flash memory $\overline{L}$ can be tied to V_{IH} if the valid address has been previously latched.
6. Depends on $\overline{G}_F$.
7. ECR15 has to be set to '1' for the Flash memory to enter Deep Power-Down.
8. A18 and A19 are used to select the BCR, RCR or DIDR registers.
9. BCR and RCR only.
10. Bit 4 of the Refresh Configuration Register must be set to '0', bit 4 (BCR4) of the Bus Configuration Register must be set to '0', and $\overline{E}$ has to be maintained High, V_{IH}, during Deep Power-Down mode.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–30	85	°C
T_{BIAS}	Temperature Under Bias	–30	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.2	2.45	V
V_{DD}	Supply Voltage	–0.2	2.45	V
V_{DDQ}	Input/Output Supply Voltage	–0.2	2.45	V
V_{PP}	Program Voltage	–1.0	11.5	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4., Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{CCP} Supply Voltage	–	–	1.7	1.95	V
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{DDQ} Supply Voltage	1.7	1.95	1.7	1.95	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Ambient Operating Temperature	–30	85	–30	85	°C
Load Capacitance (C_L)	30		30		pF
Impedance Output (Z_0)	50				Ω
Output Circuit Protection Resistance (R)	50				Ω
Input Rise and Fall Times		3		2	ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDQ}/2$		V

Figure 4. AC measurement I/O waveform

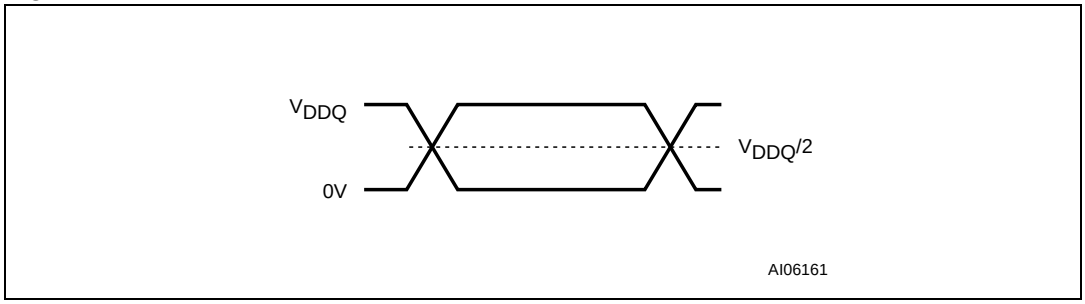


Figure 5. AC measurement load circuit

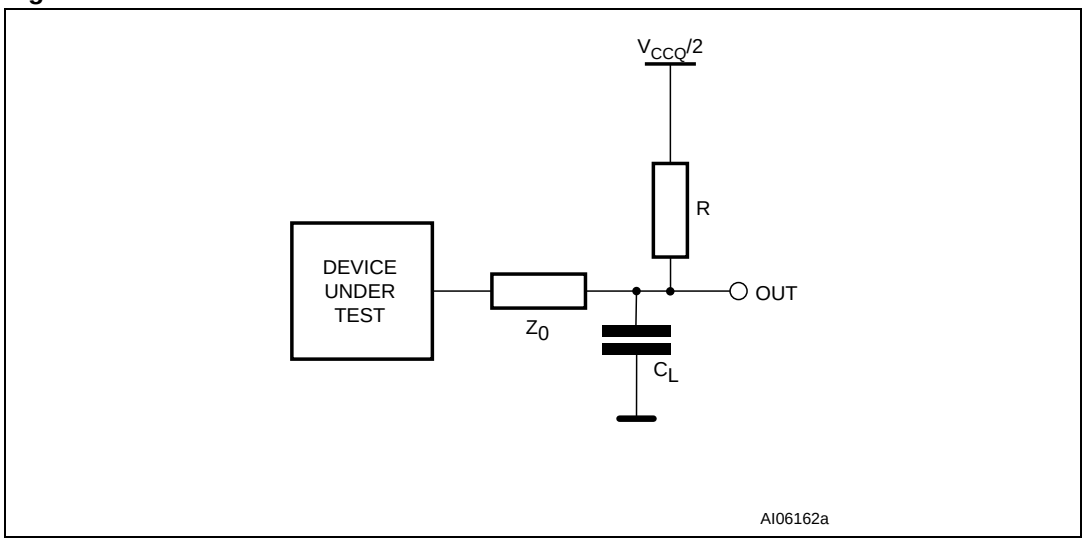


Table 5. Capacitance(1)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		14	pF

1. Sampled only, not 100% tested.

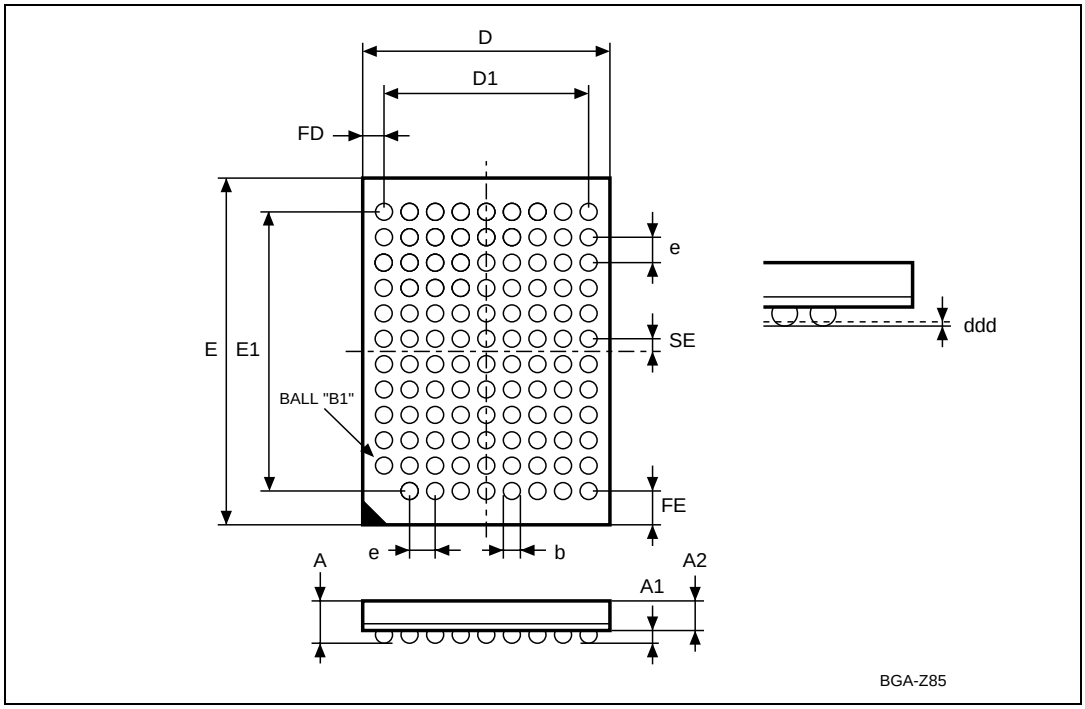
Please refer to the M58PRxxxJ and M69KB128AB datasheets for further DC and AC characteristic values and illustrations.

6 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 6. TFBGA107 8 × 11mm - 9 × 12 active ball array, 0.8mm pitch, package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA107 8 × 11mm - 9 × 12 active ball array, 0.8mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.20			0.008	
A2	0.85			0.033		
b	0.35	0.30	0.40	0.014	0.012	0.016
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	6.40			0.252		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	8.80			0.346		
e	0.80			0.031		
FD	0.80			0.031		
FE	1.10			0.043		
SE	0.40			0.016		

7 Part numbering

Table 7. Ordering information scheme

M36 P 0 R 9 0 7 0 E 0 ZAC E

Example:

Device Type

M36 = Multi-Chip Package (Multiple Flash + PSRAM)

Flash 1 Architecture

P = Multi-Level, Multiple Bank, Large Buffer

Flash 2 Architecture

0 = No Die

Operating Voltage

R = V_{DDF} = V_{CCP} = V_{DDQ} = 1.7 to 1.95V

Flash 1 Density

9 = 512 Mbits

Flash 2 Density

0 = No Die

RAM 1 Density

7 = 128 Mbits

RAM 0 Density

0 = No Die

Parameter Blocks Location

E = Even Block Flash Memory Configuration

Product Version

0 = 90nm Flash technology, 96ns speed; PSRAM

Package

ZAC= stacked TFBGA107 C stacked footprint.

Option

Blank = Standard Packing

E = ECOPACK® Package, Standard packing

F = ECOPACK® Package, Tape & Reel packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
28-Nov-2005	1	Initial release.
13-Jul-2006	2	Document status promoted from Preliminary data to full Datasheet. Document updated to latest version of M58PRxxxJ datasheet, DC characteristics tables removed (for values refer to M58PRxxxJ and M69KB128AB datasheets). PSRAM part replaced by M69KB128AB. H9 ball is DU in *Figure 2: TFBGA connections (top view through package)*. T_{STG} min and V_{PP} max modified in *Table 3: Absolute maximum ratings*. *Table 2: Main operating modes* modified. PSRAM value for Input Rise and Fall Times filled in in *Table 4: Operating and AC measurement conditions*.

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