

**LC75814V****1/4 Duty General-Purpose LCD Driver****Overview**

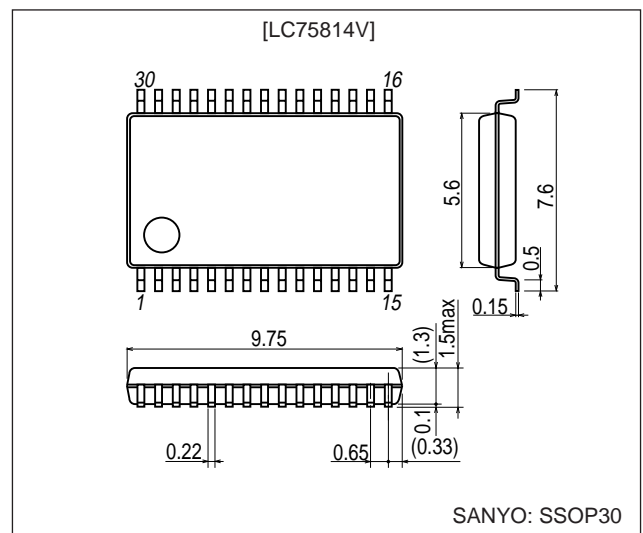
The LC75814V is a 1/4 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The LC75814V can drive an LCD with up to 64 segments directly. The LC75814V can also control up to 4 general-purpose output ports. Since the LC75814V uses separate power supply systems for the LCD drive block and the logic block, the LCD driver block power-supply voltage can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.

**Features**

- Support for 1/4 duty 1/2 bias or 1/4 duty 1/3 bias drive of up to 64 segments under serial data control.
- Serial data input supports CCB format communication with the system controller.
- Serial data control of the power-saving mode based backup function and all the segments forced off function
- Serial data control of switching between the segment output port and the general-purpose output port functions
- High generality, since display data is displayed directly without decoder intervention.
- Independent  $V_{LCD}$  for the LCD driver block ( $V_{LCD}$  can be set to any voltage in the range 2.7 to 6.0 volts, regardless of the logic block power-supply voltage.)
- The  $\overline{INH}$  pin can force the display to the off state.
- RC oscillator circuit

**Package Dimensions**

unit: mm

**3191A-SSOP30**

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- CCB is a SANYO's original bus format and all the bus addresses are controlled by SANYO.

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**SANYO Electric Co.,Ltd. Semiconductor Company**

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## LC75814V

### Specifications

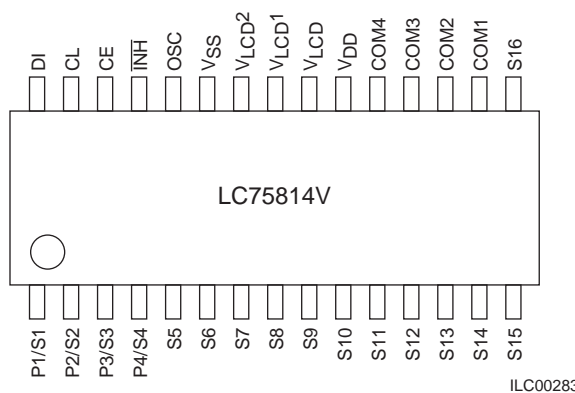
**Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD max</sub>	V <sub>DD</sub>	-0.3 to +7.0	V
	V <sub>LCD max</sub>	V <sub>LCD</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN 1</sub>	CE, CL, DI, $\overline{\text{INH}}$	-0.3 to +7.0	V
	V <sub>IN 2</sub>	OSC	-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>IN 3</sub>	V <sub>LCD 1</sub> , V <sub>LCD 2</sub>	-0.3 to V <sub>LCD</sub> + 0.3	V
Output voltage	V <sub>OUT 1</sub>	OSC	-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>OUT 2</sub>	S1 to S16, COM1 to COM4, P1 to P4	-0.3 to V <sub>LCD</sub> + 0.3	V
Output current	I <sub>OUT 1</sub>	S1 to S16	300	μA
	I <sub>OUT 2</sub>	COM1 to COM4	3	mA
	I <sub>OUT 3</sub>	P1 to P4	5	mA
Allowable power dissipation	Pd max	Ta = 85°C	100	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

**Allowable Operating Ranges at Ta = -40 to +85°C, VSS = 0 V**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	2.7		6.0	V
	V <sub>LCD</sub>	V <sub>LCD</sub>	2.7		6.0	V
Input voltage	V <sub>LCD1</sub>	V <sub>LCD1</sub>		2/3 V <sub>LCD</sub>	V <sub>LCD</sub>	V
	V <sub>LCD2</sub>	V <sub>LCD2</sub>		1/3 V <sub>LCD</sub>	V <sub>LCD</sub>	V
Input high level voltage	V <sub>IH</sub>	CE, CL, DI, $\overline{\text{INH}}$	0.8 V <sub>DD</sub>		6.0	V
Input low level voltage	V <sub>IL</sub>	CE, CL, DI, $\overline{\text{INH}}$	0		0.2 V <sub>DD</sub>	V
Recommended external resistance	R <sub>OSC</sub>	OSC		43		kΩ
Recommended external capacitance	C <sub>OSC</sub>	OSC		680		pF
Guaranteed oscillation range	f <sub>OSC</sub>	OSC	25	50	100	kHz
Data setup time	t <sub>ds</sub>	CL, DI: Figure 2	160			ns
Data hold time	t <sub>dh</sub>	CL, DI: Figure 2	160			ns
CE wait time	t <sub>cp</sub>	CE, CL: Figure 2	160			ns
CE setup time	t <sub>cs</sub>	CE, CL: Figure 2	160			ns
CE hold time	t <sub>ch</sub>	CE, CL: Figure 2	160			ns
High level clock pulse width	t <sub>øH</sub>	CL: Figure 2	160			ns
Low level clock pulse width	t <sub>øL</sub>	CL: Figure 2	160			ns
Rise time	t <sub>r</sub>	CE, CL, DI: Figure 2		160		ns
Fall time	t <sub>f</sub>	CE, CL, DI: Figure 2		160		ns
$\overline{\text{INH}}$ switching time	t <sub>c</sub>	$\overline{\text{INH}}$ , CE: Figure 3	10			μs

### Pin Assignment

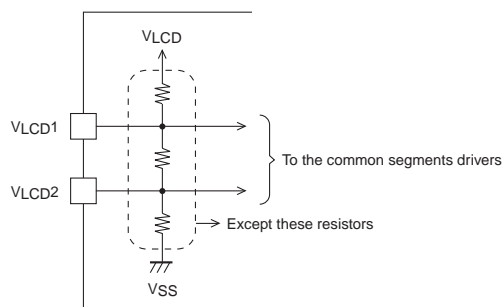


## LC75814V

### Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	$V_H$	CE, CL, DI, $\overline{\text{INH}}$		$0.1 V_{DD}$		V
Input high level current	$I_{IH}$	CE, CL, DI, $\overline{\text{INH}}$ ; $V_I = 6.0 \text{ V}$			5.0	$\mu\text{A}$
Input low level current	$I_{IL}$	CE, CL, DI, $\overline{\text{INH}}$ ; $V_I = 0 \text{ V}$	-5.0			$\mu\text{A}$
Output high level voltage	$V_{OH1}$	S1 to S16; $I_O = -20 \mu\text{A}$	$V_{LCD} - 0.9$			V
	$V_{OH2}$	COM1 to COM4; $I_O = -100 \mu\text{A}$	$V_{LCD} - 0.9$			V
	$V_{OH3}$	P1 to P4; $I_O = -1 \text{ mA}$	$V_{LCD} - 0.9$			V
Output low level voltage	$V_{OL1}$	S1 to S16; $I_O = 20 \mu\text{A}$			0.9	V
	$V_{OL2}$	COM1 to COM4; $I_O = 100 \mu\text{A}$			0.9	V
	$V_{OL3}$	P1 to P4; $I_O = 1 \text{ mA}$			0.9	V
Output middle level voltage*1	$V_{MID1}$	COM1 to COM4; 1/2 bias, $I_O = \pm 100 \mu\text{A}$	$1/2 V_{LCD} - 0.9$		$1/2 V_{LCD} + 0.9$	V
	$V_{MID2}$	S1 to S16; 1/3 bias, $I_O = \pm 20 \mu\text{A}$	$2/3 V_{LCD} - 0.9$		$2/3 V_{LCD} + 0.9$	V
	$V_{MID3}$	S1 to S16; 1/3 bias, $I_O = \pm 20 \mu\text{A}$	$1/3 V_{LCD} - 0.9$		$1/3 V_{LCD} + 0.9$	V
	$V_{MID4}$	COM1 to COM4; 1/3 bias, $I_O = \pm 100 \mu\text{A}$	$2/3 V_{LCD} - 0.9$		$2/3 V_{LCD} + 0.9$	V
	$V_{MID5}$	COM1 to COM4; 1/3 bias, $I_O = \pm 100 \mu\text{A}$	$1/3 V_{LCD} - 0.9$		$1/3 V_{LCD} + 0.9$	V
Oscillator frequency	$f_{OSC}$	OSC; $R_{OSC} = 43 \text{ k}\Omega$ , $C_{OSC} = 680 \text{ pF}$	40	50	60	kHz
Current drain	$I_{DD1}$	$V_{DD}$ ; power saving mode			5	$\mu\text{A}$
	$I_{DD2}$	$V_{DD}$ ; $V_{DD} = 6.0 \text{ V}$ , output open, $f_{osc} = 50 \text{ kHz}$		230	460	$\mu\text{A}$
	$I_{LCD1}$	$V_{LCD}$ ; power saving mode			5	$\mu\text{A}$
	$I_{LCD2}$	$V_{LCD}$ ; $V_{LCD} = 6.0 \text{ V}$ , output open 1/2 bias, $f_{osc} = 50 \text{ kHz}$		100	200	$\mu\text{A}$
	$I_{LCD3}$	$V_{LCD}$ ; $V_{LCD} = 6.0 \text{ V}$ , output open 1/3 bias, $f_{osc} = 50 \text{ kHz}$		60	120	$\mu\text{A}$

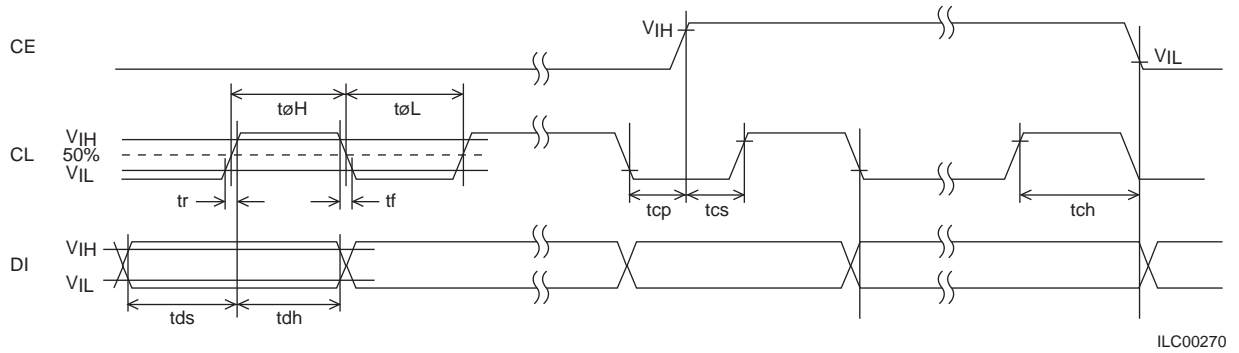
Note: \*1 Excluding the bias voltage generation divider resistors built in the  $V_{LCD1}$  and  $V_{LCD2}$ . (See Figure 1.)



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Figure 1

1. When CL is stopped at the low level



2. When CL is stopped at the high level

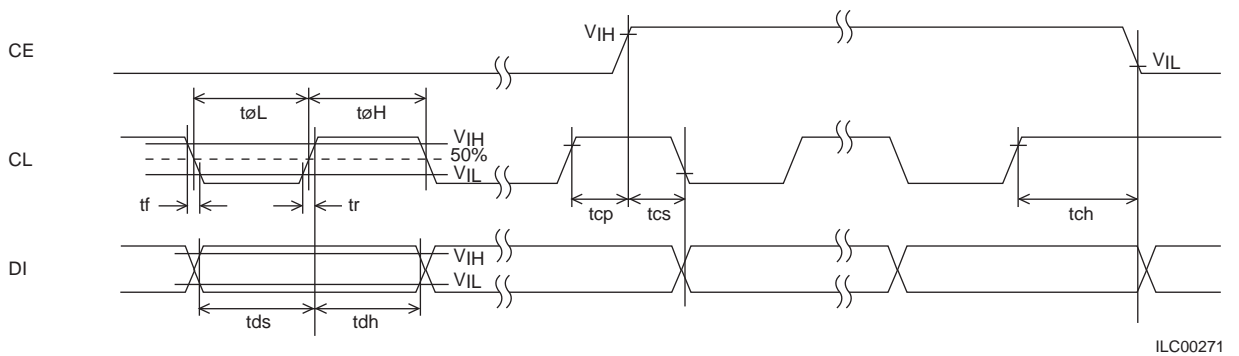
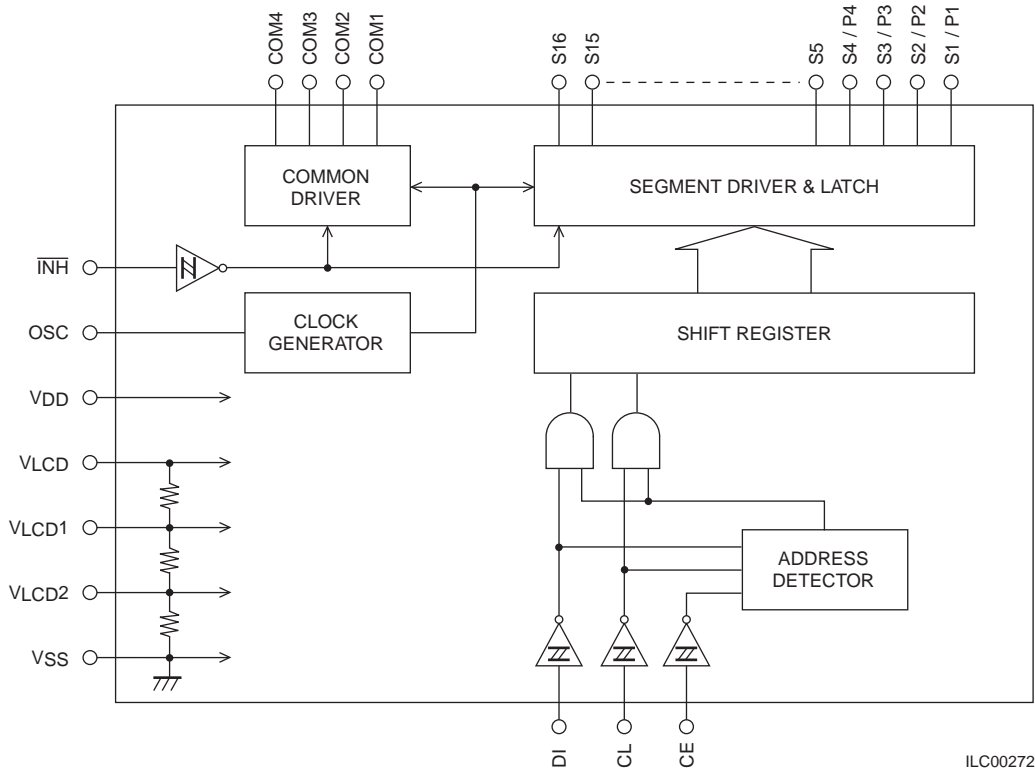


Figure 2

Block Diagram



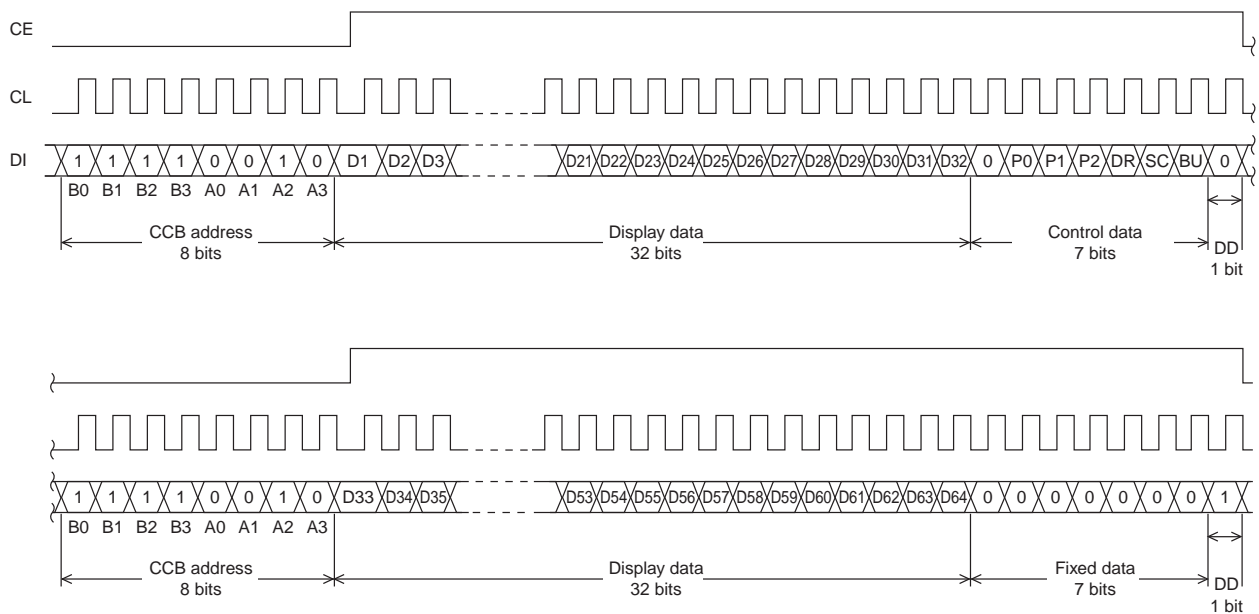
# LC75814V

## Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused						
S1/P1 to S4/P4 S5 to S16	1 to 4 5 to 16	Segment outputs for displaying the display data transferred by serial data input. The pins S1/P1 to S4/P4 can be used as general-purpose output ports when so set up by the control data.	—	O	Open						
COM1 COM2 COM3 COM4	17 to 20	Common driver outputs. The frame frequency $f_O$ is given by: $f_O = (f_{OSC}/512)$ Hz.	—	O	Open						
OSC	26	Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.	—	I/O	$V_{DD}$						
CE CL DI	28 29 30	Serial data transfer inputs. These pins are connected to the control microprocessor.	<table border="1" style="font-size: small;"> <tr><td>CE: Chip enable</td></tr> <tr><td>CL: Synchronization clock</td></tr> <tr><td>DI: Transfer data</td></tr> </table>	CE: Chip enable	CL: Synchronization clock	DI: Transfer data	<table border="1" style="font-size: small;"> <tr><td>H</td></tr> <tr><td>I</td></tr> <tr><td>—</td></tr> </table>	H	I	—	GND
CE: Chip enable											
CL: Synchronization clock											
DI: Transfer data											
H											
I											
—											
$\overline{INH}$	27	Display off control input <ul style="list-style-type: none"> <li>•<math>\overline{INH}</math> = low (<math>V_{SS}</math>): Off                             <ul style="list-style-type: none"> <li>S1/P1 to S4/P4 = Low (These pins are forcibly set to the segment output port function and fixed at the <math>V_{SS}</math> level.)</li> <li>S5 to S16 = Low (<math>V_{SS}</math>).</li> <li>COM1 to COM4 = Low (<math>V_{SS}</math>)</li> </ul> </li> <li>•<math>\overline{INH}</math> = high (<math>V_{DD}</math>): On</li> </ul> Note that serial data transfers can be performed when the display is forced off by this pin.	L	I	GND						
$V_{LCD1}$	23	Used to apply the LCD drive 2/3 bias voltage externally. This pin must be connected to $V_{LCD2}$ when 1/2 bias drive is used.	—	I	Open						
$V_{LCD2}$	24	Used to apply the LCD drive 1/3 bias voltage externally. This pin must be connected to $V_{LCD1}$ when 1/2 bias drive is used.	—	I	Open						
$V_{DD}$	21	Logic block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—						
$V_{LCD}$	22	LCD driver block power supply. Provide a voltage in the range 2.7 to 6.0 V.	—	—	—						
$V_{SS}$	25	Ground pin. Connect to ground.	—	—	—						

## Serial Data Transfer Format

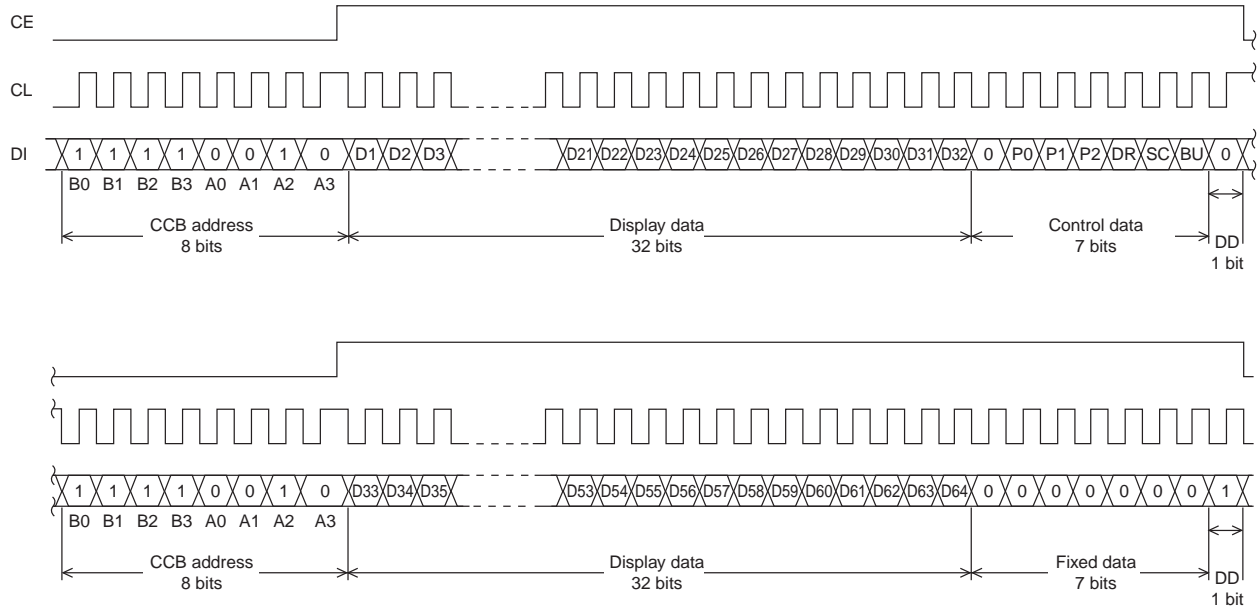
### 1. When CL is stopped at the low level



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Note: DD ... Direction data

2. When CL is stopped at the high level



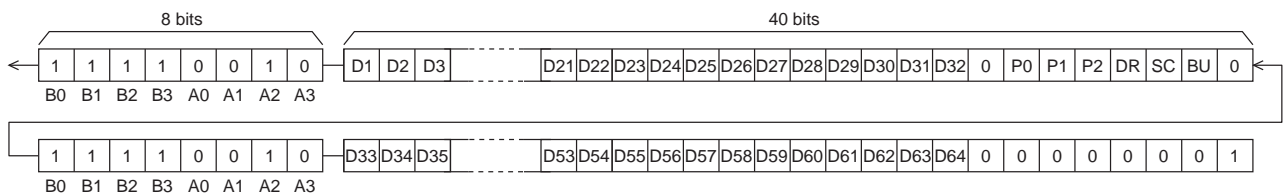
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Note: DD ... Direction data

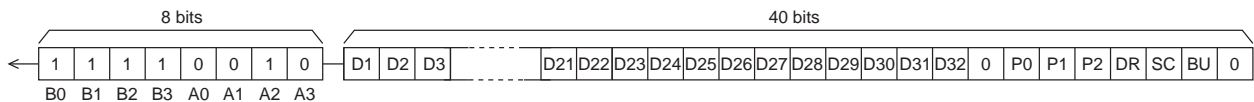
- CCB address.....4FH
- D1 to D64.....Display data
- P0 to P2 .....Segment output port/general-purpose output port switching control data
- DR .....1/2 bias drive or 1/3 bias drive switching control data
- SC.....Segments on/off control data
- BU .....Normal mode/power-saving mode control data

Serial Data Transfer Examples

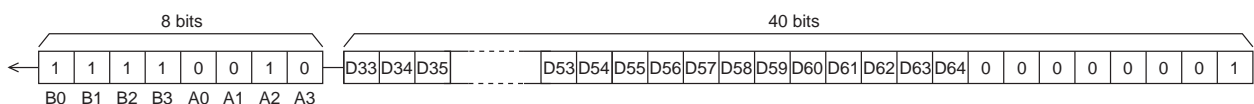
- When 33 or more segments are used, all 80 bits of the serial data must be sent.



- When fewer than 33 segments are used, only 40 bits of serial data need to be sent. However, the display data D1 to D32 and the control data must be sent.



Note: When fewer than 33 segments are used, transfers such as that shown in the figure below cannot be used.



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## Control Data Functions

1. P0 to P2: Segment output port/general-purpose output port switching control data.

These control data bits switch the S1/P1 to S4/P4 output pins between their segment output port and general-purpose output port functions.

Control data			Output pin states			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Note: Sn (n = 1 to 4): Segment output ports  
Pn (n = 1 to 4): General-purpose output ports

Also note that when the general-purpose output port function is selected, the output pins and the display data will have the correspondences listed in the tables below.

Output pin	Corresponding display data
S1/P1	D1
S2/P2	D5
S3/P3	D9
S4/P4	D13

For example, if the output pin S4/P4 has the general-purpose output port function selected, it will output a high level ( $V_{LCD}$ ) when the display data D13 is 1, and will output a low level ( $V_{SS}$ ) when D13 is 0.

2. DR: 1/2 bias drive or 1/3 bias drive switching control data

This control data bit selects either 1/2 bias drive or 1/3 bias drive.

DR	Drive type
0	1/3 bias drive
1	1/2 bias drive

3. SC: Segments on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

4. BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode (The OSC pin oscillator is stopped, and the common and segment output pins go to the $V_{SS}$ level. However, the S1/P1 to S4/P4 output pins that are set to be general-purpose output ports by the control data P0 to P2 can be used as general-purpose output ports.)

### Display Data to Segment Output Pin Correspondence

Segment output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5	D17	D18	D19	D20
S6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64

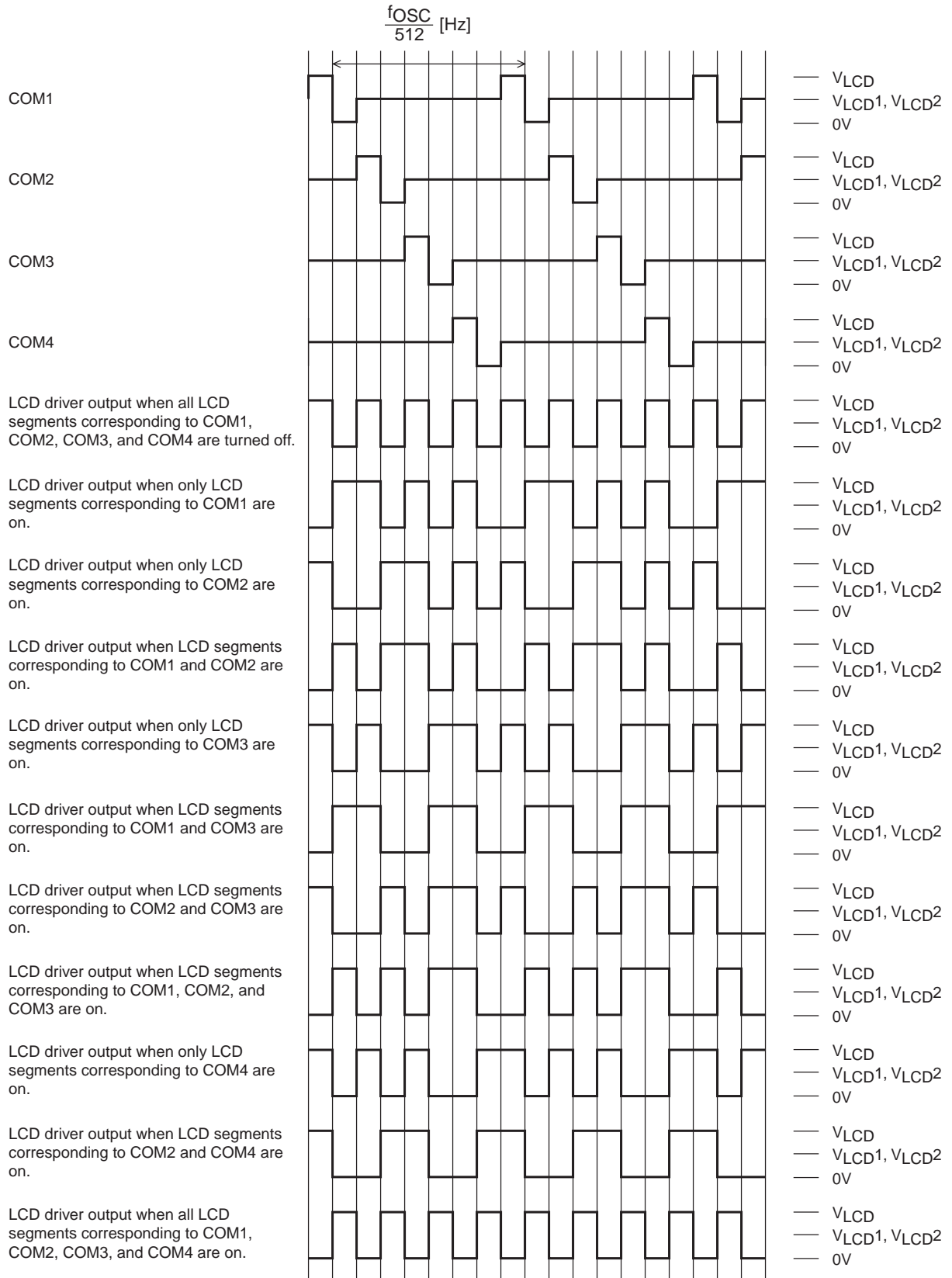
Note: This applies to the case where the S1/P1 to S4/P4 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data				Segment output pin (S11) state
D41	D42	D43	D44	
0	0	0	0	The LCD segments corresponding to COM1 to COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3 and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3 and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2 and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1 to COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1 to COM4 are on.



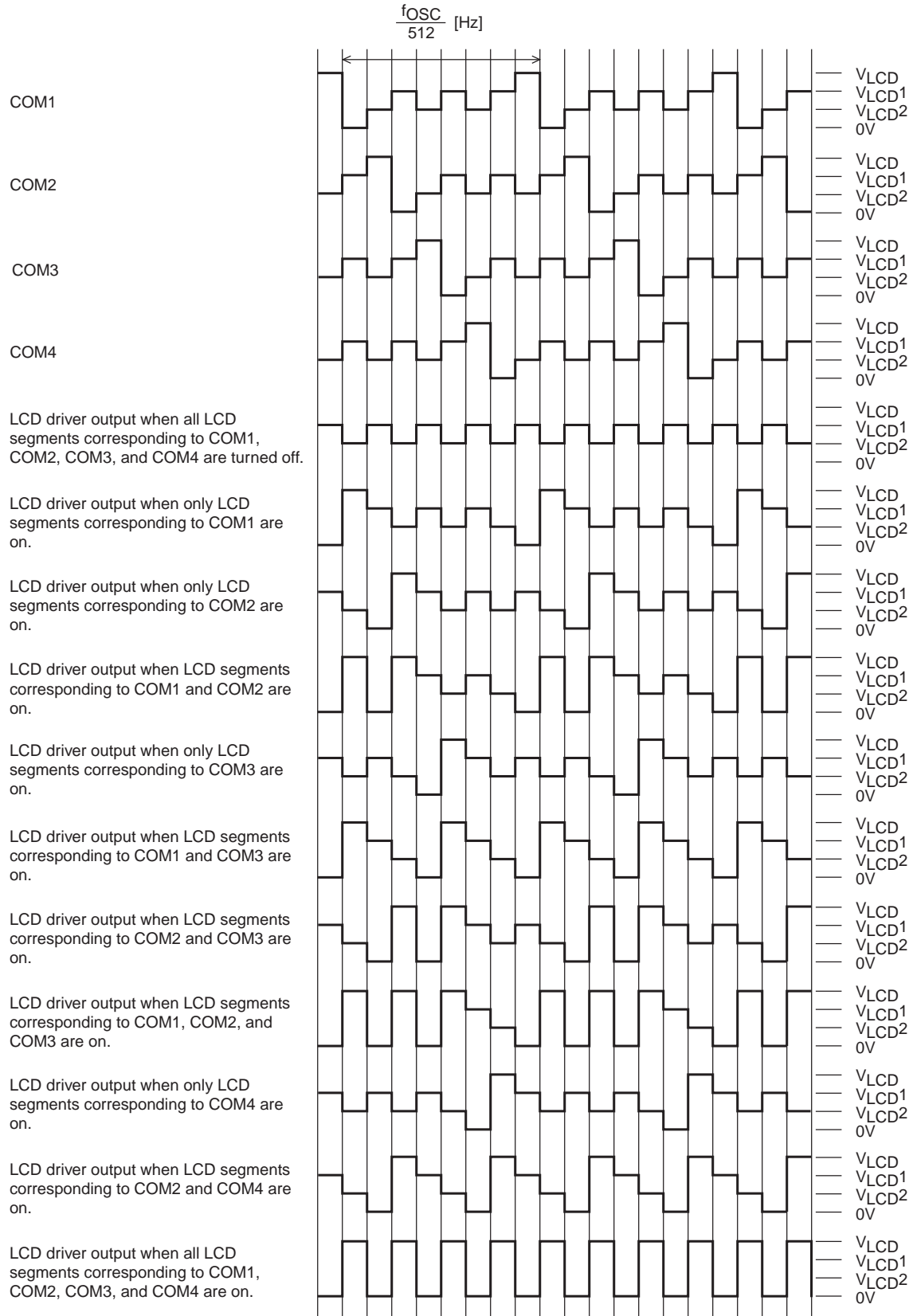
1/4 Duty, 1/2 Bias Drive Technique



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1/4 Duty, 1/2 Bias Waveforms

1/4 Duty, 1/3 Bias Drive Technique



ILC00277

1/4 Duty, 1/3 Bias Waveforms

### The $\overline{\text{INH}}$ pin and Display Control

Since the IC internal data (the display data D1 to D64 and the control data) is undefined when power is first applied, applications should set the  $\overline{\text{INH}}$  pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S4/P4, S5 to S16, and COM1 to COM4 to the  $V_{SS}$  level.) and during this period send serial data from the controller. The controller should then set the  $\overline{\text{INH}}$  pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figure 3.)

### Notes on the Power On/Off Sequences

Applications should observe the following sequence when turning the LC75814V power on and off.

- At power on: Logic block power supply ( $V_{DD}$ ) on  $\rightarrow$  LCD driver block power supply ( $V_{LCD}$ ) on
- At power off: LCD driver block power supply ( $V_{LCD}$ ) off  $\rightarrow$  Logic block power supply ( $V_{DD}$ ) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

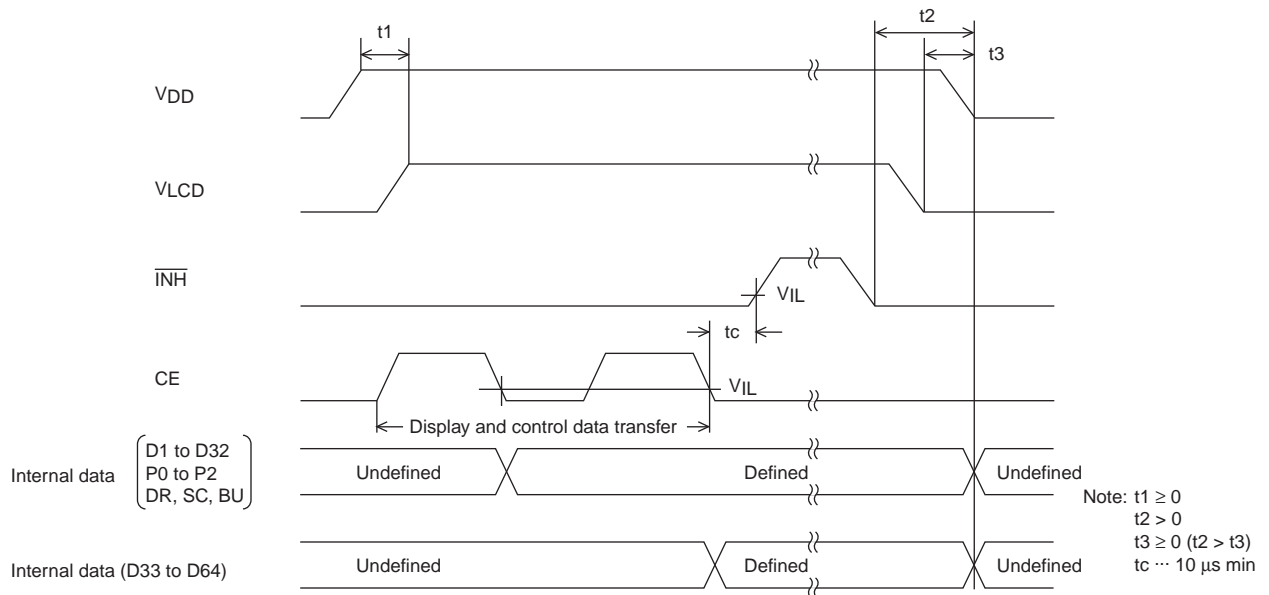


Figure 3

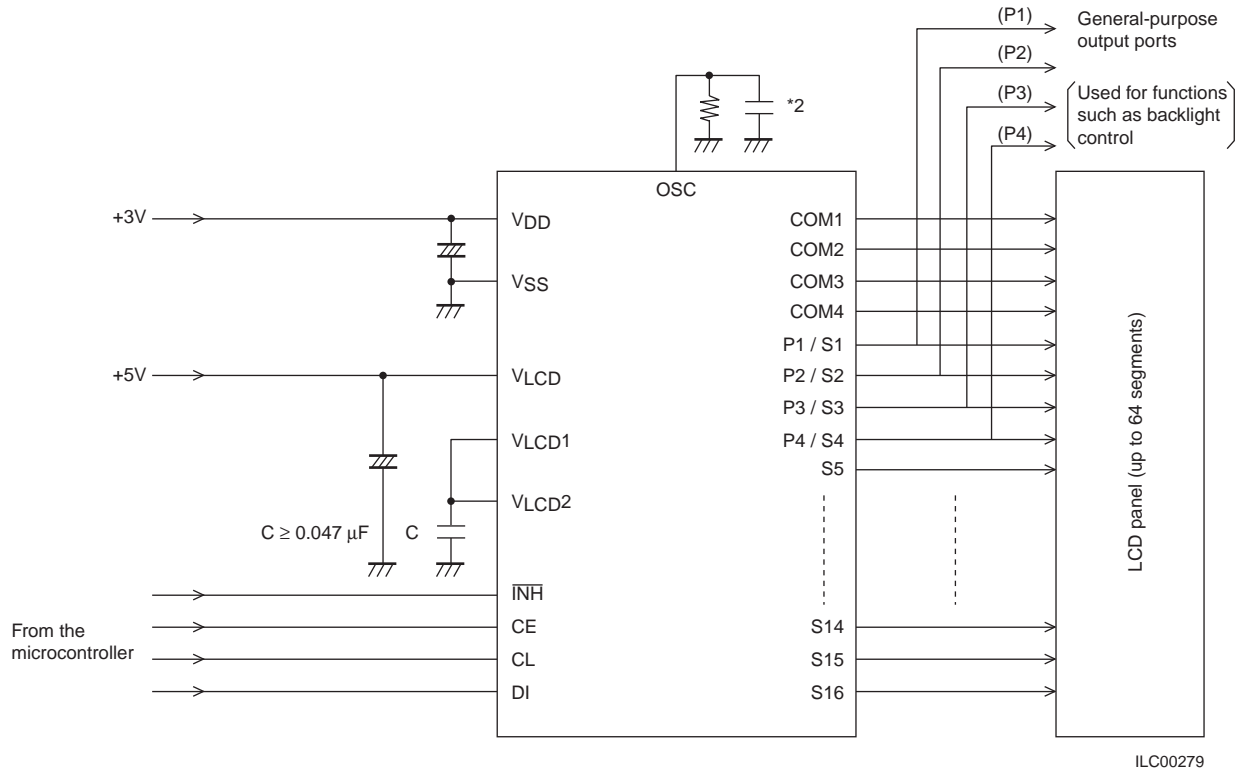
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### Notes on Controller Transfer of Display Data

Since the LC75814V accept display data (D1 to D64) divided into two separate transfer operations, we recommend that applications transfer all of the display data within a period of less than 30 ms to prevent observable degradation of display quality.

### Sample Application Circuit 1

1/2 Bias (for use with normal panels)

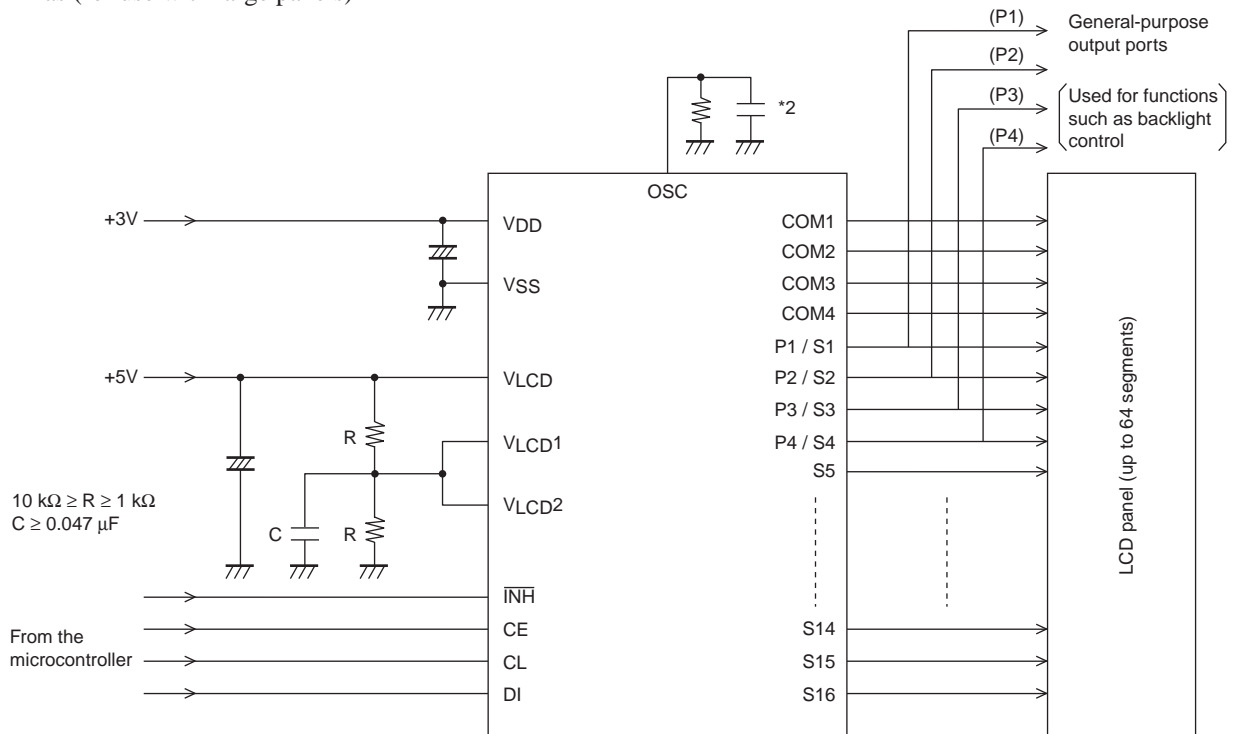


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Note: \*2 When a capacitor except the recommended external capacitance ( $C_{OSC} = 680 \text{ pF}$ ) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

### Sample Application Circuit 2

1/2 Bias (for use with large panels)

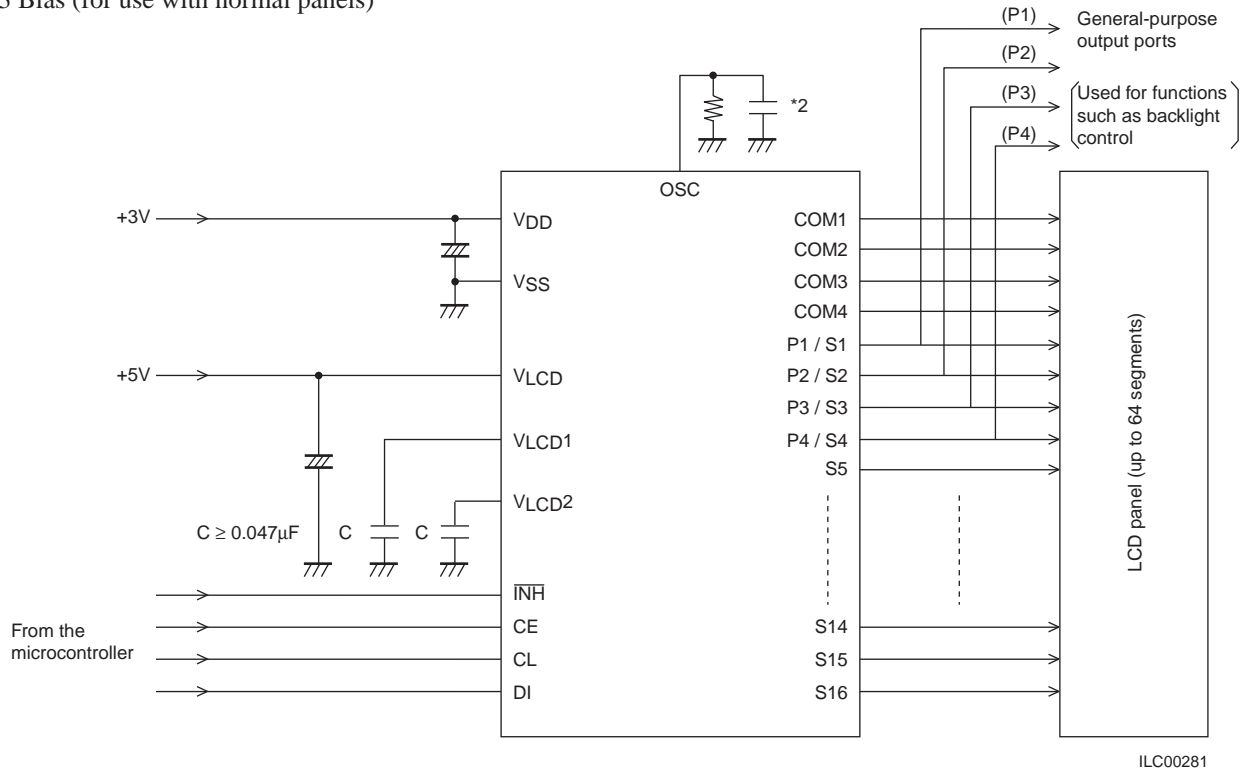


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Note: \*2 When a capacitor except the recommended external capacitance ( $C_{OSC} = 680 \text{ pF}$ ) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

### Sample Application Circuit 3

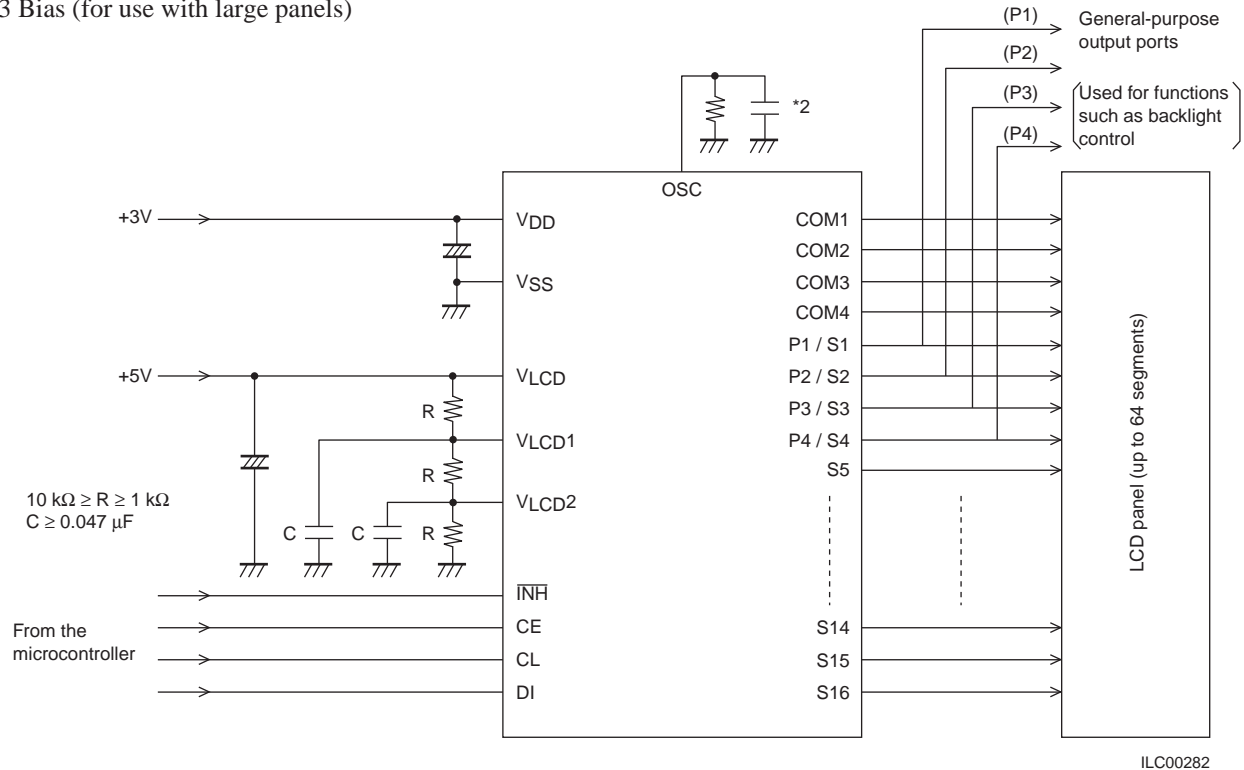
1/3 Bias (for use with normal panels)



Note: \*2 When a capacitor except the recommended external capacitance ( $C_{OSC} = 680 \text{ pF}$ ) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

### Sample Application Circuit 4

1/3 Bias (for use with large panels)



Note: \*2 When a capacitor except the recommended external capacitance ( $C_{OSC} = 680 \text{ pF}$ ) is connected the OSC pin, we recommend that applications connect the OSC pin with a capacitor in the range 220 to 2200pF.

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