

**SANYO**

No. 3318

**LB1822****3-Phase Brushless Motor Predriver  
with Digital Speed Control****Overview**

The LB1822 is a monolithic predriver IC for controlling three-phase brushless motors and has an on-chip digital speed control circuit.

The LB1822 is ideally suited for driving the motor of laser beam printers, facsimiles, plain paper copiers, and so on.

**Features**

- 30V withstand voltage and 30mA output current
- Current limiter
- Low-voltage protection circuit
- Thermal shutdown circuit
- Hall amp with hysteresis characteristic
- Start/Stop terminals
- Crystal oscillator and divider
- Digital speed control circuit
- Lock detector

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ 

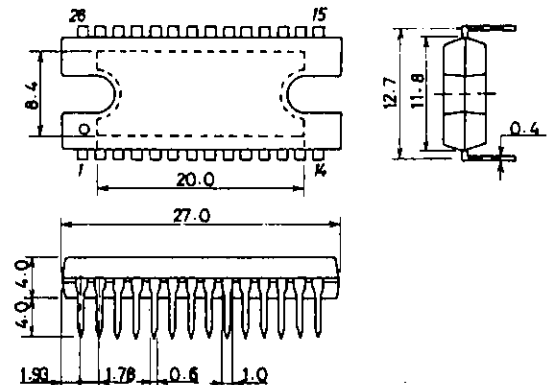
			unit
Maximum Supply Voltage 1	$V_{CC}$	30	V
Maximum Supply Voltage 2	$V_M$	30	V
Output Current	$I_O$	30	mA
Allowable Power Dissipation 1	$P_d \text{ max1}$	IC alone	3
Allowable Power Dissipation 2	$P_d \text{ max2}$	With infinite heat sink	20
Operating Temperature	$T_{opr}$	-20 to +80	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

**Allowable Operating Conditions** at  $T_a = 25^\circ\text{C}$ 

			unit
Supply Voltage 1	$V_{CC}$	9.5 to 28	V
Supply Voltage 2	$V_M$	5 to 28	V
Voltage Regulator Output Current	$I_{VH}$	0 to 20	mA
Comparator Output Current	$I_{osc}$	0 to 30	mA
Lock Detector Output Current	$I_{LD}$	0 to 20	mA

**Package Dimensions** 3147-D28HLSLSI

(unit: mm)



SANYO: DIP28HS (500 mil)

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## LB1822

Electrical Characteristics at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = V_M = 24\text{V}$

			min	typ	max	unit
Supply Current 1	$I_{CC1}$			33	50	mA
Supply Current 2	$I_{CC2}$	Stop mode		3	5	mA
Output Saturation Voltage	$V_{O\ sat1}$	$I_O = 10\text{mA}$		1.5	2.0	V
Output Leak Current	$I_{O\ leak}$				100	$\mu\text{A}$
Voltage Regulator						
Output Voltage	$V_H$	$I_{VH} = 10\text{mA}$	3.8	4.15	4.5	V
Voltage Fluctuation	$\Delta V_{H1}$	$V_{CC} = 9.5\text{ to }28\text{V}$		60	150	mV
Load Fluctuation	$\Delta V_{H2}$	$I_{VH} = 5\text{ to }20\text{V}$		60	150	mV
Temperature Coefficient				-2		mV/ $^\circ\text{C}$
Hall Amp						
Input Bias Current	$I_{HB}$			1	4	$\mu\text{A}$
Common-Mode Input Voltage	$V_{ICM}$		1.5		2.8	V
Hall Input Sensitivity			100			mVp-p
Hysteresis Width	$\Delta V_{IN}$		24	33	42	mV
Low to High Input Voltage	$V_{SLH}$		8	20	32	mV
High to Low Input Voltage	$V_{SHL}$		-25	-13	-1	mV
Oscillator						
High-Level Output Voltage	$V_{OH(CR)}$		2.9	3.2	3.5	V
Low-Level Output Voltage	$V_{OL(CR)}$		0.9	1.1	1.3	V
Oscillation Amplitude			1.8	2.1	2.4	V
Oscillation Frequency	$f$	$R = 30\text{k}\Omega, C = 1500\text{pF}$		18.5		kHz
Temperature Coefficient	$\Delta f$			0.1		%/ $^\circ\text{C}$
Comparator						
Output Voltage	$V_{OSC}$	$I_{osc} = 20\text{mA}$			1.5	V
Current Limiter						
Limiter 1	$V_{Rf1}$		0.42	0.5	0.6	V
Limiter 2	$V_{Rf2}$		0.4	0.44	0.48	V
Thermal Shutdown Temperature						
Hysteresis Width	$\Delta TSD$	Design goals	150	180		$^\circ\text{C}$
Low-Voltage Protection Voltage	$V_{LVSD}$		7.5	8.1	8.7	V
Hysteresis Width	$\Delta V_{LVSD}$		0.45	0.6	0.75	V
FG Amp						
Input Offset Voltage	$V_{IO(FG)}$		-10		10	mV
Input Bias Current	$I_{B(FG)}$		-1		1	$\mu\text{A}$
High-Level Output Voltage	$V_{OH(FG)}$	$I_{FG} = -2\text{ mA}$	5.6	6.2	6.8	V
Low-Level Output Voltage	$V_{OL(FG)}$	$I_{FG} = 2\text{ mA}$		1	1.5	V
FG Input Sensitivity		$10 \times \text{Gain}$	5			mV
Schmitt Width at Next Stage				16		mV
Operating Frequency Range					5	kHz
Open-Loop Voltage Gain			60			dB
Speed Discriminator						
High-Level Output Voltage	$V_{OH(D)}$			4.7		V
Low-Level Output Voltage	$V_{OL(D)}$			0.3		V
Maximum Clock Frequency		$T_j = 100^\circ\text{C}$	1.05			MHz
Count Pulses			2044	2046	2048	

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# LB1822

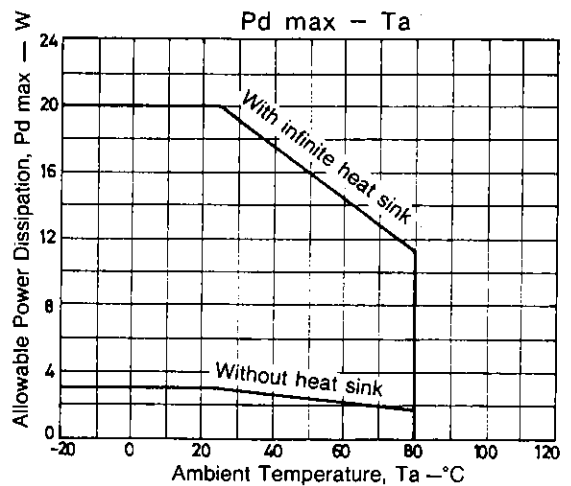
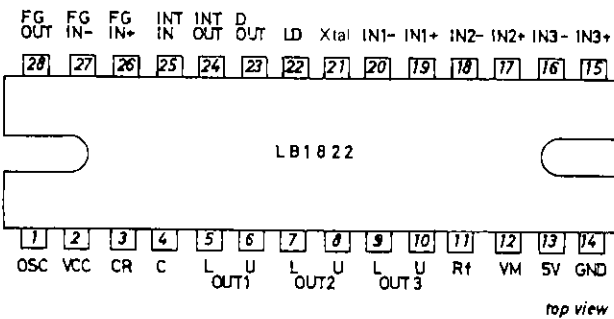
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			min	typ	max	unit
<b>Integrator</b>						
Input Offset Voltage	$V_{IO(INT)}$		-10		10	mV
Input Bias Current	$I_{B(INT)}$		-0.4		0.4	$\mu A$
High-Level Output Voltage	$V_{OH(INT)}$		3.7	4.3	4.9	V
Low-Level Output Voltage	$V_{OL(INT)}$			0.8	1.2	V
Open-Loop Gain			60			dB
Gain-Bandwidth Product				1.6		MHz
Reference Voltage			-5%	$V_5/2$	5%	V
5V Supply	$V_5$		4.6	5	5.4	V
<b>Lock Detection</b>						
Low-Level Output Voltage	$V_{OL(LD)}$	$I_{LD} = 10mA$			0.5	V
Locking Range				$\pm 3.125$		%
<b>Start/Stop</b>						
Operating Voltage			0.4	0.5	0.6	V
<b>Crystal Oscillator</b>						
Precision of Oscillating Frequency		Referenced to indicated frequency	-500		500	ppm
Temperature Coefficient				-3		ppm/ $^{\circ}C$
Drift in Rotation Speed				$\pm 0.01$		%

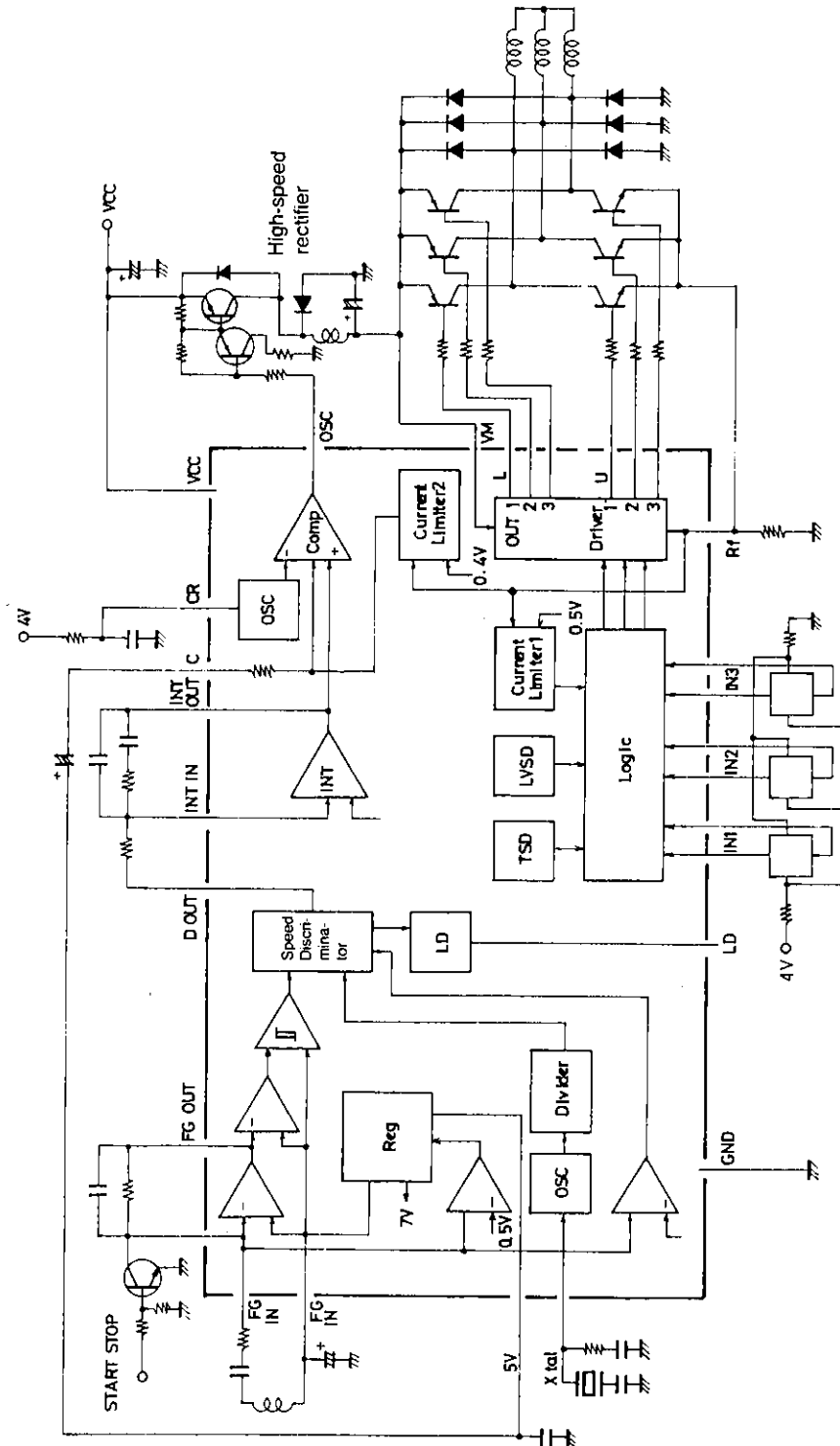
### Truth Table

Item	Source Sink	Input		
		IN1	IN2	IN3
1	OUT 3 → OUT 2	H	H	L
2	OUT 3 → OUT 1	H	L	L
3	OUT 2 → OUT 3	L	L	H
4	OUT 1 → OUT 2	L	H	L
5	OUT 2 → OUT 1	H	L	H
6	OUT 1 → OUT 3	L	H	H

### Pin Assignment



Block Diagram



## Description of Terminal Functions

Pin Name	Pin No.	Description
IN <sup>+</sup> 1, IN <sup>-</sup> 1	19, 20	OUT1: Hall element input terminals for Phase 1. "H" logic is the state when IN <sup>+</sup> > IN <sup>-</sup> .
IN <sup>+</sup> 2, IN <sup>-</sup> 2	17, 18	OUT2: Hall element input terminals for Phase 2. "H" logic is the state when IN <sup>+</sup> > IN <sup>-</sup> .
IN <sup>+</sup> 3, IN <sup>-</sup> 3	15, 16	OUT3: Hall element input terminals for Phase 3. "H" logic is the state when IN <sup>+</sup> > IN <sup>-</sup> .
OUT1	5, 6	Output terminals for Phase 1. U ... source
OUT2	7, 8	Output terminals for Phase 2. L ... sink
OUT3	9, 10	Output terminals for Phase 3.
Vcc	2	Power supply for everything, except outputs.
VM	12	Power supply for outputs.
R <sub>f</sub>	11	Output current detection terminal. An R <sub>f</sub> is connected across this terminal and GND, and the output current is detected as voltage.
GND	14	Ground for everything, except outputs. The minimum potential for output transistors is the voltage at R <sub>f</sub> .
CR	3	Sets the oscillating frequency of the switching regulator.
OSC	1	Outputs duty-controlled pulses. Open-collector output.
INT. OUT	24	Integrator output terminal (speed control terminal). Varies the switching regulator output voltage.
INT. IN	25	Integrator input terminal.
D. OUT	23	Speed discriminator output terminal. Goes LOW when the specified speed is exceeded.
C	4	Suppresses ripples in the motor current during operation of current limiter 2.
LD	22	Lock detection terminal. Goes LOW when the motor rotation speed is within the locking range.
FG, IN <sup>-</sup>	27	FG pulse input (Start/Stop control) terminal.
FG, IN <sup>+</sup>	26	FG pulse input (4V supply) terminal.
FGOUT	28	FG amp output terminal.
X'tal	21	Crystal oscillator terminal to which a crystal resonator is connected.
5V	13	5V supply terminal.

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