Application Note 10.13

Migrating from the LAN83C180 10/100 PHY to the LAN83C185 10/100 PHY

APPLICATION NOTE

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

1 General Description

This application note discusses how to migrate from an existing design using the SMSC LAN83C180 PHY to SMSC's next generation LAN83C185 PHY. A general overview is provided which includes such topics as power connections, magnetics interface, proper signal termination, clock circuit implementation and pinout differences.

1.1 Overview

This application note provides a summary of the recommendations and requirements for migrating from a SMSC LAN83C180 10/100 PHY design to a new design incorporating the LAN83C185 10/100 PHY. This document references additional documentation and schematics (see section 1.2 "Reference Documents"). This document also uses the original "LAN83C180 10/100 Adapter Reference Design" as a reference for all LAN83C180 vs. LAN83C185 discussions.

Please note that since each customer's LAN83C180 design may differ, the contents below are offered as a general guideline. Specific customer requirements may force the guidelines discussed here to be adjusted or ignored.

1.2 Reference Documents

The following documents are referred to in this application note:

- SMSC LAN83C185 datasheet
- SMSC LAN83C185 MII Customer PCB (Assy. 6316 Rev. A2) Schematic
- SMSC LAN83C180 10/100 PHY Adapter Reference Design (Assy. 6096 Rev. A1) Schematic
- SMSC Application Note AN 8.13 - "Suggested Magnetics"
- SMSC Application Note AN 10.7 - "Parallel Crystal Circuit Input Voltage Control"

Please note that it is important to always refer to the SMSC LAN83C185 datasheet and the LAN83C185 MII Customer Reference Design Schematic for complete and current information regarding LAN83C185 designs. Additionally, the circuit examples shown in this document are for illustrative purposes only. Please reference the LAN83C185 MII Customer Reference Design Schematic when implementing actual circuits in your design.

Please visit SMSC's website at http://www.smsc.com/ for the latest updated documentation.

2 Summary of Differences Between the LAN83C180 and LAN83C185

The areas listed below briefly outline areas of change that a designer needs to address when transitioning from the LAN83C180 to LAN83C185 designs. For details, please refer to the corresponding sections in this application note.

Table 2.1 – Design Transitions from the LAN83C180 to LAN83C185

SECTION	DESCRIPTION	PAGE (S)
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3 Power Requirements

The LAN83C185 requires a +3.3V power source, which may be obtained from any existing on-board +3.3V source, or, if none is available, by incorporating an external regulator such as the Linear Technologies LT1086 +5V-input to +3.3V-output fixed-voltage regulator - into the LAN83C185 design.

The +3.3V regulator output is supplied to the LAN83C185 core via the pins listed in Table 3.1 below:

Table 3.1 – LAN83C185 Power Pins

SIGNAL NAME	LAN83C185 PIN NO'S.
VDD	8, 18, 43
AVDD	53, 57, 61, 63
VREG	13

It is recommended that all VDD, AVDD, and VREG signals on the LAN83C185 be supplied +3.3V from the board's power plane via three ferrite beads (one per signal group – see Figure 3.1 below).

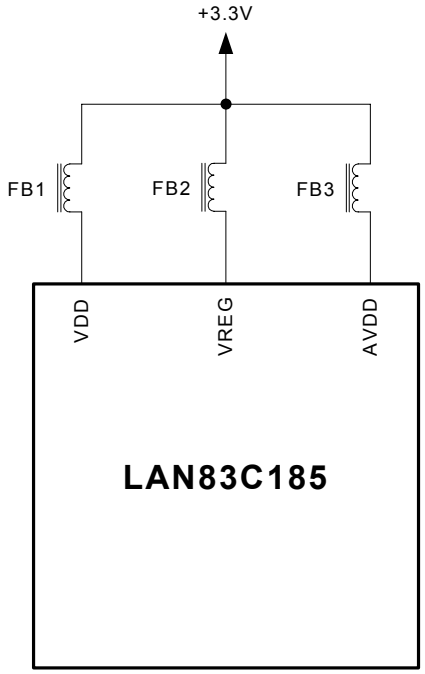


Figure 3.1 - Power Pin Connections - LAN83C185 to +3.3V

4 Cable Interface

The requirements for the cable interface, including the magnetics and RJ45 connector interfaces, are outlined in the sections below.

4.1 Magnetics

The LAN83C185 Phy Customer Reference Design uses the Bel S558-5999-46 magnetics module, which replaces the magnetics module originally specified in the LAN83C180 Customer Reference design. Please refer to SMSC Application Note 8.13 - "Suggested Magnetics" for a listing of currently approved magnetics, and to the LAN83C185 MII Customer Reference Board (Assy. 6316) schematic for details.

4.2 Connector (RJ45) Interface

All connections between the RJ45 connector and magnetics module for the LAN83C185 remain identical to LAN83C180.

4.3 Transmit & Receive Terminations

4.3.1 Transmit Terminations

The LAN83C185 transmit signals (TXP, TXN) should be pulled to +3.3V supplied from the board's power plane via a ferrite bead and termination resistors R_{Term} (see Figure 4.1 below). Power is supplied to the transmitter via the 10-Ohm resistor and the transformer center tap.

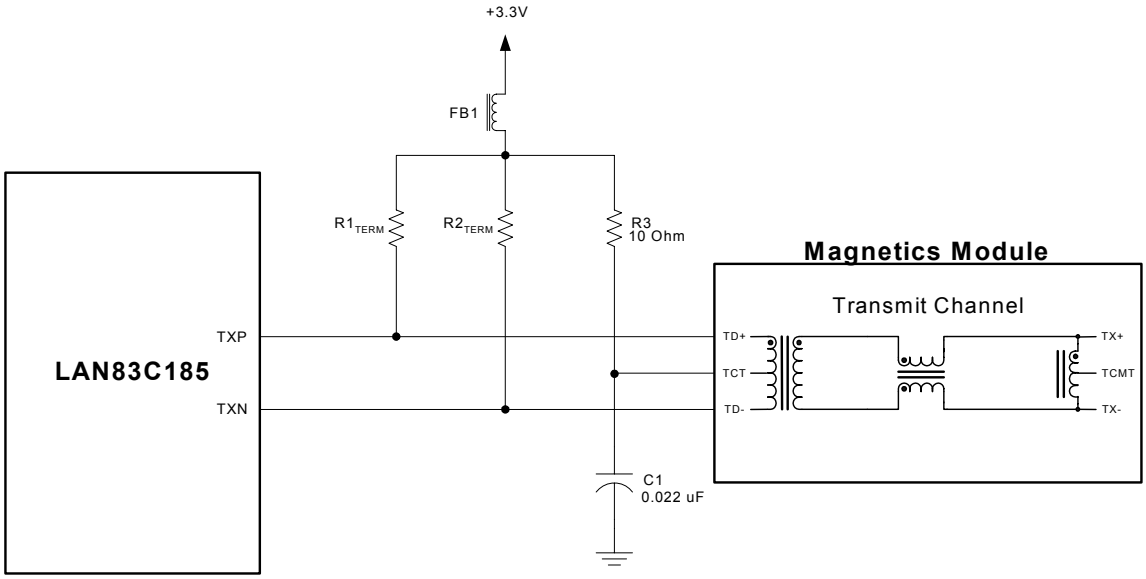


Figure 4.1 - Tx to Magnetics Interface

4.3.2 Receive Terminations

Each of the LAN83C185 receive signals (RXP, RXN) should be AC-coupled to the magnetics module's receive interface via a capacitor. Additionally, RXP and RXN signals should be terminated through a resistor via a capacitor connected to ground (see Figure 4.2 below). Please refer to the LAN83C185 Customer Reference Board schematic for recommended values.

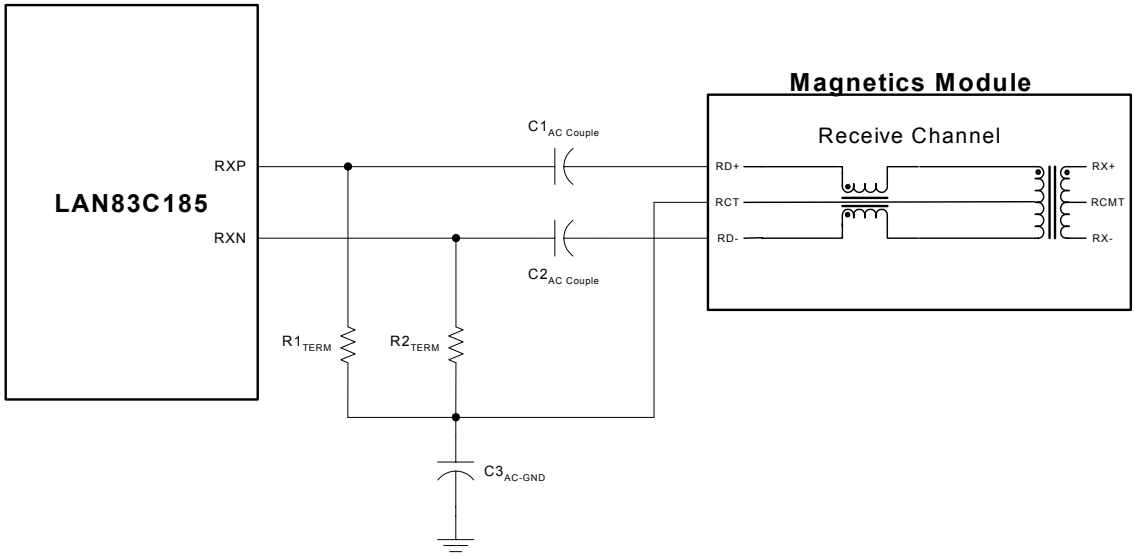


Figure 4.2 - Rx to Magnetics Interface

5 Clock Circuit

The LAN83C185 can accept either a 25MHz crystal or 25 MHz clock oscillator input. The LAN83C185 shares the 25MHz clock oscillator input (CLKIN) with the crystal input (XTAL1) on pin 23. This differs from the LAN83C180, which uses a dedicated clock oscillator pin (REFCLK).

It is recommended that a crystal utilizing matching parallel load capacitors be used for the LAN83C185 crystal input/output signals (XTAL1, XTAL2). Please refer to the crystal device datasheet for recommended capacitor values.

Additionally, SMSC recommends a series resistor for the crystal circuit. Further details are provided in SMSC Application Note 10.7 - "Parallel Crystal Circuit Input Voltage Control" and in the LAN83C185 MII Customer Reference Board (Assy. 6316) schematic.

6 LED's

The LAN83C185 provides four LED outputs signals, which share pins with the PHY address signals, as described in the PHY address section below: These signals are:

- Speed LED (SPEED100)
- Link LED (LINKON)
- Activity LED (ACTIVITY)
- Full-Duplex LED (FDUPLEX)

The LAN83C185 **does not include** the collision LED signal (COLST) found on the LAN83C180.

Please note: LED polarity is dependent on the PHY Address strapping. Please refer to the LAN83C185 datasheet for proper operation.

7 General Considerations

The topics described in the following sub-sections below require additional attention by the systems designer when changing from the LAN83C180 PHY to the LAN83C185 PHY.

7.1 Pinout Differences

The LAN83C180 and the LAN83C185 are **not** pin compatible. Always refer to the LAN83C185 datasheet and LAN83C185 Customer Reference Board schematic when implementing a design using the LAN83C185.

7.1.1 PHY Address

The LAN83C185 has five PHY address signals (PHYAD0:4). The PHY address signals on the LAN83C185 are multiplexed with other signals (please refer to Table 7.1 below). The LAN83C180 provided these signals on dedicated pins.

Table 7.1 - LAN83C185 PHY Address Pins

SIGNAL NAME	LAN83C185 PIN NO'S.
SPEED100 / PHYAD0	16
LINKON / PHYAD1	17
ACTIVITY / PHYAD2	19
FDUPLEX / PHYAD3	20
GPO1 / PHYAD4	2

Please refer to the LAN83C185 datasheet, "LED Description" section for proper PHY address/LED implementation.

7.1.2 MII Interface

The MII interface functionality remains the same for both the LAN83C180 and the LAN83C185 – note that the pin-outs are different. Please refer to the LAN83C185 datasheet for the proper pin numbers and definitions.

The LAN83C185 incorporates series resistors between the LAN83C185 outputs and the MII interface inputs. These signals are listed in Table 7.2 below.

Table 7.2 - LAN83C185 MII Series Terminations

SIGNAL NAME	LAN83C185 PIN NO'S.
MDIO	26
RXD0:3	32, 31, 30, 29
RX_DV	33
RX_CLK	34
RX_ER	35
TX_CLK	38
COL	47
CRS	48

Additionally, the MDIO signal (pin 26 on the LAN83C185) should be pulled to +5V via a 1.5K-Ohms resistor.

7.1.3 RBIAS

The LAN83C180 incorporates two (2) RBIAS resistors on signals TXREF100 and TXREF10 (Pins 33, 34). The LAN83C185 combines these onto one RBIAS signal - EXRES1 (Pin 59). The RBIAS resistor value for the LAN83C185 is 12.4K-Ohm.

7.1.4 Mode

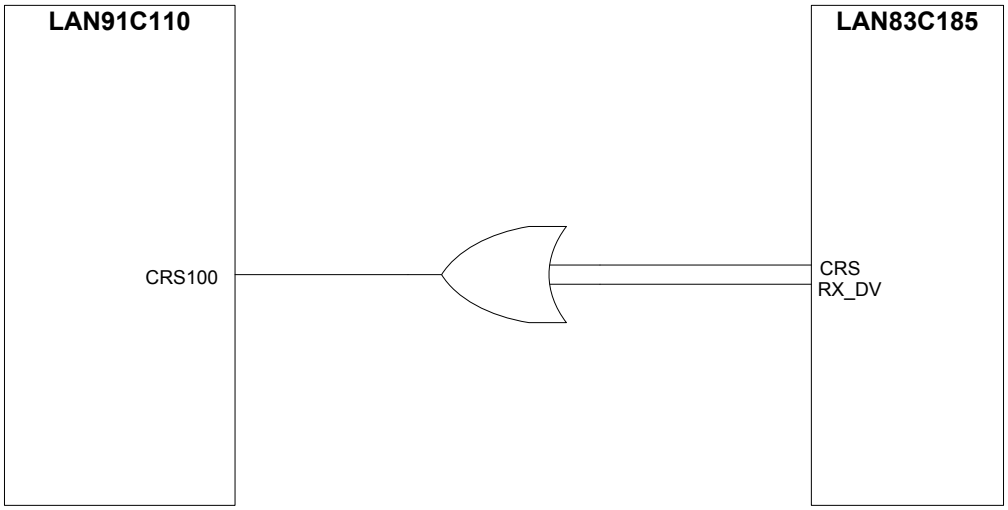
The Mode pins control the auto-negotiation, 10 and 100 Mbps data rates, and full-/half-duplex operation of the LAN83C185 PHY.

The LAN83C180 utilizes two (2) pins - RPTR (Pin 21) and ANEN (Pin 22) which are analogous to the LAN83C185's MODE pins (Pins 4, 5, and 6).

Please refer to the LAN83C185 datasheet, "Mode Bus" paragraph, in the "Configuration Signals" section for proper Mode bus operation.

8 Application Specific Notes

When designing the LAN83C185 with the SMSC LAN91C110 device, an extra single OR-GATE is required. The OR-GATE should be wired with CRS and RX_DV signals (from the LAN83C185) to the inputs of the OR-GATE. The output of the OR-GATE should be wired to the CRS100 pin of the LAN91C110.



9 Conclusion

Following the guidelines in this application note will help to ensure a proper design-in when migrating from the LAN83C180 to the LAN83C185

Note that this application note serves only as a general set of guidelines that should be followed when using an SMSC LAN83C185 chip. Specific customer requirements may both create new guidelines, which must be followed, and/or force specific rules dictated here to be broken.