

Document Title

1Mx16 bit Uni-Transistor Random Access Memory

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	October 6, 2003	Preliminary

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K1S1616B1A

1M x 16 bit Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 1M x16 bit
- Power Supply Voltage: 1.7V~2.1V
- Three State Outputs
- Compatible with Low Power SRAM
- Dual Chip selection support
- Package Type: 48-FBGA-6.00x7.00

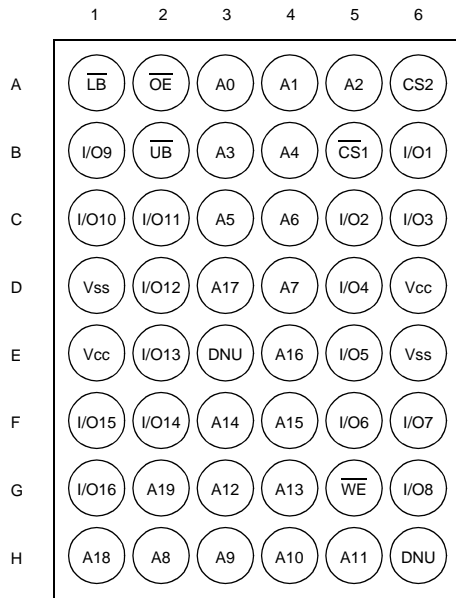
GENERAL DESCRIPTION

The K1S1616B1A is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports Industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports dual chip selection for user interface.

PRODUCT FAMILY

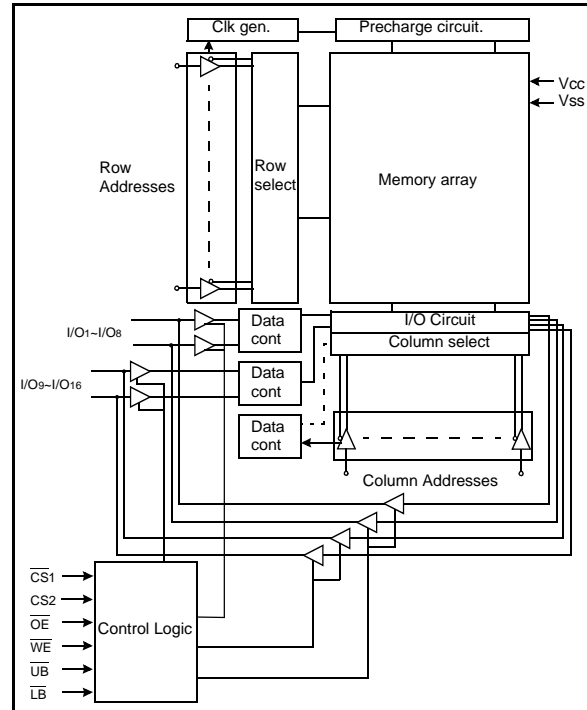
Product Family	Operating Temp.	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max.)	Operating (I _{CC2} , Max.)	
K1S1616B1A-I	Industrial(-40~85°C)	1.7V~2.1V	70/85ns	80μA	25mA	48-FBGA-6.00x7.00

PIN DESCRIPTION



48-FBGA: Top View(Ball Down)

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs	Vcc	Power
\overline{OE}	Output Enable Input	Vss	Ground
\overline{WE}	Write Enable Input	\overline{UB}	Upper Byte(I/O ₉₋₁₆)
A ₀ -A ₁₉	Address Inputs	\overline{LB}	Lower Byte(I/O ₁₋₈)
I/O ₁ -I/O ₁₆	Data Inputs/Outputs	DNU	Do Not Use ¹⁾

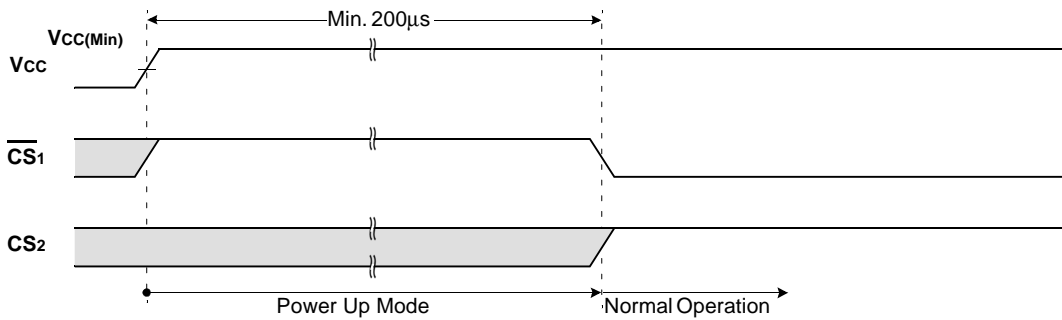
1) Reserved for future use.

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POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power ($V_{cc \text{ min.}} = 1.7V$) for a minimum $200\mu s$ with $\overline{CS1} = \text{high}$ or $CS2 = \text{low}$.

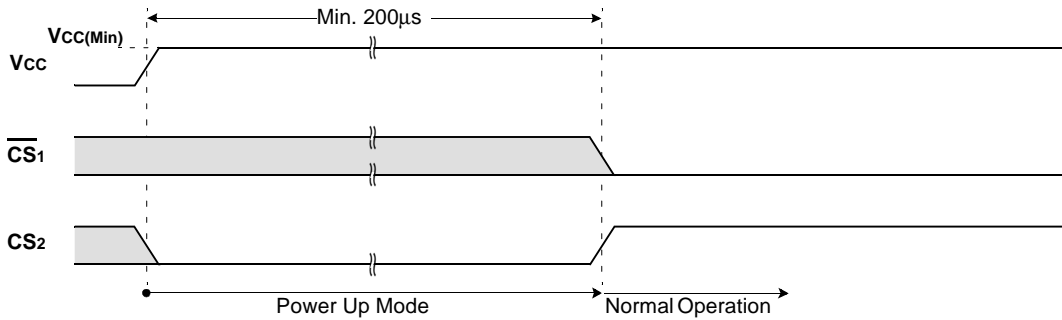
TIMING WAVEFORM OF POWER UP(1) ($\overline{CS1}$ controlled)



POWER UP(1)

1. After V_{cc} reaches $V_{cc(Min.)}$, wait $200\mu s$ with $\overline{CS1}$ high. Then the device gets into the normal operation.

TIMING WAVEFORM OF POWER UP(2) ($CS2$ controlled)



POWER UP(2)

1. After V_{cc} reaches $V_{cc(Min.)}$, wait $200\mu s$ with $CS2$ low. Then the device gets into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{CS1}$	$CS2$	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.2 to 2.5V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K1S1616B1A-FI70	48-FBGA-6.00x7.00, 70ns
K1S1616B1A-FI85	48-FBGA-6.00x7.00, 85ns
K1S1616B1A-BI70 ¹⁾	48-FBGA-6.00x7.00, 70ns
K1S1616B1A-BI85 ¹⁾	48-FBGA-6.00x7.00, 85ns

1. Lead Free Product

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	1.7	1.8/2.0	2.1	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	1.4	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

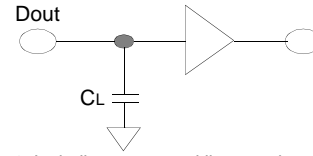
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS1} \leq 0.2V$, $\overline{LB} \leq 0.2V$ or/and $\overline{UB} \leq 0.2V$, $CS2 \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	5	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS1}=V_{IL}$, $CS2=V_{IH}$ $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	-	25	mA
Output low voltage	V _{OL}	I _{OL} = 0.1mA	-	-	0.2	V
Output high voltage	V _{OH}	I _{OH} = -0.1mA	1.4	-	-	V
Standby Current(CMOS)	I _{SB1}	Other inputs=0~V _{CC} 1) $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ ($\overline{CS1}$ controlled) or 2) $0V \leq CS2 \leq 0.2V$ ($CS2$ controlled)	-	-	80	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to $V_{CC}-0.2V$
 Input rising and falling time: 5ns
 Input and output reference voltage: $0.5 \times V_{CC}$
 Output load (See right): $C_L=50pF$



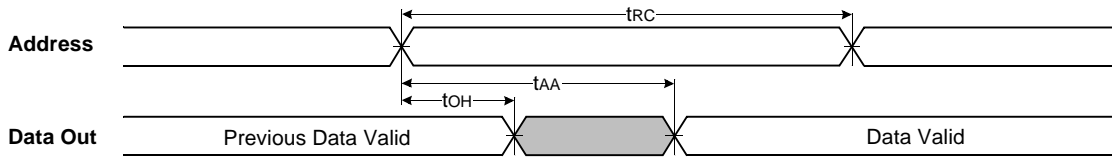
AC CHARACTERISTICS ($V_{CC}=1.7\sim 2.1V$, $T_A=-40$ to $85^\circ C$)

Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	tRC	70	-	85	-	ns
	Address Access Time	tAA	-	70	-	85	ns
	Chip Select to Output	tCO	-	70	-	85	ns
	Output Enable to Valid Output	tOE	-	35	-	40	ns
	\overline{UB} , \overline{LB} Access Time	tBA	-	70	-	85	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	\overline{UB} , \overline{LB} Enable to Low-Z Output	tBLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	25	0	25	ns
	\overline{UB} , \overline{LB} Disable to High-Z Output	tBHZ	0	25	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	25	0	25	ns
Output Hold from Address Change	tOH	5	-	5	-	ns	
Write	Write Cycle Time	tWC	70	-	85	-	ns
	Chip Select to End of Write	tCW	60	-	70	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	60	-	70	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	tBW	60	-	70	-	ns
	Write Pulse Width	tWP	55 ¹⁾	-	60 ¹⁾	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	25	0	25	ns
	Data to Write Time Overlap	tDW	30	-	35	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	5	-	5	-	ns	

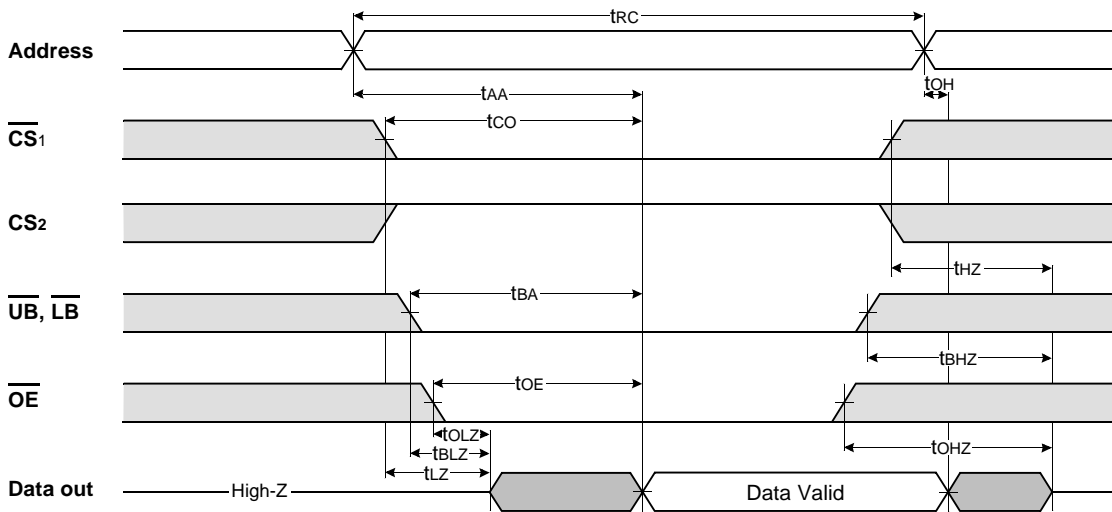
1. tWP(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



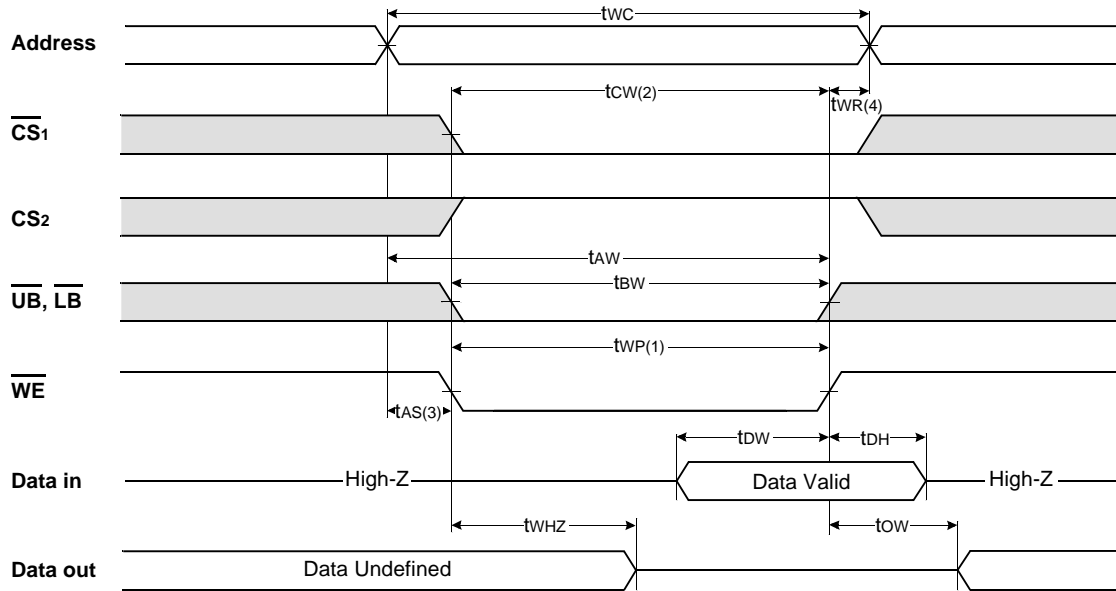
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



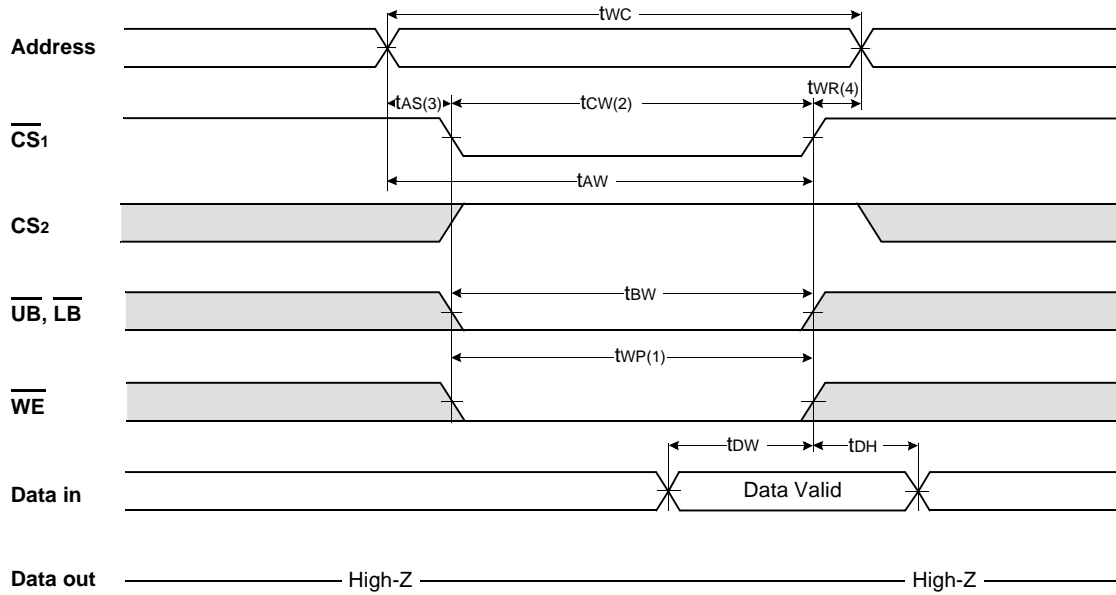
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4 μ s, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4 μ s.

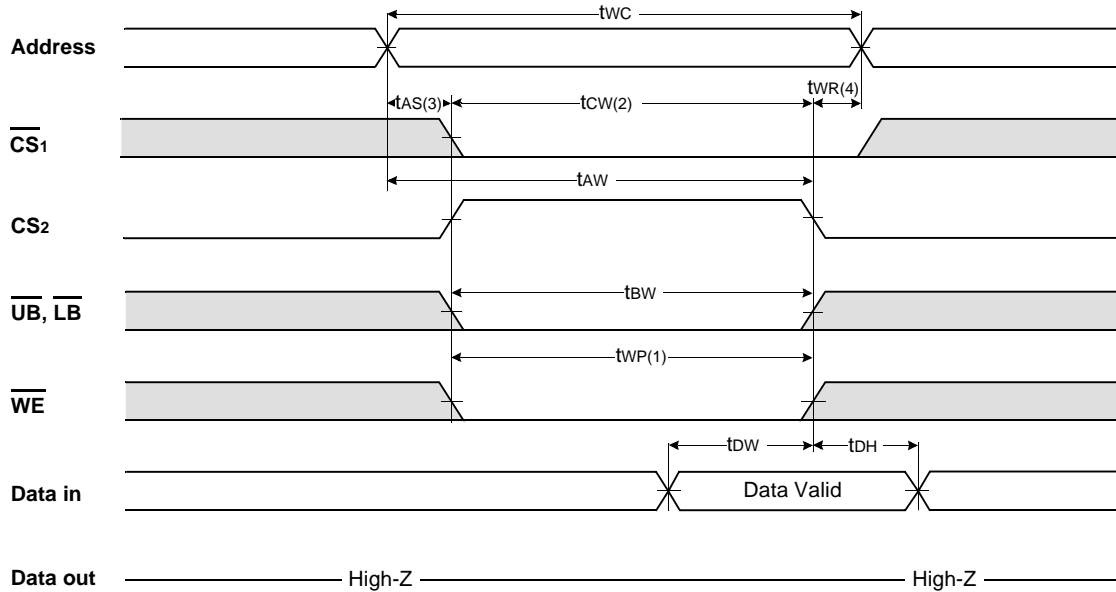
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



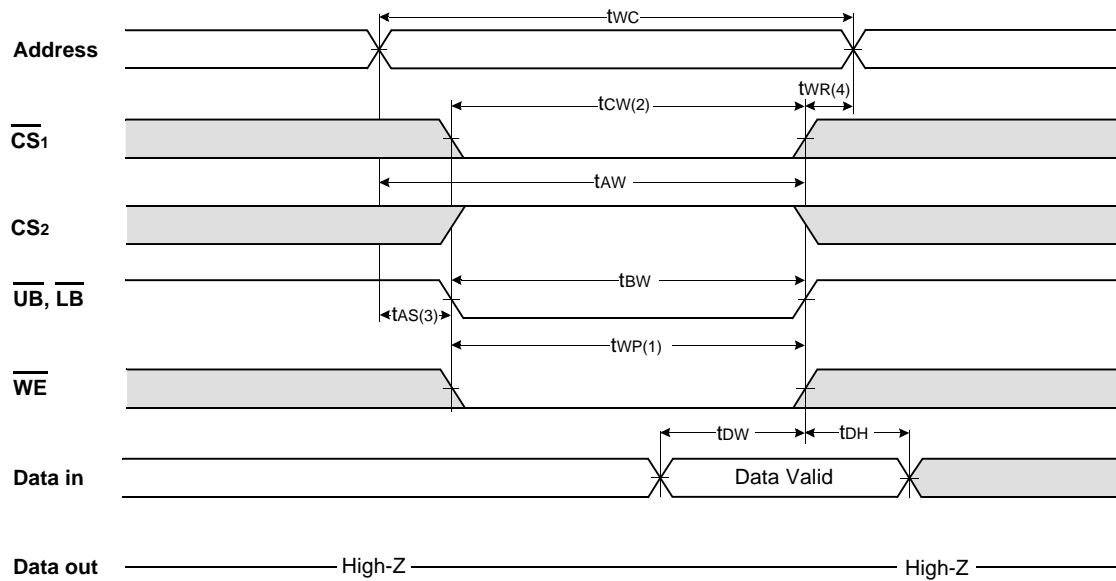
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) (\overline{UB} , \overline{LB} Controlled)



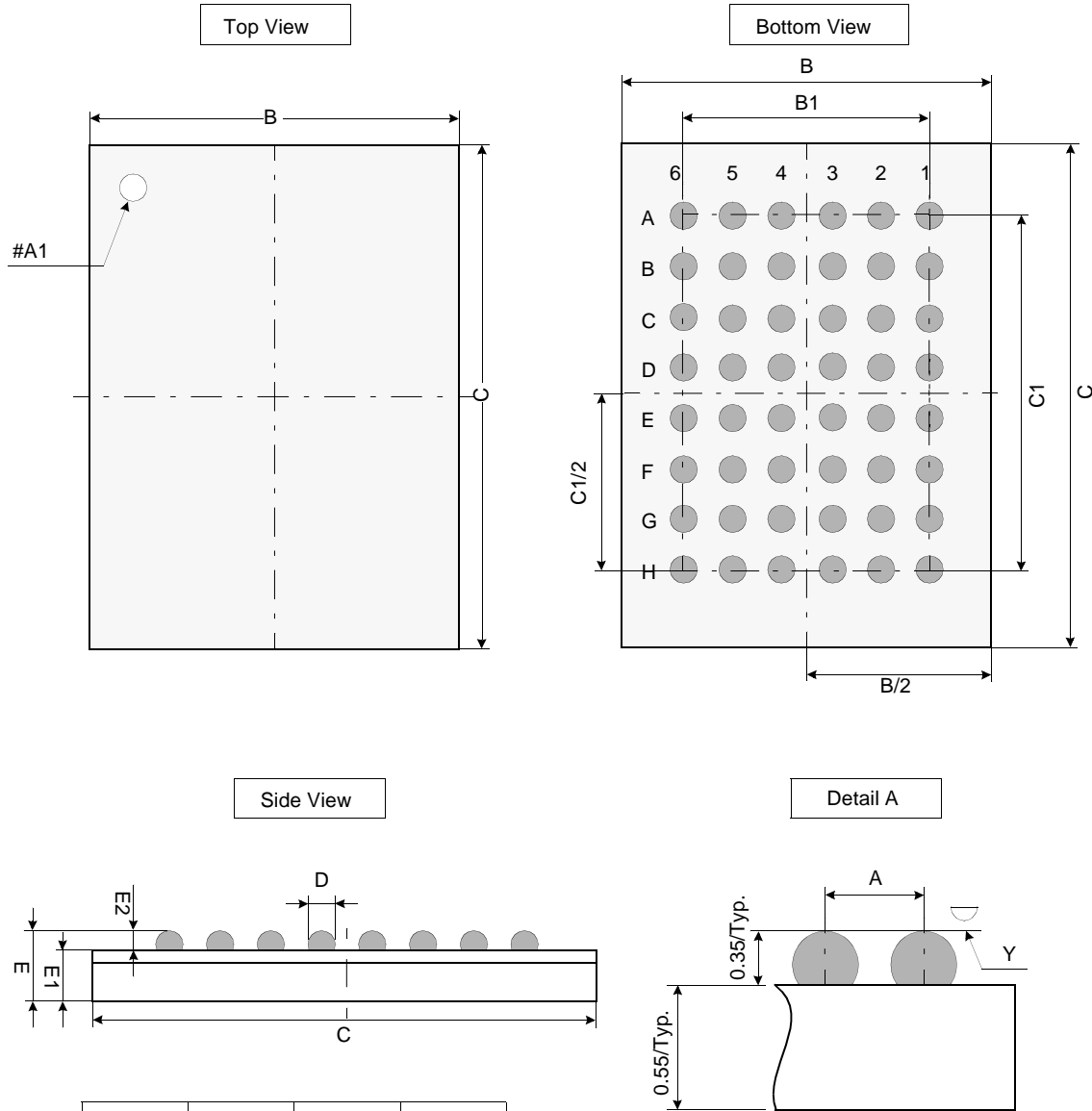
NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low \overline{WE} . A write begins when $\overline{CS1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS1}$ or \overline{WE} going high.

PACKAGE DIMENSION

Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.10

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.10(Max)